

# Modeling and simulation of single-electron transistors

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## ABSTRACT

Single-electron transistor (SET) can offer lower power consumption and faster operating speed in the era of nanotechnology. It operates in single electronics regime where only one electron can tunnel from source to drain via island. Thus single electron tunneling is the phenomena that describe the principle of SET. Owing to the stochastic nature of the tunneling event, a tunneling electron is considered as a discrete charge. To simulate the SET, Monte Carlo method is used due to its reasonable accuracy in the single electronics simulation. A model is described and used to study the electronic properties of SET. Monte Carlo method follows the tunneling path of a representative number of electrons and it can give a clear picture of the inner work of the single electron circuits.

| Modeling | Single-electron transistor | Coulomb blockade | Single-electron tunneling |

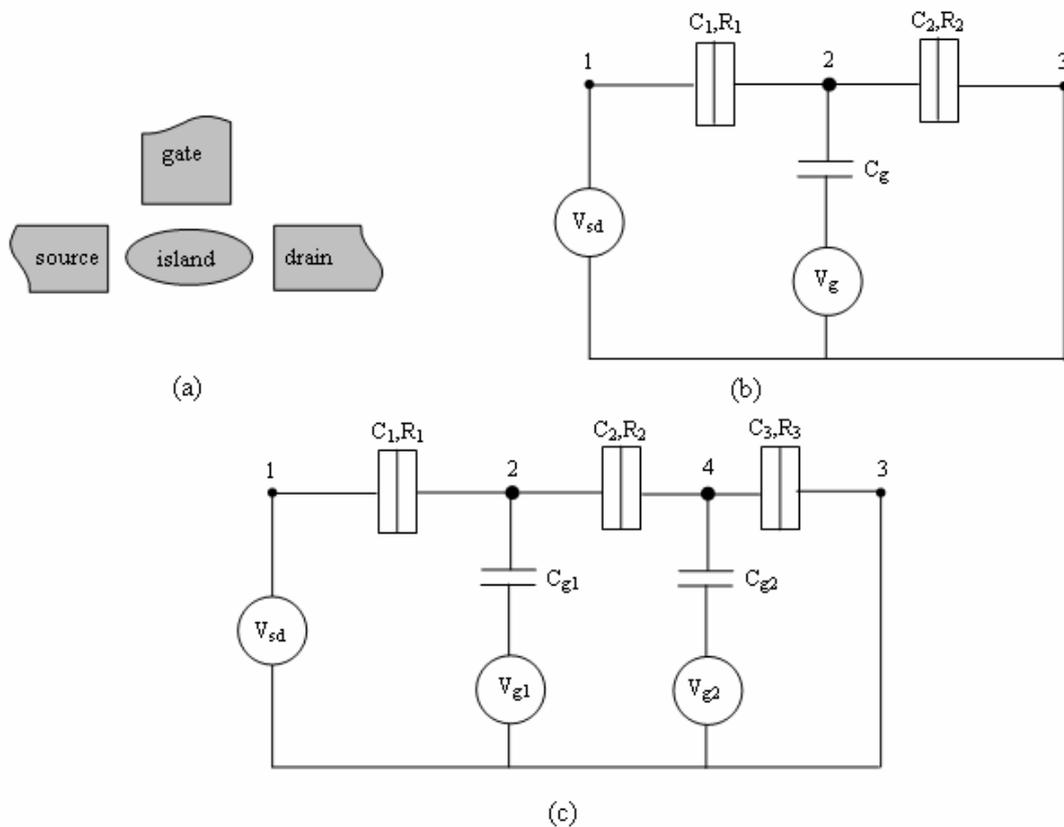
## 1. Introduction

Single-electron transistor (SET) has been received a great attention since a decade as the miniaturization of the technology reaches nano size. Besides offering lower power consumption, SET has the advantage of faster operating speed which these are the attraction nowadays in the fabrication of electronic devices. When nano size is reached, quantum-mechanical effects will come into play in controlling their behavior.

Single electron transistor consists of an island in between a source and drain, with a gate voltage exerted on the island. The so-called Single-Electron Transistor is due to its operation in single electronics regime where only one electron can tunnel from the source to drain via the island. The processes that take place in this nanostructure are Coulomb blockade and single electron tunneling. In this mesoscopic area, the charge discretization and energy contribution from a single electron are not negligible and leads to non-linear I-V characteristic for the device.

A number of modeling methods have been used to study and investigate the phenomena of single electron transistor. Monte Carlo (MC) method has been implemented by several groups [1], whilst Master Equation (ME) formalism has been used to simulate the static and dynamic behavior of the single electron circuit [2,3]. A combination of MC and ME methods have also been used in order to facilitate the study of rare events like cotunneling and to eliminate the burden of state finding [4]. Besides these, there are many other methods were used according to the results desired.

In this study, only MC method is used to investigate the electronic properties of the single electron transistor. MOSES, a Monte Carlo Single-Electronics Simulator is used to implement the simulation.



**Fig. 1** (a) Geometry of SET, (b) Equivalent circuit of SET consisting of tunnel and non-tunnel junctions with ideal voltage sources, (c) SET with double islands.

## 2. Theory and Model

Single electron transistor is considered as a circuit consisting of islands that are arbitrarily connected with tunnel junctions and capacitors as well as ideal voltage sources those control the circuit (see Figure 1). The operating temperature,  $T$  is low such that  $k_B T \ll E_{c \min}$  where  $E_{c \min}$  is the minimum charging energy which is also equal to the energy level spacing of the island,  $k_B$  is the Boltzmann constant, and  $E_c = e^2/2C_\Sigma$ ,  $C_\Sigma$  is the total capacitance of the island. In another way, the junction capacitance should be small enough to ensure that the charging energy exceeds the thermal energy.

Single electron circuits are composed of small tunnel junctions, capacitances, and voltage sources. A tunneling electron can be described as a discrete charge due to stochastic nature of a tunneling event. In Figure 1, node 1 represents source electrode, node 2 (and 4) is island, while node 3 represents drain electrode. In between these nodes are tunnel junctions, which are described by tunnel capacitance,  $C$  and tunnel resistance,  $R$ .

When the bias voltage is zero, Fermi levels of both source and drain are in the state of equilibrium until the bias voltage is exerted. An electron will tunnel independently through the tunnel junctions from source to drain via dot when there is empty state at the energy level of the island which is between the Fermi levels of the electrodes (see Figure 2). The electron tunneling alters the electrostatic potential of the island as well as charge

distribution in the circuit. By adjusting the gate voltage, energy levels can be shifted and control the addition of removal of the electrons and thus ON and OFF the device.

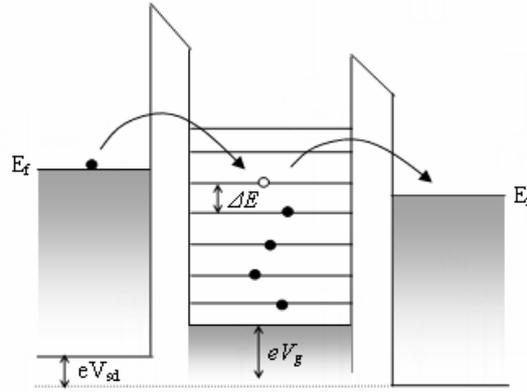


Fig. 2 Schematic band diagram of the single-electron transistor.

Monte Carlo Single-Electronics Simulator simulates single charge tunneling using equation of the so-called orthodox theory [6]. This theory makes the following major assumptions [7]:

- i) The electron energy quantization inside the conductors is ignored, i.e. the electron energy spectrum is treated as continuous.
- ii) The time of electron tunneling through the barrier is assumed to be negligibly small in comparison with other time scales (including the interval between neighboring tunneling events).
- iii) Coherent quantum processes consisting of several simultaneous tunneling events (cotunneling) are ignored. This assumption is valid if the resistance  $R$  of all tunnel barriers of the system is much higher than the quantum unit of resistance  $R_Q$ . This is given by  $R \gg R_Q$ , where  $R_Q = h / e^2 \approx 25.8 \text{ k}\Omega$ .

This third assumption ensures that quantum fluctuation with energy of  $h/RC$  is small compared with the charging energy of the order of  $e^2/2C$ .

To simulate the tunneling of electron, rates of all possible tunneling events have to be determined. The tunneling rate is shown by equation (1).

$$\Gamma = \frac{\Delta E}{e^2 R_T \left( 1 - \exp\left(-\frac{\Delta E}{k_B T}\right) \right)} \quad (1)$$

where  $\Delta E$  is electrostatic energy difference,  $R_T$  is the tunnel resistance. The electrostatic energy difference can be expressed by equation (2). [7]

$$\Delta E = \frac{(ne - Q_e)^2}{2C_\Sigma} - \frac{eV(n_1 C_2 + n_2 C_1)}{C_\Sigma} + \frac{e}{C_g} \quad (2)$$

in which  $e/C_g$  is a constant and  $Q_e$  is the background charge. At single voltage-biased tunnel junction,  $\Delta E$  can be replaced by  $-eV$ . Thus, equation (2) yields linear current-voltage relation  $I_T = e [\Gamma(V) - \Gamma(-V)] = V/R_T$ .

Once all tunnel rates are known, one occurring event is determined with Monte Carlo method. The concrete random tunnel times  $\tau$  are computed for all events by using random number as shown in equation (3) where  $r$  is random number distributed between [0 1].

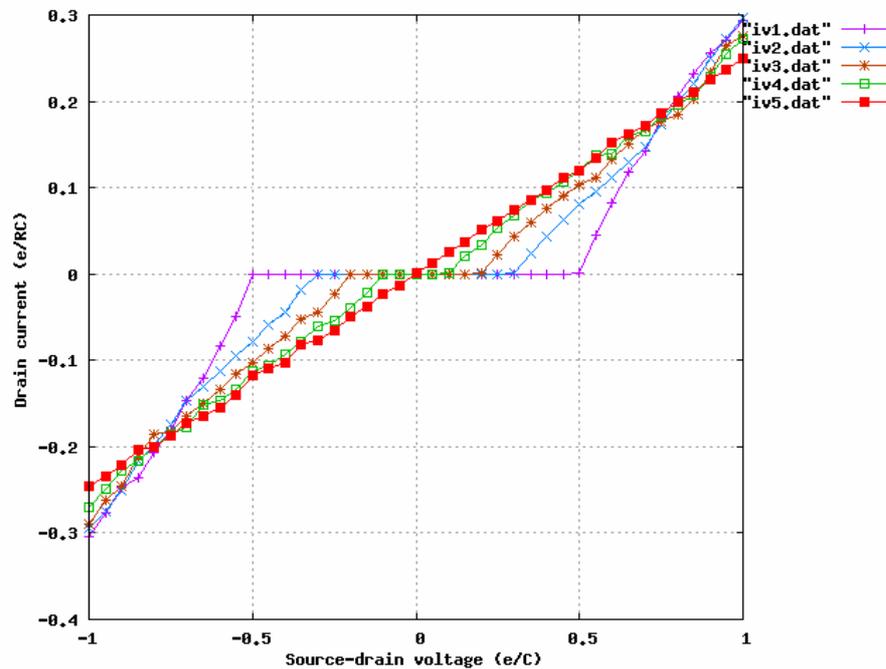
$$\tau = \frac{\ln(r)}{\Gamma} \quad (3)$$

The one with shortest time will be taken as the actually tunnel event. Charges and voltages are updated on all circuit nodes and new tunnel rates are calculated. Macroscopic behavior of the circuit can be obtained by looping this procedure many times.

### 3. Results and Discussion

By understanding the energy of the different charge configuration, many properties of SET can be known. Nonetheless, knowledge of the tunneling rate of the electrons is required for detailed understanding of the I-V characteristic.

Another property of SET extended from the I-V curve described above is that the source-drain current is a periodic function of the gate voltage as shown in Figure 5.



**Fig. 3** I-V characteristic of SET for several values of charge  $Q(2)$  (charge on node 2 of circuit (a) in figure (1)) ( $V_g=0$ ,  $C_1=C_2$ ,  $R_1=R_2$ ,  $T=0K$ ).

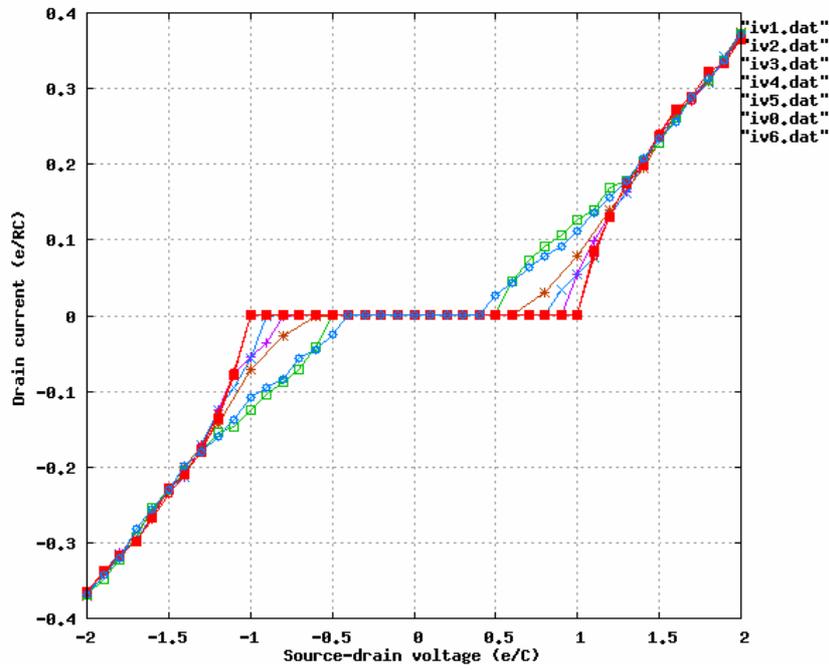


Fig. 4 I-V characteristic for double islands SET for few charge values of node 2 and 4.

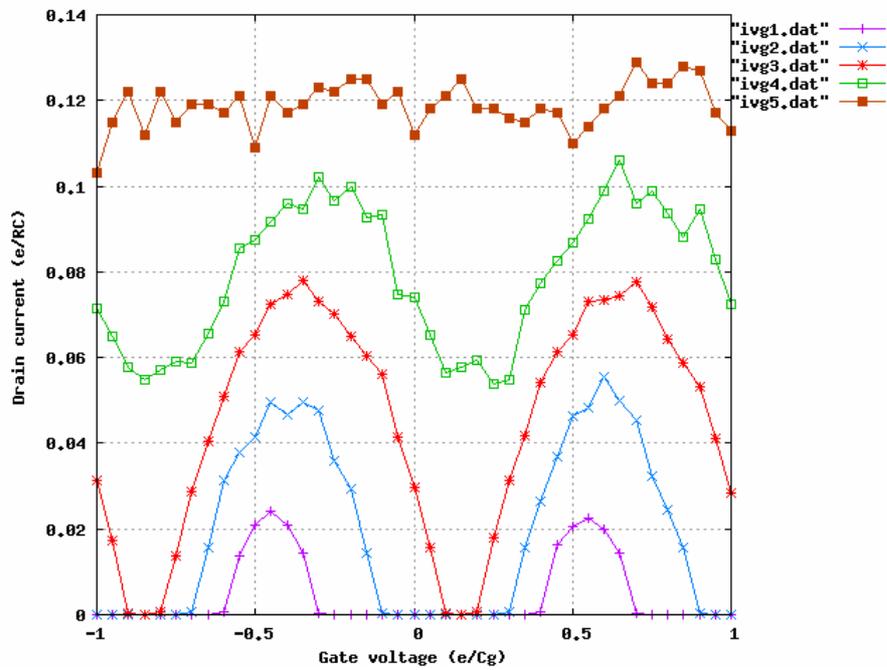


Fig. 5 Relation of current and gate voltage for a few source-drain voltages. ( $C_g = 1 \times 10^{-16}$  F,  $Q(2) = 0$ ).

It can be observed that the current ON and OFF periodically when gate voltage is changing indicating that the gate voltage acts as the transistor switch. The interval where no current flow is the adjustment that gate voltage need for bringing the next available empty state for electron tunneling. Increasing the bias voltage allows more current to flow through. This oscillation occurs in the region of coulomb blockade that is described above. For gate capacitance,  $C_g = 1 \times 10^{-16}$  F, the coulomb blockade threshold has the value of  $0.4e/C$ . The current flows in a discrete style for  $V_{sd}$  of value from  $0.1e/C$  to  $0.3e/C$ . At  $V_{sd} = 0.4 e/C$  and  $0.5e/C$ , the behavior of the device change outside the regime of coulomb blockade. Coulomb blockade charging does not exist and thus the current can flow without suppression.

#### 4. Conclusion

Single electron transistor can be modeled as a circuit consisting of arbitrary configuration of capacitors, tunnel junctions and voltage sources. I-V characteristic explained the behavior of SET that discrete electrons flow onto and off the island through tunnel junctions. Besides that, coulomb blockade charging phenomena play an important role to the SET operation.

#### 5. Acknowledgements

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#### 6. References

- [1] S. Roy, "Simulation tools for the analysis of single electronic systems," Ph.D. dissertation, Univ. of Glasgow, U.K., 1994.
- [2] L. R. C. Fonseca, A. N. Korotkov, K. K. Likharev, and A. A. Odintsov, *J. Appl. Phys.*, 78 (1995) 3238–3251.
- [3] J. R. Barker, S. Babiker, and S. Roy, *Phys. B*, 22 (1997) 787–22791.
- [4] C. Wasshuber, H. Kosina, and S. Selberherr, *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, 3 (1997) 937–944.
- [5] S. Mahapatra, A. Ionescu, and K. Banerjee, *IEEE Electron Device Lett.*, 23 (2002) 366–369.
- [6] D. M. R. Kaplan, "Monte-Carlo Single-Electronics Simulator 1.2 User's Guide".
- [7] K. K. Likharev, *Proceedings of the IEEE87*, (1999) 606.