AN EVOLVABLE BLOCK-BASED NEURAL NETWORK ARCHITECTURE FOR EMBEDDED HARDWARE

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UNIVERSITI TEKNOLOGI MALAYSIA
AN EVOLVABLE BLOCK-BASED NEURAL NETWORK ARCHITECTURE FOR EMBEDDED HARDWARE

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A thesis submitted in fulfilment of the requirements for the award of the degree of Doctor of Philosophy (Electrical Engineering)

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Dedicated to
my beloved family
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ABSTRACT

Evolvable neural networks are a more recent architecture, and differs from the conventional artificial neural networks (ANN) in the sense that it allows changes in the structure and design to cope with dynamic operating environments. Block-based neural networks (BbNN) provide a more unified solution to the two fundamental problems of ANNs, which include simultaneous optimization of structure, and viable implementation in reconfigurable embedded hardware such as field programmable gate arrays (FPGAs) due to its modular structure. However, BbNNs still have several outstanding issues to be resolved for an effective implementation. An efficient hardware design can only be obtained with proper design consideration. To date, there has been no previous work reported on BbNNs configured in recurrent mode for complex case studies, even though it is theoretically possible. Existing BbNN models do not explicitly specify or model the latency of the system, determine how it affects the system, nor how it can be optimized. Also, current methods of training BbNNs using genetic algorithm (GA) are slow, especially with large training datasets. This thesis presents an improved BbNN model, proposes a state-of-the-art simulation and co-design environment for it, and implements it on a hardware platform for improved speed and performance. It has a novel architecture with deterministic outputs that can evolve and operate in both feedforward and recurrent modes. The BbNN is redesigned for optimal system latency to achieve higher performance, and supports on-chip training for multi-objective optimization using a multi-population parallel genetic algorithm. All the algorithms proposed led to an efficient and scalable hardware implementation. The viability of the resulting BbNN system-on-chip (SoC) is proven with real-time performance analysis of real-world case studies, where performance improvements of up to 410× are observed. The hardware logic utilization is minimized with the help of theoretical analysis and design considerations. A case study requiring the use of recurrent mode BbNN is also presented. All case studies tested with the BbNN give equivalent or better classification accuracies compared to those provided in previous works, but with optimized latency values. As an example, the proposed BbNN solution achieves a classification accuracy of 99.41% for the heart arrhythmia case study, which is an improvement over previous work. The validity of the proposed BbNN model is thus verified.
ABSTRAK

## TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>CHAPTER</th>
<th>TITLE</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>DECLARATION</td>
<td></td>
<td>ii</td>
</tr>
<tr>
<td>DEDICATION</td>
<td></td>
<td>iii</td>
</tr>
<tr>
<td>ACKNOWLEDGEMENT</td>
<td></td>
<td>iv</td>
</tr>
<tr>
<td>ABSTRACT</td>
<td></td>
<td>v</td>
</tr>
<tr>
<td>ABSTRAK</td>
<td></td>
<td>vi</td>
</tr>
<tr>
<td>TABLE OF CONTENTS</td>
<td></td>
<td>vii</td>
</tr>
<tr>
<td>LIST OF TABLES</td>
<td></td>
<td>xii</td>
</tr>
<tr>
<td>LIST OF FIGURES</td>
<td></td>
<td>xiv</td>
</tr>
<tr>
<td>LIST OF ABBREVIATIONS</td>
<td></td>
<td>xix</td>
</tr>
<tr>
<td>LIST OF SYMBOLS</td>
<td></td>
<td>xxi</td>
</tr>
<tr>
<td>LIST OF APPENDICES</td>
<td></td>
<td>xxii</td>
</tr>
</tbody>
</table>

1 INTRODUCTION 1

1.1 Block-based Neural Networks 2
1.2 Problem Statement 3
1.3 Objectives 6
1.4 Scope of Work 6
1.5 Contributions 8
1.6 Dissertation Organization 9

2 LITERATURE REVIEW AND THEORETICAL BACKGROUND 11

2.1 Artificial Neural Networks (ANN) 11
  2.1.1 Background Theory of ANNs 11
  2.1.2 Neuron Activation Functions 13
  2.1.3 Common Criticism of Conventional ANNs 16
2.2 Background Theory of BbNNs 18
  2.2.1 Previous Work on BbNNs in Hardware 20
2.3 Genetic Algorithm
  2.3.1 Multi-objective Optimization Models Using GA

2.4 Previous Work on Selected Case Studies
  2.4.1 Driver Drowsiness Classification Using Heart Rate Variability
  2.4.2 ECG Signal Classification in Detection Heart Arrhythmia
  2.4.3 Tomita Language Grammar Inference

3 METHODOLOGY

3.1 Research Approach
  3.1.1 System Latency and GA-based Training for the Proposed BbNN
  3.1.2 Design Considerations in Neuron Block Hardware Development
  3.1.3 Design Approach of the Simulation Model for the Proposed BbNN
  3.1.4 Hardware Design: Co-Design and SoC Implementation

3.2 Software Tools and Design Environment
  3.2.1 The GAlib Library
  3.2.2 Mentor Graphics Modelsim
  3.2.3 Icarus Verilog
  3.2.4 Verilator
  3.2.5 Nios2-Linux Embedded Operating System

3.3 Hardware Design Verification Methodology
  3.3.1 Using the Command-line Version of Modelsim for Verification
  3.3.2 Using SystemVerilog DPI-C in Modelsim for Co-Verification
  3.3.3 Viewing Waveforms with GTKWave
  3.3.4 Using Icarus Verilog for Verification
  3.3.5 Using Verilator for Advanced Co-Simulation

3.4 Case Studies for Verification of the Proposed BbNN
  3.4.1 Test Dataset Creation from HRV Feature Vectors for Case Study 2
4 MODELING, ALGORITHMS, AND SIMULATION OF PROPOSED BLOCK-BASED NEURAL NETWORKS 63

4.1 BbNN as a Structured Neural Network 63
4.2 Modeling of a Neuron Block in the Proposed BbNN 65
   4.2.1 System Latency and Synchronous Logic Structure of Neuron Blocks 68
   4.2.2 Design Considerations: Range of Values for the Synaptic Weights 71
4.3 GA-based Training and Optimization of the Proposed BbNN 72
   4.3.1 Formulation of the GA Fitness Function 75
4.4 BbNN Array Interconnect Algorithm 79
4.5 Implementation of the BbNN Simulation Model 84

5 HARDWARE DESIGN AND IMPLEMENTATION 87

5.1 System Architecture of BbNN in Hardware 87
5.2 Hardware Design Considerations 89
   5.2.1 Number Representation for Fixed-Point Arithmetics and Precision 89
   5.2.2 Activation Function of the Hardware Neuron Block 92
5.3 Design of the Proposed Hardware Neuron Block 96
   5.3.1 Neuron Block FSM Control Unit 98
   5.3.2 Multiplexing Sequence of the Multiplier Inputs 100
   5.3.3 Neuron Block Dual-Port On-chip Memory Submodule 102
   5.3.4 Neuron Block Input Multiplexer Submodule 104
   5.3.5 Neuron Block ALU Submodule 105
   5.3.6 Neuron Block Operand Selector Submodule 108
6 EXPERIMENTAL RESULTS, CASE STUDIES, AND ANALYSIS

6.1 Analysis to Obtain Optimum Range of Weight Values
   6.1.1 Geometric Analysis of a Neuron Block with One Synapse
   6.1.2 Geometric Analysis of a Neuron Block with Two Synapses
   6.1.3 Geometric Analysis of a Neuron Block with Three Synapses
   6.1.4 Weight Boundary Selection and Empirical Analysis

6.2 Verification and Analysis of Proposed BbNN through Case Studies
   6.2.1 Functional Verification of Proposed BbNN Using the XOR Classification Problem
   6.2.2 Case Study 2: Driver Drowsiness Detection Based on HRV
   6.2.3 Case Study 3: Heart Arrhythmia Classification from ECG Signals
   6.2.4 Case Study 4: Grammar Inference of the Tomita Language

6.3 Verification of the BbNN Implementation Model in Hardware
   6.3.1 Simulation Results of the Neuron Block Submodules
   6.3.2 Simulation Results of the Neuron Block
   6.3.3 Co-Simulation of BbNN HW-SW Design

6.4 Resource Utilization of the BbNN Implementation Model in Hardware

6.5 Performance Analysis of the Proposed BbNN Models
   6.5.1 Single Thread vs Multithreaded BbNN Simulation Models
6.5.2 Software vs Verilated BbNN Simulation Models 144
6.5.3 Embedded Software vs Hardware BbNN Implementation Models 144

7 CONCLUSION 147
7.1 Concluding the Experimental Results 148
7.2 Contributions 150
7.3 Future Work 151

REFERENCES 153
Appendices A – E 160 – 182
## LIST OF TABLES

<table>
<thead>
<tr>
<th>TABLE NO.</th>
<th>TITLE</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.1</td>
<td>All the required multiplication operands used for computing Equation 5.12-5.15 used in this work.</td>
<td>101</td>
</tr>
<tr>
<td>5.2</td>
<td>Summary of ALU adder operation based on opcode.</td>
<td>106</td>
</tr>
<tr>
<td>5.3</td>
<td>The values of Sel.Addr, Sel.X and Sel.Y based on the operand counter that is required by the state machine.</td>
<td>109</td>
</tr>
<tr>
<td>5.4</td>
<td>Description of all the registers in the BbNN controller module.</td>
<td>111</td>
</tr>
<tr>
<td>6.1</td>
<td>Distribution cases for Equation 6.1.</td>
<td>115</td>
</tr>
<tr>
<td>6.2</td>
<td>Distribution cases for Equation 6.2 with an ignored bias ($b = 0$).</td>
<td>117</td>
</tr>
<tr>
<td>6.3</td>
<td>All possible combination of offsets used on Equation 6.2 with $x_1$ and $x_2$ preset to maximum positive values.</td>
<td>119</td>
</tr>
<tr>
<td>6.4</td>
<td>Parameters used for GA evolution for this analysis.</td>
<td>122</td>
</tr>
<tr>
<td>6.5</td>
<td>Statistics of generations required by GA to achieve a fitness of 0.95 when training a $7 \times 1$ BbNN for classification of heart arrhythmia.</td>
<td>122</td>
</tr>
<tr>
<td>6.6</td>
<td>XOR training dataset for the BbNN structure.</td>
<td>123</td>
</tr>
<tr>
<td>6.7</td>
<td>Parameters used for GA evolution.</td>
<td>125</td>
</tr>
<tr>
<td>6.8</td>
<td>Results on BbNN classification accuracy of heart arrhythmia using individual record training.</td>
<td>129</td>
</tr>
<tr>
<td>6.9</td>
<td>Benchmarking results on BbNN classification accuracy of the heart arrhythmia case study with all records combined.</td>
<td>130</td>
</tr>
<tr>
<td>6.10</td>
<td>Results on BbNN classification accuracy for Tomita languages.</td>
<td>131</td>
</tr>
<tr>
<td>6.11</td>
<td>Results on BbNN configuration and optimum latency achieved for each Tomita language.</td>
<td>132</td>
</tr>
<tr>
<td>6.12</td>
<td>Benchmarking results in classification accuracy for the grammar inferencing case study.</td>
<td>133</td>
</tr>
<tr>
<td>6.13</td>
<td>The training accuracy and latency of all the case studies tested with the verilated BbNN model.</td>
<td>139</td>
</tr>
</tbody>
</table>
6.14 FPGA logic utilization of the proposed design in relation to previous works using various neuron block array configurations.

6.15 Selected FPGA prototyping platform and BbNN bit precision for the proposed design in comparison with previous work.

6.16 Benchmark of the processors used in this work.

6.17 Performance analysis for the training of single and multithreaded BbNN simulation models.

6.18 Performance analysis for the training of the software and verilated BbNN simulation models.

6.19 Performance analysis for both embedded software and hardware implementation BbNN models for various latency values.

6.20 Performance analysis for the training of the embedded software and hardware implementation BbNN models.
# LIST OF FIGURES

<table>
<thead>
<tr>
<th>FIGURE NO.</th>
<th>TITLE</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>A multilayer-perceptron ANN with a single hidden layer.</td>
<td>1</td>
</tr>
<tr>
<td>1.2</td>
<td>Neuron blocks interconnected as a scalable grid to form a BbNN structure [8].</td>
<td>2</td>
</tr>
<tr>
<td>1.3</td>
<td>Example of a $2 \times 2$ BbNN structure configured in recurrent mode.</td>
<td>4</td>
</tr>
<tr>
<td>1.4</td>
<td>Layers of the proposed embedded BbNN SoC.</td>
<td>8</td>
</tr>
<tr>
<td>2.1</td>
<td>A single neuron with three synapses in a conventional ANN.</td>
<td>12</td>
</tr>
<tr>
<td>2.2</td>
<td>A multilayer-perceptron ANN with a single hidden layer.</td>
<td>12</td>
</tr>
<tr>
<td>2.3</td>
<td>The observable bell shaped curve from the plot of a sigmoidal function.</td>
<td>15</td>
</tr>
<tr>
<td>2.4</td>
<td>Depiction of a massively interconnected multilayer-perceptron ANN.</td>
<td>17</td>
</tr>
<tr>
<td>2.5</td>
<td>Neuron blocks interconnected as a scalable grid to form a BbNN structure [8].</td>
<td>18</td>
</tr>
<tr>
<td>2.6</td>
<td>Functional block diagram of a neuron block in hardware as described in [20, 36, 37].</td>
<td>21</td>
</tr>
<tr>
<td>2.7</td>
<td>Behavioral flow chart for Simple GA [38].</td>
<td>23</td>
</tr>
<tr>
<td>2.8</td>
<td>Spectral analysis of heart rate using the three different power bands.</td>
<td>27</td>
</tr>
<tr>
<td>2.9</td>
<td>ECG signals from a patient depicting (a) a normal heartbeat and (b) a heartbeat with premature ventricular contraction (PVC).</td>
<td>29</td>
</tr>
<tr>
<td>3.1</td>
<td>BbNN structure with a latency of three computational cycles.</td>
<td>33</td>
</tr>
<tr>
<td>3.2</td>
<td>Verification of the neuron block using Modelsim and DPI-C interfacing with a golden reference software model as comparison.</td>
<td>37</td>
</tr>
<tr>
<td>3.3</td>
<td>Methodology for co-simulation of the BbNN hardware design using Verilator and C/C++.</td>
<td>37</td>
</tr>
<tr>
<td>3.4</td>
<td>Layers of the proposed embedded BbNN SoC.</td>
<td>38</td>
</tr>
</tbody>
</table>
3.5 Diagram of the connection between Nios2-Linux, FPGA, Nios II CPU and the external hardware.

3.6 The testbench design environment [69].

3.7 Constrained-random test progress over time vs. directed testing [69].

3.8 Modelsim compilation and simulation output for the TestVerilog module.

3.9 Verification of a hardware module using Modelsim and DPI-C interfacing with a golden reference software model as comparison.

3.10 GTKWave displaying the waveforms of a simulated module.

3.11 The methodology of verifying a design using Verilator by converting SystemVerilog hardware modules into cycle accurate C/C++ libraries.

3.12 Output from the C/C++ verification program for testing the verilated adder module.

3.13 HRV sleep state classification using BbNN.

3.14 QRS complex detection.

3.15 HR plotting at the center of every RR interval.

3.16 HRV extraction to obtain power bands.

3.17 Spectral analysis of HR.

3.18 Overview of ECG signal preprocessing and feature extraction.

3.19 ECG signal preprocessing flow.

4.1 Diagram depicting (a) neuron blocks interconnected as a scalable grid to form a BbNN structure and (b) an example of a configured neuron block.

4.2 All possible internal configurations of a neuron block.

4.3 Conceptual model of a single neuron block.

4.4 BbNN structure with a latency of (a) five computational cycles and (b) three computational cycles.

4.5 Example of a recurrent mode 2 × 2 BbNN structure.

4.6 A flowchart depicting the (a) basic concept of the BbNN training model and (b) multi-population parallel GA with migration applied in this work.

4.7 Encoding the chromosome of a BbNN structure.

4.8 A r × c BbNN with detailed labeling of the input/output interconnects.

4.9 Architecture of the proposed BbNN simulation model.
4.10 CPU utilization during BbNN training.
5.1 System architecture of the proposed FPGA-based BbNN SoC.
5.2 Layers of the proposed embedded BbNN SoC.
5.3 The Q4.11 fixed-point number format used in this work.
5.4 A neuron block with the maximum possible combination of weights connected to the output neuron.
5.5 Performing addition (or subtraction) using fixed-point arithmetic on Q4.11 type numbers.
5.6 Performing multiplication using fixed-point arithmetic on Q4.11 type numbers with truncation.
5.7 Plot of the proposed piecewise quadratic (PWQ) function.
5.8 Functional block diagram of the proposed neuron block in hardware.
5.9 Algorithmic state machine chart for the FSM control unit.
5.10 Individual interconnections of the multiplier unit within the neuron block.
5.11 Block diagram of the dual-port on-chip memory of the neuron block.
5.12 Using the direction bits to perform a conditional statement to enable or disable the first operand.
5.13 The architecture of the input multiplexer within the neuron block.
5.14 The architecture of the ALU within the neuron block.
5.15 The logic circuit for obtaining the select signal $S_2$.
5.16 Logic circuit for determining the positive and negative limit of the $x$ value in register A.
5.17 Block diagram of the operand selector module within the neuron block.
5.18 Functional block diagram of the BbNN controller module designed for handling the CPU bus interface.
6.1 A neuron block with one synapse connected to the output node.
6.2 Geometric structure of Equation 6.1 for both input cases with weights ranging from $-1$ to $+1$.
6.3 Geometric structure of Equation 6.1 with weights ranging from $-3$ to $+3$.
6.4 A neuron block with two synapses connected to the output node.
6.5 Geometric structure of Equation 6.2 with weights ranging from $-1$ to $+1$ using (a) ignored bias and (b) maximum bias offset.

6.6 Geometric structure of Equation 6.2 with weights ranging from $-3$ to $+3$ with (a) maximum positive bias offset and (b) maximum negative bias offset.

6.7 A neuron block with three synapses connected to the output node for mathematical analysis.

6.8 Geometric structure of Equation 6.3 for case 7 with weights ranging from (a) $-1$ to $+1$ and (b) $-3$ to $+3$.

6.9 Geometric structure of Equation 6.3 for case 8 with weights ranging from (a) $-1$ to $+1$ and (b) $-3$ to $+3$.

6.10 Geometric structure of Equation 6.3 for case 9 with weights ranging from (a) $-1$ to $+1$ and (b) $-3$ to $+3$.

6.11 Evolved BbNN that solves the XOR problem.

6.12 Fitness trend of the BbNN evolution for the XOR problem case study.

6.13 Evolved BbNN structure in driver drowsiness detection.

6.14 Fitness trend of the BbNN evolution for the driver drowsiness detection case study.

6.15 Fitness trend of the BbNN evolution for the heart arrhythmia classification case study.

6.16 Evolved BbNN structure for the classification of heart arrhythmia using all records combined as training data.

6.17 Evolved BbNN structure for the classification of Tomita language 3.

6.18 Fitness trend of the BbNN evolution for the grammar inference of Tomita language 3.

6.19 Simulation results (in dumpfile form) for the dual-port on-chip memory.

6.20 Simulation results (in dumpfile form) for the ALU submodule.

6.21 Simulation results (in dumpfile form) for the FSM submodule.

6.22 Simulation results (in dumpfile form) for the operand selector submodule.

6.23 SystemVerilog testbench with DPI-C interfacing for co-verification of the neuron block.

6.24 Results of the neuron block co-verification routine.
<table>
<thead>
<tr>
<th>Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.25</td>
<td>Co-simulation of the BbNN hardware design using Verilator and C/C++.</td>
</tr>
<tr>
<td>6.26</td>
<td>Terminal output from the training algorithm after successfully training the verilated BbNN hardware applied on case study 2.</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Full Form</td>
</tr>
<tr>
<td>--------------</td>
<td>-----------</td>
</tr>
<tr>
<td>ALU</td>
<td>Arithmetic Logic Unit</td>
</tr>
<tr>
<td>ANN</td>
<td>Artificial Neural Network</td>
</tr>
<tr>
<td>BPF</td>
<td>Band Pass Filter</td>
</tr>
<tr>
<td>BbNN</td>
<td>Block-based Neural Network</td>
</tr>
<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
</tr>
<tr>
<td>DDR SDRAM</td>
<td>Double Data Rate Synchronous Dynamic Random-Access Memory</td>
</tr>
<tr>
<td>DPI</td>
<td>Direct Programming Interface</td>
</tr>
<tr>
<td>DUT</td>
<td>Device-Under-Test</td>
</tr>
<tr>
<td>DUV</td>
<td>Device-Under-Verification</td>
</tr>
<tr>
<td>EA</td>
<td>Evolutionary Algorithm</td>
</tr>
<tr>
<td>ECG</td>
<td>Electrocardiogram</td>
</tr>
<tr>
<td>FFT</td>
<td>Fast Fourier Transform</td>
</tr>
<tr>
<td>FPU</td>
<td>Floating Point Unit</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
</tr>
<tr>
<td>FSM</td>
<td>Finite State Machine</td>
</tr>
<tr>
<td>GA</td>
<td>Genetic Algorithm</td>
</tr>
<tr>
<td>GCC</td>
<td>GNU Compiler Collection</td>
</tr>
<tr>
<td>GNU</td>
<td>Gnu’s Not Unix</td>
</tr>
<tr>
<td>GUI</td>
<td>Graphical User Interface</td>
</tr>
<tr>
<td>HDL</td>
<td>Hardware Description Language</td>
</tr>
<tr>
<td>HF</td>
<td>High Frequency</td>
</tr>
<tr>
<td>HPF</td>
<td>High Pass Filter</td>
</tr>
<tr>
<td>HRV</td>
<td>Heart Rate Variability</td>
</tr>
<tr>
<td>HW</td>
<td>Hardware</td>
</tr>
<tr>
<td>HW-SW</td>
<td>Hardware-Software</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>I/O</td>
<td>Input/Output</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Definition</td>
</tr>
<tr>
<td>--------------</td>
<td>------------</td>
</tr>
<tr>
<td>LE</td>
<td>Logic Elements</td>
</tr>
<tr>
<td>LF</td>
<td>Low Frequency</td>
</tr>
<tr>
<td>LPF</td>
<td>Low Pass Filter</td>
</tr>
<tr>
<td>LUT</td>
<td>Lookup Table</td>
</tr>
<tr>
<td>Mbit</td>
<td>Mega Bits</td>
</tr>
<tr>
<td>MDIPS</td>
<td>Millions of Dhrystone Instructions Per Second</td>
</tr>
<tr>
<td>MHz</td>
<td>Mega Hertz</td>
</tr>
<tr>
<td>MLP</td>
<td>Multilayer perceptron</td>
</tr>
<tr>
<td>MMU</td>
<td>Memory Management Unit</td>
</tr>
<tr>
<td>ms</td>
<td>Millisecond</td>
</tr>
<tr>
<td>MUX</td>
<td>Multiplexer</td>
</tr>
<tr>
<td>MWIPS</td>
<td>Millions of Whetstone Instructions Per Second</td>
</tr>
<tr>
<td>NoC</td>
<td>Network-on-Chip</td>
</tr>
<tr>
<td>ns</td>
<td>Nanosecond</td>
</tr>
<tr>
<td>OS</td>
<td>Operating System</td>
</tr>
<tr>
<td>PC</td>
<td>Personal Computer</td>
</tr>
<tr>
<td>PWL</td>
<td>Piecewise Linear</td>
</tr>
<tr>
<td>PWQ</td>
<td>Piecewise Quadratic</td>
</tr>
<tr>
<td>RTL</td>
<td>Register Transfer Level</td>
</tr>
<tr>
<td>RTOS</td>
<td>Real Time Operating System</td>
</tr>
<tr>
<td>SoC</td>
<td>System-on-Chip</td>
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<tr>
<td>SOM</td>
<td>Self Organizing Maps</td>
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<tr>
<td>SW</td>
<td>Software</td>
</tr>
<tr>
<td>USB</td>
<td>Universal Serial Bus</td>
</tr>
<tr>
<td>VHDL</td>
<td>Very High Speed Integrated Circuit Hardware Description Language</td>
</tr>
<tr>
<td>VLF</td>
<td>Very Low Frequency</td>
</tr>
<tr>
<td>WFDB</td>
<td>Waveform Database</td>
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</tbody>
</table>
LIST OF SYMBOLS

$x_{0−3}$ – Inputs of a neuron block

$y_{0−3}$ – Outputs of a neuron block

$w_{0−5}$ – Weight values for the synapses inside a neuron block

$b_{0−3}$ – Bias values for the nodes inside a neuron block

$d_{0−3}$ – Direction values for the neuron block interconnects

$r$ – The amount or rows in a BbNN structure

$c$ – The amount or columns in a BbNN structure

$f_{BbNN}$ – Fitness value of the BbNN structure

$P_{err}$ – BbNN error parameter

$P_{LQ}$ – BbNN latency quality parameter

$P_{pen}$ – BbNN penalty parameter

$\alpha$ – General scaling or modifier constant

$\beta$ – General scaling or modifier constant

$\beta_{1−3}$ – BbNN parameter scaling constants

$L_s$ – Specified latency value of the BbNN system

$L_{min}$ – Minimum possible latency value

$L_{max}$ – Maximum possible latency value

$\sigma$ – Latency modifier for $L_{max}$

$\phi$ – Latency offset for $L_{min}$

$N_{inv}$ – Number of neuron blocks with invalid configurations

$g(x)$ – General representation of an activation function

$s_p$ – Activation function saturation point

$C_a$ – Classification accuracy

$T_P$ – The number of true positives

$F_P$ – The number of false positives

$T_N$ – The number of true negatives

$F_N$ – The number of false negatives
# LIST OF APPENDICES

<table>
<thead>
<tr>
<th>APPENDIX</th>
<th>TITLE</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Publications</td>
<td>160</td>
</tr>
<tr>
<td>B</td>
<td>BbNN Simulation Model Source Codes</td>
<td>162</td>
</tr>
<tr>
<td>C</td>
<td>BbNN Hardware Implementation Source Codes</td>
<td>167</td>
</tr>
<tr>
<td>D</td>
<td>Verification Routines</td>
<td>176</td>
</tr>
<tr>
<td>E</td>
<td>Octave Routines used for Experimentation and Data Preparation</td>
<td>182</td>
</tr>
</tbody>
</table>
An artificial neural network (ANN) is a mathematical model inspired by biological neural networks [1]. A neural network consists of an interconnected group of artificial neurons, and it processes information using a connectionist approach to computation. Typically, ANNs are used in adaptive systems that require a training phase to properly configure itself to perform a classification or control task. Figure 1.1 depicts a multilayer perceptron ANN with a single hidden layer.

ANNs have been successfully deployed in solving various kinds of classification and control problems, which include speech recognition, image analysis, adaptive control, and biomedical signal analysis [1–3]. Typically, existing ANN solutions are based on statistical estimations of a given complex problem, in which the relation between the datasets are inferred through heuristics during the training process.

However, ANNs have been criticized for many shortcomings [4, 5]. One weakness of conventional ANNs is the difficulty of obtaining an optimal structure.
for a given problem. Another issue is that the internal structure of conventional ANNs are rigid, massively interconnected, and allows for little change, making it unsuitable for digital hardware implementation. Also, most types of neural networks are computationally intensive and cannot be implemented in embedded software without sacrificing real time execution [5].

1.1 Block-based Neural Networks

Evolvable neural networks are a more recent architecture, and differs from the conventional ANNs in the sense that it allows changes in the structure and design to cope with dynamic operating environments [6]. Block-based neural networks (BbNNs) were first introduced in 2001 by Moon and Kong [7]. It provides a more unified solution to the two fundamental problems of ANN, which include simultaneous optimization of structure, and viable implementation in reconfigurable digital hardware such as field programmable gate arrays (FPGAs). A BbNN structure is a network of neuron blocks interconnected in the form of a grid as shown in Figure 1.2. A neuron block is a basic data processing unit comprising of a neural network having four variable input/output nodes.

![Neuron blocks interconnected as a scalable grid to form a BbNN structure](image)

**Figure 1.2:** Neuron blocks interconnected as a scalable grid to form a BbNN structure [8].
BbNNs have a modular structure, allowing it to be scaled easily by adding or removing neuron blocks. It has been successfully deployed for various kinds of classification problems [6], and is specifically meant to be implemented in digital hardware due to its regular structure. The number of rows ($r$) and columns ($c$) differ according to the complexity of the problem being tackled. In addition to this, the internal configuration of the neuron blocks can also change or evolve according to the problem being tackled. These two structural aspects can change dynamically, and provide the evolutionary feature of a BbNN system.

Optimization algorithms are used for training BbNN structures, as is in the case of most evolvable ANNs. Almost all previous work reported in literature make use of genetic algorithm (GA), a search heuristic that mimics the process of natural evolution [9]. The GA methodology has been shown to be able to solve difficult and complex problems that fall in the domain of optimization and search. In GA, a chromosome represents a possible solution, and the chromosome is divided into genes which represent parameters of the solution to a problem. Hence in digital systems, a chromosome is represented in the form of a binary string [10]. In the case of BbNN training, the chromosome represents the synaptic weights and configuration of the BbNN structure.

BbNNs have been successfully used in various applications such as ECG signal classification [8], hypoglycemia detection [11], pattern recognition [12], heart rate variation [13, 14], network intrusion [15, 16], mobile robot control [7], dynamic fuzzy control [17] and many more [6]. Most of these works report very high classification rates, often outperforming equivalent regular ANNs designs. This is mostly due to its evolvable structure.

### 1.2 Problem Statement

The main advantage of BbNNs when compared to other forms of evolvable ANNs is its modular structure, making it a very promising candidate for an efficient hardware implementation. Hardware implementation platforms such as FPGAs have limited logic elements, and efficient neural network designs allow better resource utilization. Efficient hardware implementation of BbNN structures is the primary goal of this thesis.
Even though BbNNs give relatively promising results as reported in current literature, there are still several outstanding issues to be resolved with currently defined models. These relate to the modeling, hardware design, and optimization of BbNN structures. This thesis tackles these issues by redefining certain aspects of BbNN operation in order to obtain an improved model for better hardware and software implementation. It is likely that the reluctant adoption of BbNNs in practical applications is related to these outstanding issues. Also, to properly apply BbNNs in complex real world problems, it should ideally be implemented in hardware, and must be able to handle on-chip training.

Despite the wide range of applications reported in literature, to date there has been no work reported on BbNNs configured in recurrent mode for complex case studies, even though it is theoretically possible [7]. This is due to a lack of a time-step model required for the design and simulation of recurrent neural networks. Figure 1.3 shows an example of a $2 \times 2$ BbNN structure configured in recurrent mode. The behavior of such a configuration in hardware would be indeterministic if a registered architecture is not used, and would normally result in an asynchronous feedback that can lead to circuit metastability. Existing BbNN models in literature do not discuss registering the outputs of the neuron blocks in depth, nor do they include a latency variable that is essential for properly using such models.

![Diagram of a $2 \times 2$ BbNN structure configured in recurrent mode.](image)

**Figure 1.3**: Example of a $2 \times 2$ BbNN structure configured in recurrent mode.

Related to the recurrent BbNN issue mentioned above, existing BbNN models do not explicitly specify or model the latency of the system, determine how it affects the system, nor how it can be optimized. This is important because optimizing the
latency not only provides obvious benefits such as improved performance and reduced power consumption, but also allows the BbNN to behave in a more deterministic manner. This deterministic behavior will allow BbNNs to be able to function properly in recurrent or feedback mode, and can even have internal configurations that would have been normally deemed invalid. Also, previous works on BbNNs [6, 11, 12, 15, 17–20] are difficult to be repeated without latency control because specifying different latency values will often cause different results to appear at the outputs. This thesis proposes a redefined BbNN model with latency control taken into account.

Another issue with BbNN structures is in regards to its hardware design. Previous work only presented the modeling of the BbNN, after which a hardware design is obtained [20, 21]. The methodology and process of mapping the models to hardware are not provided, thus leaving several open questions on the design considerations such as the architectural options, system partitioning, selected activation function, lower/upper limits of internal network parameters (synaptic weight and neuron biases), number representation for arithmetic operations (fixed or floating point), bit precision, finite state machine flow, and register transfer level (RTL) design.

The optimum range for the lower/upper limits of internal network parameters, such as the synaptic weight, neuron biases, and activation function saturation points are not clearly defined in existing work. An efficient hardware design can only be obtained after the optimum range of these values is known. The main rationale of using BbNNs instead of conventional ANNs is the advantage in hardware utilization, but this cannot be achieved if the hardware design is not efficient. This thesis explores this aspect of BbNN modeling with the goal of obtaining an optimal neuron block design for effective hardware implementation.

Current methods of training BbNNs using GA are slow, especially with large training datasets. The problem worsens when training for recurrent BbNNs whereby the convergence rate will drop significantly. An improved GA mechanism is required to improve speed and convergence rate, as well as to allow multithreaded simulation of BbNN structures for parallel fitness evaluation. This will allow the use of superior computational techniques to be applied on BbNN training, such as supercomputing clusters or parallelized FPGAs.

BbNNs, like most evolvable ANNs, have complex neuron interconnects. The interconnections are simple for small BbNN structures, but gradually increase in complexity as the structure grows bigger. Thus a parameterizable interconnection
algorithm is required for experimentation, and will not only be useful for creating scalable BbNN structures in simulation models, but also facilitate automated generation of interconnects in hardware implementations. To date, no such algorithm exists in published literature. Such an algorithm would be complex and prone to errors, and the lack of this in current literature is possibly another reason for the reluctant adoption of BbNN systems.

1.3 Objectives

The primary objective of this thesis is to improve on existing BbNN models, to propose a state-of-the-art simulation and co-design environment for it, and to implement it on hardware for performance analysis. In detail, the objectives of this thesis are:

1. To propose a block-based neural network (BbNN) architecture that has the following novel features:
   - Evolvable architecture with deterministic outputs that can operate in both feedforward and recurrent mode.
   - Redesigned for optimal system latency to achieve higher performance.
   - On-chip training and multi-objective optimization using state-of-the-art parallel genetic algorithms.
   - Allows for an efficient and scalable hardware implementation.
   - Provides a platform for effective solutions to real world complex classification problems.

2. To develop an effective implementation platform for practical BbNN solutions that is based on FPGA embedded hardware, and prove the viability of the resulting hardware-software design with real-time performance analysis of complex, real world case studies.

1.4 Scope of Work

The work in this thesis uses a combination of tools mostly obtained from open source software and libraries. This allows for a work that is easier to repeat in the future. The platform for testing and using BbNN models are built from scratch using a
variety of tools. The software tools and prototyping platform applied in this thesis are described as follows:

a) Algorithmic models are verified and analyzed using GNU Octave, an open source Matlab alternative freely available on Linux. It is also used for graph plotting, data preprocessing, and equation optimization.

b) The proposed BbNN software model is developed in C/C++ and modeled using the proposed array interconnect algorithm. It is compiled with the GCC compiler under Ubuntu Linux, with all compiler optimizations turned on for maximum performance (optimization level 3).

c) This work utilizes GAlib, a powerful C/C++ open source library for applying GA optimization in software [22]. The optimization algorithm applied is scoped to a multiple population version of steady state GA, which is better suited for multi-objective problems.

d) Parallel processing for BbNN simulation and training is achieved using a computer equipped with a 2.8 Ghz Intel Core i7 processor. For performing multithreaded execution, the libpthread library is used.

e) Verilog and SystemVerilog HDL is used to model the hardware design of the BbNN. Hardware prototyping and implementation of the BbNN system as an SoC is done on an Altera Stratix III FPGA as shown in Fig. 1.4. The Nios II processor used is clocked at 266 MHz, and provides a platform in which the Nios2-Linux operating system can execute. This allows the use of the GAlib library, filesystem support, and USB host support (through libUSB) for embedded systems. It also allows the usage of external USB-based sensors.

f) The neuron blocks are verified in Icarus Verilog and Modelsim using SystemVerilog testbenches. The DPI-C interface in Modelsim is used for more advanced testbenches to incorporate co-verification with C/C++ golden reference models. The BbNN structure is constructed by combining these neuron blocks to form an array.

g) The BbNN structure is modeled in such a way that the rows and columns are parameterizable, by using the proposed array interconnect algorithm in conjunction with the Verilog generate command. SystemVerilog is used for the top-level BbNN structure because of the better support for multi-dimensional arrays for signals and registers.

h) The entire BbNN hardware structure is verified using co-simulation with C/C++ due to the complexity of the design. Verilator is used for this purpose.
The case studies used to verify and analyze the performance of the proposed BbNN model are limited to the following problems:

i) The XOR classification problem.

ii) Driver drowsiness detection based on HRV.

iii) Heart arrhythmia classification from ECG signals.

iv) Grammar inference of the Tomita language.

Figure 1.4: Layers of the proposed embedded BbNN SoC.

1.5 Contributions

The proposed BbNN model in this thesis has an improved architecture over existing work. A platform is developed for the simulation, verification, and implementation of the proposed BbNN model. In summary, the main contributions of this thesis are:

- Based on all known previous works, this work is among the first successful attempts at training a BbNN in recurrent mode, hence demonstrating the ability to evolve recurrent structures through feedback signals with the help of latency optimization. The recurrent mode BbNN is applied in a test case study on grammar inference using randomly generated datasets from the Tomita language [23–25].

- This thesis is also among the first work in the field to describe and optimize the latency of evolvable BbNNs using multi-objective genetic algorithm (GA).
during the training process. This is done by introducing the latency value as a gene in the BbNN chromosome, and is simultaneously optimized during the training process. A suitable fitness function for the GA is proposed for achieving this.

- This work proposes an effective hardware implementation platform for BbNN with on-chip training. The performance of the hardware implementation allows real-time classification.

- A novel multithreaded solution is proposed for accelerating the training of BbNN simulation models, which are repetitively evaluated by the GA fitness function. Significant reduction in simulation time is obtained when compared to using a only a single thread.

- An equation describing the optimum range for the upper/lower boundaries of the internal BbNN parameters is proposed. This equation was obtained through geometric analysis, and is empirically proven. Using this equation, it is possible to select an optimum range for these parameters that is suitable for resource constrained hardware implementation platforms.

- This thesis also presents the RTL design of a neuron block with properly described methodology, using a single multiplier for each neuron block. A novel method of reusing the multiplier to smoothly approximate a hyperbolic tangent (\( \tanh \)) function to be used as the activation function for the neuron blocks is presented. This is an important contribution, because a sigmoid-like activation function (which provides faster learning rates [26,27]) is provided at almost zero cost.

- This thesis also provides a parameterizable BbNN array interconnect algorithm that works for software simulation models as well as hardware implementation models. Without this algorithm, designing a BbNN array will pose an obstacle due to the complexity of the neuron block interconnects, especially when the size of the array needs to be changed during the experiments.

1.6 Dissertation Organization

The thesis is organized as follows.

Chapter 2 covers literature review and discusses previous work done, including works on the case studies used in this thesis. It also covers all related background
Chapter 3 covers the methodology for the work done in this thesis. This also includes the general approach taken for the research done in this work, as well as the tools and platform used. It also includes a section describing the case studies used and the methodology for creating the datasets.

Chapter 4 presents the development of the models, algorithms, system latency and design considerations for the proposed BbNN model. The architecture of a parameterizable multithreaded simulation model is discussed. The application of GA for performing multi-objective optimization in the training of the proposed BbNN is also presented.

Chapter 5 provides a complete description on the RTL design used for the implementation of the proposed BbNN system in hardware, and an overview of the hardware system architecture. Hardware related design considerations are discussed here.

Chapter 6 presents the results and analysis of all the experimentation done in this thesis, including the geometric analysis for the synaptic weight boundaries of the neuron blocks, the results of the four different case studies used, the hardware verification results, and the performance analysis of all proposed BbNN models.

Chapter 7 summarizes the thesis, re-stating the contributions, and suggest directions for future research.
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APPENDIX A

PUBLICATIONS

This appendix shows the papers written based on the results obtained from the work done in this thesis. It also includes papers that are related to the work done in thesis, such as SoC design, GA-based hardware designs, embedded hardware and computing systems. The following is a summary of these papers:


