PERFORMANCE EVALUATION OF SINGLE-STAGE DIFFERENTIAL AMPLIFIER BASED ON CARBON NANOTUBE

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DEDICATION

This dissertation is dedicated to my father, who taught me that the best kind of knowledge to have is that which is learned for its own sake. It is also dedicated to my mother, who taught me that even the largest task can be accomplished if it is done one step at a time.

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ABSTRACT

The demand for power sensitive CMOS designs has grown significantly due to the fast growth of battery-operated portable applications. Design of low-power and high-performance submicron and deep submicron CMOS circuits has become a big challenge in nanoelectronics industries due to short-channel effect that occurs after scaling towards nanoscale devices. Silicon-based power transistor devices has low power consumption which allows more components per chip surface area. But silicon-based short-channel devices has generated DIBL effect, hot carriers' effect and surface scattering, results in device performance degradation. To overcome these unwanted effects, carbon nanotube-based devices has shown the potential to replace silicon-based devices by sustaining the requirements of a high-speed nano-dimensional devices because it has similar device operation with CMOS and produces lower leakage power than silicon-based devices. Differential amplifier circuit topology is applied in this research because it is a very useful operational amplifier circuit to examine the performance differences between carbon nanotube and conventional silicon when they are used as channel material by evaluating Common-Mode Rejection Ratio (CMRR) of differential amplifier. The objective of this research is to study the performance of Carbon Nanotube based differential amplifier based on CMRR and to compare the performance of Carbon Nanotube based differential amplifier with the silicon based differential amplifier. HSPICE tool is used in this research to simulate the differential amplifier circuit with current mirrors active load configuration to maintain the voltage gain for single-ended output, which is built using netlists of SPICE CNFET model and PTM model, respectively. From the research findings, the highest CMRR of CNFET-based differential amplifier with constant input DC offset voltages in differential mode and common mode is 72.68 dB. When input DC offset voltages in differential mode and common mode decreases, CNFET-based differential amplifier has achieved CMRR of 92.16 dB, which increases by 26.8% compared to that of constant input DC offset voltages. The CMRR of MOSFET-based differential amplifier (21.83 dB) is smaller than the CMRR of CNFET-based differential amplifier (132.02 dB), with a difference of 110.19 dB or 143.2% .

ABSTRAK

Permintaan terhadap reka bentuk *CMOS* yang bersensitif kuasa telah mengalami pertumbuhan yang ketara disebabkan oleh pertumbuhan aplikasi pengendalian bateri yang cepat. Reka bentuk submikron litar *CMOS* yang berkuasa rendah dan berprestasi tinggi merupakan cabaran yang besar dalam industri nanoelektronik disebabkan oleh kesan saluran pendek selepas menjadi skala nano. Peranti transistor kuasa yang diperbuat daripada silikon mempunyai penggunaan kuasa yang rendah dan membenarkan lebih banyak component dalam kawasan permukaan cip. Walau bagaimanapun, peranti transistor silikon ini telah menghasilkan banyak kesan buruk dan merendahkan prestasi peranti transistor. Bagi menyelesaikan kesan-kesan ini, tiub nano karbon berpotensi tinggi untuk menggantikan silikon bagi mengekalkan keperluan peranti skala nano kerana tiub nano karbon berfungsi serupa dengan *CMOS* dan menghasilkan kebocoran kuasa yang rendah berbanding dengan peranti silikon. Kajian ini bertujuan menilai prestasi *Common-Mode Rejection Ratio (CMRR)* daripda litar penguat kebezaan menggunakan tiub nano karbon sebagai bahan saluran dan membandingkan dengan litar penguat kebezaan menggunakan silikon sebagai bahan saluran. Alat simulasi *HSPICE* digunakan dalam kajian ini untuk menjalankan simulasi litar penguat kebezaan dengan konfigurasi litar beban aktif untuk mengekalkan keuntungan voltan tinggi kepada isyarat input pembezaan dan keluaran hujung tunggal berdasarkan model dan netlist yang berbeza untuk tiub nano karbon (*CNFET*) dan silikon (*MOSFET*). Berdasarkan carian dalam penyelidikan ini, nilai *CMRR* paling tinggi yang dicapai oleh litar penguat kebezaan *CNFET* yang mempunyai voltan DC yang tetap dalam *differential mode* dan *common mode* ialah 72.68 dB. Apabila voltan DC dalam *differential mode* dan *common mode* menigkat, litar penguat kebezaan *CNFET* mencapai *CMRR* sebanyak 92.16 dB yang memberi peingkatan sebanyak 26.8% berbanding dengan nilai *CMRR* dalam voltan DC yang tetap. Litar penguat kebezaan *MOSFET* (21.83 dB) mempunyai nilai *CMRR* yang lebih kecil daripda litar penguat kebezaan *CNFET* (132.02 dB). Perbezaan ialah 110.19 dB atau peratusan perbezaan sebanyak 143.2%.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

AC	-	Alternating Current
BJT	-	Bipolar Junction Transistor
CMOS	-	Conventional Metal Oxide Semiconductor
CMRR	-	Common-Mode Rejection Ratio
CNT	-	Carbon Nanotube
CNFET	-	Carbon Nanotube Field Effect Transistor
DC	-	Direct Current
DIBL	-	Drain Induced Barrier Lowering
DOS	-	Density of States
FET	-	Field Effect Transistor
FinFET	-	Fin Field Effect Transistor
FOM	-	Figure of Merit
GIDL	-	Gate Induced Drain Leakage
HSPICE	-	Hewlett-Simulation Program with Integrated Circuit Emphasis
ICMR	-	Input Common-Mode Range
IoT	-	Internet of Things
IRDS	-	International Roadmap for Devices and Systems
MOS	-	Metal Oxide Semiconductor
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
NEMS	-	Nano-Electro-Mechanical-Systems
PP	-	Peak-to-Peak
PSRR	-	Power Supply Rejection Ratio
SNM	-	Static Noise Margin
SPICE	-	Simulation Program with Integrated Circuit Emphasis
SWCNTs	-	Single-Walled Carbon Nanotubes
UTM	-	Universiti Teknologi Malaysia
VLSI	-	Very Large-Scale Integration

LIST OF SYMBOLS

D	-	Diameter of carbon nanotube
L	-	Length of CNFET or MOSFET
m	-	Metallic chirality of carbon nanotube
n	-	Semiconducting chirality of carbon nanotube
N	-	Number of carbon nanotube
S	-	Distance between the adjacent carbon nanotubes or pitch
r	-	Radius of carbon nanotube
W	-	Width of CNFET or MOSFET
ɑ	-	Carbon-to-carbon atom inter-atomic distance

CHAPTER 1

INTRODUCTION

1.1 Research Background

According to Moore's law, the number of transistors in an integrated circuit will double every two years [1]. This theory of technology scaling on transistors was introduced by Gordon Moore in year 1965, and this theory has become the driving force behind the semiconductor technology at Intel [1]. Technology scaling is the reduction of horizontal and vertical dimensions of the transistor chip along with the reduction of supply voltage V_{DD}, which reduces the power dissipation and overcome the oxide breakdown [2]. Threshold voltage will be reduced proportionally under this condition to balance the output of the transistor. However, narrow oxide thickness and low threshold voltage will give an increment in gate leakage and subthreshold leakage current, which causes leakage power to be the highest contributor to the chip. The continuous downscaling of the devices has reduced the number of dopants, cut down the cost of doping in CMOS devices and provide higher functional density. The major challenges nowadays for semiconductor industry at the nanoscale design is to reduce dynamic and leakage power and prolong the lifetime of the transistors [2] because both dynamic and leakage power minimization are equally important for nanoscale design. To overcome this scaling limitation, Carbon Nanotube Field Effect Transistor (CNFET) is a promising non-planar transistor to replace classical conventional Metal Oxide Semiconductor (CMOS) technology which uses Metal Oxide Semiconductor Field Effect Transistor (MOSFET).

In MOSFET, channel length has played an important role in its functioning. For long channel devices, the source and drain are linked by long channel length whereas short channel devices link the source and drain with short channel length. Short-channel MOSFET has a good processing speed and low operating potential is needed which can improve transistor density on a single chip [2]. But the influence of short channel effect and abrupt rise in subthreshold leakage current has degraded the device performance due to downscaling in dimensions of transistors to micro or

nano level [2]. Increase in leakage current has resulted in huge power dissipation due to Drain Induced Barrier Lowering (DIBL) effect. DIBL is the differences in threshold voltages when the drain current varies from 0.1 V to 1 V. It estimates the overall gate control of the device on the channel electrostatics of the device. The thickness of the oxide layer in MOS needs to be reduced to overcome DIBL effect but this will increase the leakage due to Gate Induced Drain Leakage (GIDL) [3]. To reduce the GIDL, it needs high and abrupt drain doping which helps reducing series resistance to attain high transistor drive current. Therefore, CNFET is used because carbon nanotubes allow reduction of short channel effect and as it has higher electric field density, leads to lower DIBL and off current [4].

In CNFET, it exhibits quantum mechanical process of carrier transport properties and allows ballistic transport at room temperature due to comparable sizes of medium length and mean free path of carriers, which leads to higher current densities [4]. Several desirable properties that CNTs possess include a high thermal conductivity, high electrical mobility, high electrical current capacity, high tensile strength, small size, compatibility with current semiconductor fabrication processes, and ability to be functionalized [5]. The diameter of carbon nanotube is mentioned in terms of a chirality vector [6]. The arrangement is specified in terms of an index (n, m) where m, n is the pair of integers that express its chirality vector. Chirality vectors of carbon nanotubes are inversely proportional to the threshold voltage, Vth of CNFET [7]. Nanotubes can significantly reduce the DIBL effect and subthreshold swing in silicon channel replacement while sustaining smaller channel area at higher current density due to related high field effects in carbon nanotubes. The performance of a carbon nanotubes channel is enhanced when the source or drain width is minimized rather than the channel length due to gate to source or drain parasitic fringe capacitances. CNFET utilizes semiconducting single-walled carbon nanotubes to assemble electronic devices like MOSFET [8]. Single-walled carbon nanotubes (SWCNTs) have very interesting band structures. Its electronic properties can be metallic or semiconducting, made carbon nanotubes a strong competitor to silicon-based devices [9]. It has interesting structural qualities such as no surface roughness scattering and electrostatic properties such as ballistic transport. However, the fabrication of carbon nanotubes is still a complicated process with the current technology as obstacles remain in controlling proper chirality, specific and precise

nanotube separation, and surface state control [9]. So, SPICE simulation for carbon nanotubes device is focused on this research.

In this research, the comparative performance analysis between MOSFET and CNFET using single-stage differential amplifier will be presented. Differential amplifier is a base component in many types of active circuits [10], and it is the foundation for most operational amplifier designs [11]. A differential amplifier amplifies the difference between two separate input voltages for basic MOS differential-pair differential amplifier, it uses a pair of MOSFET to amplify the difference in voltage between gate-to-source voltages of both transistors. Current mirror is used to maintain the gain of the differential amplifier with two differential input voltages. For CNFET-based differential amplifier, specific device parameters such as number of nanotubes (N), inter nanotube spacing pitch (S), diameter of CNTs (D), and input supply voltage (V) are adjusted to give different threshold voltages [6].

1.2 Problem Statement

Over the past few years, researchers have encountered problems in present silicon-based transistors after further scaling down the device. The problems are related to fabrication technology and device performance with the shrinking down in the device dimension to meet the nanoscale design requirement. Limitations in fabrication such as electron tunnelling through short channel effect and thin insulator films, and device performance degradation due to associated leakage currents, passive power dissipation, device structure mismatching, mobility degradation and random doping fluctuation.

MOSFET was introduced to be used as power transistor device in VLSI circuit after BJT has found to have static power dissipation. MOSFET has lower power consumption to allow more components per chip surface area. However, MOSFET-based short channel devices has some restrictions such as DIBL effect, surface scattering and hot carrier effect, which resulting in device degradation.

To overcome these drawbacks, carbon nanotube-based devices has shown the potential to sustain the requirements of a high-speed nano dimensional device in the future because it has similar device operation with CMOS and can produce lower

leakage power with continued device downscaling to sustain the continuity of the nanoelectronics VLSI manufacturing technology progress as compared to silicon-based devices.

Carbon nanotube is one of the suggested materials to replace silicon as outlined in International Roadmap for Devices and Systems (IRDS). The dimensions of carbon nanotube are very sensitive to its electrical performance. Therefore, it is necessary to study the effect of its dimensions for the application of differential amplifier The performance of differential amplifier particularly based on Common-Mode Rejection Ratio (CMRR) when the channel material is replaced with carbon nanotubes will be studied in this research.

1.3 Research Objectives

Existing works have studied on the performance of Carbon Nanotube based Differential Amplifier. However, the works only focused on fixed dimensions of carbon nanotube. It is necessary to investigate the effect of various dimensions of carbon nanotube on the performance of differential amplifier. Therefore, it will be studied in this research. The objectives of the research are:

(a) To study the performance of Carbon Nanotube based Differential Amplifier based on Common-Mode Rejection Ratio (CMRR).

(b) To compare the performance of Carbon Nanotube based Differential Amplifier with conventional silicon material.

1.4 Research Scopes

The following are the scopes for this research:

(a) The circuit design and simulation will be using HSPICE tool.

(b) The 32 nm CNT SPICE model used is adopted from Stanford CNT SPICE model [12].

(c) The comparison using the conventional silicon material with 32 nm technology node is adopted from PTM model [13].

(d) The performance of the differential amplifier focuses on the Differential mode gain (A_{dm}), Common mode gain (A_{cm}) and Common-Mode Rejection Ratio (CMRR).

(e) The channel length of the CNFET and MOSFET is 32 nm.

(f) The radius of carbon nanotube will be varied from 0.5 nm to 1.5 nm.

(g) The pitch of carbon nanotube will be varied from 16 nm to 20 nm.

(h) The number of channels in CNFET is 1, 2 and 3.

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