MODELLING AND SIMULATION OF HETEROMATERIAL DUAL-GATE DOPINGLESS TFET (HTDGDL-TFET) AND ITS APPLICATION AS DIGITAL INVERTER

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DEDICATION

To my beloved father, mother, and family.

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ABSTRACT

Tunnel Field -Effect Transistor (TFET) has been known as one of the promising devices which will be replacing Conventional Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) as a future low-power and high-speed logic application. This is because as the size of MOSFET reduce decade by decade, to achieve better speed and lower power, and currently moving towards the nanometer regime, has leads to the limitation of the performance of MOSFET. These few bottlenecks such as increasing of leakage current, Short Channel Effects (SCEs) and complexity in device fabrication have been faced while scaling down the size of MOSFET. Therefore, TFET which work on principle of tunnelling phenomenon has been proposed as one of the devices to replace MOSFET which work on the principle of thermionic emission that limits the device's sub-threshold swing to 60mV/decade. TFET has various of features such as immunity from most of the Short Channel Effects, lower leakage current, lower sub-threshold swing which is below 60mV/dec, lower threshold voltage and higher OFF current over ON current ratio. However, there are also some drawbacks for TFET such as complexity of fabrication process in doped TFET which cause various defects. These can be overcome by using dopingless technique. This technique helps in producing defects-less and more economical devices. Another drawback would be TFET exhibits lower ON state current. Heteromaterial TFET can be used to solve the low Ion issue. To have a better controllability of heteromaterial TFET channel, dual gate is proposed. Sub-threshold swing (SS) is one of the important parameters to determine a device performance. By lowering the SS, the device performance will be better in term of lower leakage current, better Ion/Ioff ratio and lesser energy. There are 3 objectives for this project: To model and simulate Heteromaterial Dual-gate Dopingless TFET (HTDGDL-TFET). To compare the performance of TFET between Ge, Si and GaAs as Source region material. To apply the HTDGDL-TFET as a Digital Inverter. This project will be simulated using Silvaco TCAD tool. Single-Gate and Double-Gate HTDL-TFET has been successfully modelled. 4 simulation test cases have been done for this project to select the best structure of proposed TFET. Several important parameters such as Vth, SS, Ion, Ioff and Ion/Ioff ratio are used to measure the performance of TFET. Among all of the 4 test cases, the best TFET structure is with Ge as source region material, source and drain region carrier concentration of $1 \times 10^{19}\ cm^{-3}$ and channel carrier concentration of $1 \times 10^{17}\ cm^{-3}$ and dopingless. This is because the device shows Vth value of 0.97V, SS value of 15mV/dec, and Ion/Ioff ratio of 7×10^{11}. The propagation delay for designed TFET inverter is 75 times shorter than the inverter from [21] and is 29 times shorter than the market inverter [SN74AUC1G14DBVR]. Some future works also have been suggested in this thesis.

ABSTRAK

Transistor Kesan Medan Terowong (TFET) telah dikenali sebagai salah satu peranti menjanjikan yang akan menggantikan Transistor Kesan Medan Semikonduktor Oksida Logam Konvensional (MOSFET) sebagai aplikasi logik berkuasa rendah dan berkelajuan tinggi pada masa hadapan. Ini kerana apabila saiz MOSFET mengurangkan dekad demi dekad, untuk mencapai kelajuan yang lebih baik dan kuasa yang lebih rendah, dan kini bergerak ke arah rejim nanometer, telah membawa kepada pengehadan prestasi MOSFET. Beberapa kesesakan ini seperti peningkatan arus kebocoran, Kesan Saluran Pendek (SCE) dan kerumitan dalam fabrikasi peranti telah dihadapi sambil mengecilkan saiz MOSFET. Oleh itu, TFET yang berfungsi pada prinsip fenomena terowong telah dicadangkan sebagai salah satu peranti untuk menggantikan MOSFET yang berfungsi berdasarkan prinsip pelepasan termionik yang akan mengehadkan sub-ambang buai peranti kepada 60mV/dekad. TFET mempunyai pelbagai ciri seperti imuniti daripada kebanyakan Kesan Saluran Pendek, arus bocor yang lebih rendah, sub-ambang buai yang lebih rendah iaitu di bawah 60mV/dis, voltan ambang yang lebih rendah dan arus OFF yang lebih tinggi berbanding nisbah arus ON. Namun begitu, terdapat juga beberapa kelemahan bagi TFET seperti kerumitan proses fabrikasi dalam TFET doped yang menyebabkan pelbagai kecacatan, ini boleh diatasi dengan menggunakan teknik tanpa doping. Teknik ini membantu dalam menghasilkan peranti yang kurang kecacatan dan lebih menjimatkan. Kelemahan lain ialah TFET mempunyai arus keadaan ON yang lebih rendah. TFET Heteromaterial boleh digunakan untuk menyelesaikan isu Ion rendah. Untuk mempunyai kebolehkawalan saluran TFET heteromaterial yang lebih baik, dwi gerbang dicadangkan. Sub-ambang buai (SS) ialah salah satu parameter penting untuk menentukan prestasi peranti. Dengan menurunkan SS, prestasi peranti akan menjadi lebih baik dari segi arus bocor yang lebih rendah, nisbah Ion/Ioff yang lebih baik dan tenaga yang lebih rendah. Terdapat 3 objektif untuk projek ini: Untuk memodelkan dan mensimulasikan TFET Heteromaterial Dual-pintu Tanpa Doping (HTDGDL-TFET). Untuk membandingkan prestasi TFET antara Ge, Si dan GaAs sebagai bahan rantau Sumber. Untuk menggunakan HTDGDL-TFET sebagai Penyongsang Digital. Projek ini akan disimulasikan menggunakan alat Silvaco TCAD. Satu-Pintu dan Dual-Pintu HTDL-TFET telah berjaya dimodelkan. 4 kes ujian simulasi telah dilakukan untuk projek ini untuk memilih struktur terbaik TFET yang dicadangkan. Beberapa parameter penting seperti nisbah Vth, SS, Ion, Ioff dan Ion/Ioff digunakan untuk mengukur prestasi TFET. Di antara kesemua 4 kes ujian, struktur TFET terbaik ialah dengan Ge sebagai bahan kawasan sumber, kepekatan pembawa kawasan sumber dan longkang sebanyak $1 \times 10^{19}\ cm^{-3}$ dan kepekatan pembawa saluran $1 \times 10^{17}\ cm^{-3}$ dan tanpa doping. Ini kerana peranti menunjukkan nilai Vth 0.97V, nilai SS 15mV/dec, dan nisbah Ion/Ioff 7×10^{11}. Kelewatan perambatan untuk penyongsang TFET yang direka adalah 83.8ps iaitu kira-kira 75 kali lebih pantas daripada penyongsang dari [21] dan 29 kali lebih pantas daripada penyongsang pasaran [SN74AUC1G14DBVR]. Beberapa karya akan datang juga telah dicadangkan dalam tesis ini.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

TCAD	-	Technology Computer-Aided Design
SS	-	Sub-threshold Swing
MOSFET	-	Metal Oxide Semiconductor Field-Effect Transistor
TFET	-	Tunnel Field-Effect Transistor
IC	-	Integrated Circuit
SCE	-	Short Channel Effects
UTM	-	Universiti Teknologi Malaysia
RDF	-	Random Dopant Fluctuation
2D	-	Two Dimensional
3D	-	Three Dimensional
BTBT	-	Band-to-band Tunneling
SG-TFET	-	Single Gate TFET
DG-TFET	-	Double Gate TFET

LIST OF SYMBOLS

ϕ_B	-	Schottky barrier height
N	-	Surface doping concentration
ε_s	-	Dielectric constant
m	-	Electron mass
H	-	Planck’s constant
$\emptyset$	-	Metal workfunction
ΔV	-	Change of voltage

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

1.1 Problem Background

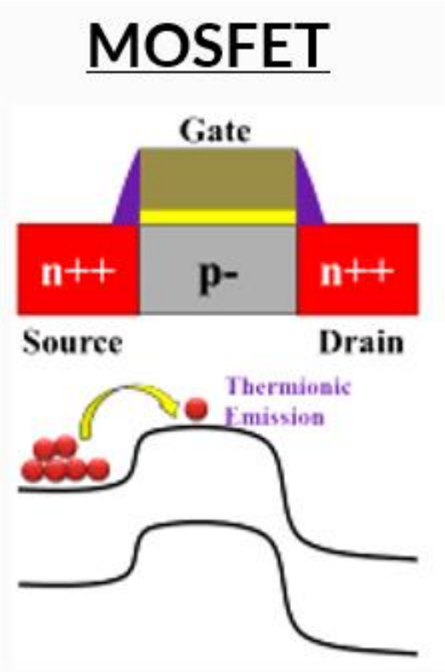
Since 1960s, Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) has been widely used as a low power and high-speed logic application. Size of MOSFET also has been minimizing over half decade of century in the past and currently moving towards to nanometer regime. The continuous size reduction of MOSFET has helped in building faster IC which consumed lower power as compared to larger size MOSFET.

In nanometer regime, besides the bright side which MOSFET able to include large amount of functionality in Integrated Circuit [IC], it also leads to several downside. Due to the continuous reduction of MOSFET size until nanometer, it leads to limitation of the performance of MOSFET and faces several bottlenecks. Increasing of leakage current is one of the bottlenecks that have been faced in reduction of MOSFET size. Various Short Channel Effects (SCE) and complexity of device fabrication process has become more obvious when MOSFET come to nanometer size. Besides that, the power dissipation has also been increasing when scaling down the size of MOSFET.

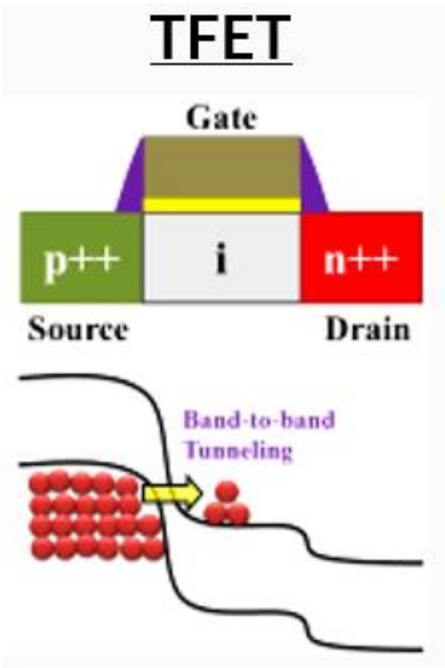
Tunnel Field-Effect Transistor (TFET) which works on principle of tunneling phenomenon has been proposed as one of the devices to replace MOSFET which work on principle of the thermionic emission. This is because TFET has numerous features or advantages that can overcome the bottlenecks that are faced in MOSFET. For example, TFET has immunity from SCEs, have low leakage current, low threshold voltage, low Sub-threshold Swing (SS) that is below 60mV/dec and it also have high

ON current over OFF current ratio $\left(\frac{I_{on}}{I_{off}}\right)$. Besides the advantages of TFET, there are also some drawbacks for TFET such as fabrication process is complex in doped TFET which will cause various defects, and it also have low ON state current.

Figure 1.1 shows the structure of MOSFET and TFET and each of their corresponding energy band diagram. By comparing the structure of MOSFET and TFET, MOSFET is N-type – P-type – N-type (N-P-N) whereas TFET is P-type – Intrinsic – N-type (P-I-N). Then from energy band diagram, MOSFET is using Thermionic Emission principle whereas TFET is using Band-to-Band Tunneling principle.



(a)



(b)

Figure 1.1 Structure and energy band diagram of (a) MOSFET (b) TFET [28]

Sub-threshold Swing (SS) is one of the important parameters to determine the performance of an FET. A low Sub-threshold Swing value indicates the device having low leakage current, better $\frac{I_{on}}{I_{off}}$, and have lesser energy. Therefore, it is important to characterize the SS properties of a device.

1.2 Problem Statement

As mentioned in previous chapter “Problem Background”, there are some drawbacks of TFET. One of the drawbacks of TFET is the complexity of fabrication process in doped TFET. This leads to various defects to occur in the device and also will cause the cost of the device to increase. This drawback can be overcome by using dopingless technique. This technique has a simpler fabrication process which can help in producing more economical and defect-less devices. Besides that, another drawback of TFET is low ON state current. This issue can be solved by using heteromaterial TFET.

Another problem statement is, according to [9], material used in heteromaterial TFET will affect the performance of TFET. With smaller bandgap material in source region, the Band-to-Band Tunnelling efficiency will be higher, which will help to improve the performance of TFET.

In addition, most of the studies in TFET are only on device level and it is rarely on circuit / logic level. Therefore, this cause the circuit performance of TFET hard to be analyzed.

1.3 Research Objectives

The objectives of the research are:

(a) To model and simulate Heteromaterial Dual-gate Dopingless TFET (HTDGDL-TFET) in TCAD simulation tool.

(b) To compare the performance of TFET between Ge, Si and GaAs as Source region material.

(c) To apply the HTDGDL-TFET as a digital inverter.

1.4 Motivation

Most of the studies which related to TFET are only in one aspect for example either in dopingless TFET, or Dual-gate TFET. Rarely the studies are in Heteromaterial Dual-gate Dopingless TFET. Besides, by comparing different source region material in TFET, the effect of the performance of TFET due to will be affected by the different material can be determined. Last but not least, circuit performance of TFET is hard to be analyzed if it is only on logic level. So, the proposed design will be applied as a Digital Inverter to analyze its circuit performance.

1.5 Research Scopes

Study of Tunnel Field Effect Transistor includes a very huge field of study. There are many types of TFET such as Vertical TFET, Feedback TFET, Heterojunction TFET, Dopingless TFET, Junctionless TFET and so on. Nevertheless, this project will only be focus on Heteromaterial Dual-Gate Dopingless TFET.

Below are the scopes for this project:

1. This project will focus on modelling and simulating Heteromaterial Dual-gate Dopingless TFET (HTDGDL-TFET).
2. Germanium, Ge, Silicon, Si and Gallium Arsenide, GaAs will be used and compare as material in source region.
3. Parameters which will be compared are Threshold voltage (V_{th}), Sub-threshold Swing (SS), On state Current (I_{on}), Off state Current (I_{off}) and I_{on} over I_{off} ratio.
4. The proposed structure is applied as a digital inverter and its circuit performance which are propagation delay (t_p), t_{pHL}, t_{pLH} are analysed.
5. This project will be modelled and simulated using Silvaco TCAD Tool.

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