# HIGH-SPEED ROBERT'S CROSS EDGE DETECTOR USING RESIDUE NUMBER SYSTEM

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## DEDICATION

This thesis is dedicated to my father, who taught me that the best kind of knowledge to have is that which is learned for its own sake. It is also dedicated to my mother, who taught me that even the largest task can be accomplished if it is done one step at a time.

**ACKNOWLEDGEMENT**

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**ABSTRACT**

Digital image processing is one of the high demands in the market that is targeted from a variety of fields. This demand has arisen because of the introduction of applications for editing and capturing images in the market. In image processing, the Robert's Cross Detector (RCD) is a detector that conducts median reordering, picture smoothing, and quick 2-D convolution on an image to discover edge pixels. This approach is based on noise reduction and gradient-based edge detection algorithms. RCD is designed to avoid creating statistics that are artificial while highlighting changes in intensity that occur in a diagonal direction. When it comes to speed, power consumption, and throughput rate application, having a mathematical arithmetic process with a high throughput is always one of the most important factors to attain. Positional number system requires large bit width to process the data which slows down the computation and becomes the major issue while processing the edge detection. On the other hand, the complexity of this implementation's design and the amount of computing it requires make it expensive to implement. Therefore, Residue Number System (RNS) architecture is implemented to replace normal PNS architecture. The RNS represents binary numbers using a set of residue numbers. Each modulus in the moduli set transforms enormous numbers into a collection of small residue numbers without requiring the full propagation chain length of adders and multipliers. Due to the carry free characteristic of residue numbers, the calculation on the set of residue numbers can be performed in parallel. As a result, RNS outperforms conventional positional number systems in mathematical computations. This study aims to create an RNS-based RCD with a high computing speed and throughput for processing picture data. In Gaussian filter and Robert Cross Operator (RCO) functional blocks, arithmetic units are implemented in Positional Number System and Residue Number System. Those units are replaced with smaller bit width of modulo adder and multiplier in residue number system. Simulation is carried out in Quartus Prime 21.1 and compiled in Synopsys Design Compiler. The Signal Noise Ratio, Peak Signal Noise Ratio, and absolute percentage error show better results in the RNS-based Gaussian Filter functional block. The results are similar for both the PNS and RNS-based RCO functional blocks. From the result of Synopsys Design Compiler, the operating frequency and throughput of RNS-based RCD are 282MHz and 3384MHz, whereas for PNS-based RCD, they are 151MHz and 2416MHz. The area of the RNS-based RCD and PNS-based RCD is 1187212.12um and 1143353.53um, respectively. For power analysis, RNS-based RCD consumed more power, which is 299.138mW, whereas PNS-based RCD consumed 290.646mW. In conclusion, the RNS-based RCD outperforms the PNS-based RCD by 86.75% and 40.10% from the speed perspective, but it traded off and required higher area and power, with a percentage of 3.83% and 2.92%, respectively.

# ABSTRAK

Dengan pengenalan aplikasi penyuntingan dan penangkapan imej di pasaran, pemprosesan imej digital merupakan salah satu permintaan tinggi dalam pasaran yang disasarkan daripada pelbagai bidang. Pengesan Roberts Cross (RCD) adalah ialah pengesan yang terdiri daripada pengurangan hingar dan pendekatan algoritma pengesanan tepi berasaskan kecerunan yang melakukan penyusunan semula median, pelicinan imej dan lilitan 2-D pantas pada imej untuk menemui piksel tepi dalam pemprosesan imej. RCD mengelakkan menjana data yang tidak realistik sambil menekankan perubahan keamatan dalam arah pepenjuru. Proses aritmetik matematik pantas sentiasa menjadi faktor utama untuk dicapai dari segi kelajuan, penggunaan kuasa. pelaksanaan ini adalah mahal yang berkadar dengan kerumitan reka bentuk dan pengiraannya. Oleh itu, pengubahsuaian menggunakan Residue Sistem Nombor (RNS) dalam menggantikan seni bina sistem nombor kedudukan biasa (PNS) dalam projek ini. RNS menggunakan set nombor sisa untuk mewakili nombor binari. Pada asasnya, setiap modulus dalam set moduli menukar nombor yang besar menjadi koleksi nombor yang kecil tanpa memerlukan panjang rantai penyebaran bawaan penambah dan pengganda. Pengiraan pada set nombor baki boleh dilakukan secara selari. Akibatnya, RNS lebih baik daripada PNS dengan kelajuan pengiraan yang tinggi dalam pengiraan matematik. Dalam projek ini, RCD berasaskan RNS menyasarkan kelajuan pengiraan tinggi dan daya pemprosesan semasa memproses data imej. Unit aritmetik dalam penapis Gaussian dan blok berfungsi Robert Cross Operator (RCO) dilaksanakan ke dalam kedua-dua PNS dan RNS. Nisbah Bunyi Isyarat, Nisbah Bunyi Isyarat Puncak dan ralat peratusan mutlak menunjukkan lebih baik dalam blok berfungsi Penapis Gaussian berasaskan RNS. Hasilnya adalah serupa untuk blok berfungsi RCO berasaskan PNS dan RNS. Daripada Synopsys Design Compiler, kekerapan operasi dan daya pemprosesan RCD berasaskan RNS ialah 282MHz dan 3384MHz manakala untuk RCD berasaskan PNS, ia adalah 151MHz dan 2416MHz. Keluasan RCD berasaskan RNS dan RCD berasaskan PNS masing-masing ialah 1187212.12um dan 1143353.53um. Untuk analisis kuasa, RCD berasaskan RNS menggunakan kuasa yang lebih tinggi iaitu 299.138mW manakala RCD berasaskan PNS menggunakan 290.646mW. Kesimpulannya, RCD berasaskan RNS mengatasi RCD berasaskan PNS sebanyak 86.75% dan 40.10% untuk perspektif kelajuan tetapi reka bentuk ini memerlukan kawasan dan kuasa yang lebih tinggi, dengan peratusan masing-masing 3.83% dan 2.92%.

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## LIST OF ABBREVIATIONS

| | | |
|---|---|---|
| RCO | - | Roberts Cross Operator |
| RCD | - | Roberts Cross Detector |
| PNS | - | Positional Number System |
| BNS | - | Binary Number System |
| RNS | - | Residue Number System |
| MAC | - | Multiply Accumulate Unit |
| PPA | - | Power, Performance, and Area |
| HDL | - | Hardware Description Language |
| LUT | - | Look-up tables |
| CRT | - | Chinese Remainder Theorem |
| MRC | - | Mixed-Radix Conversion |
| DA | - | Distributed Arithmetic |
| DSP | - | Digital Signal Process |
| TVL | - | Ternary Value Logic |
| LOG | - | Laplacian of Gaussian |
| CORDIC | - | Coordinate Rotation Digital Computer |
| RAM | - | Random Access Memory |
| BRAM | - | Block RAM |
| SNR | - | Signal Noise Ratio |
| PSNR | - | Peak Signal Noise Ratio |
| gcd | - | Greatest Common Divisor |

## LIST OF SYMBOLS

| | | |
|---|---|---|
| µ | - | Micro |
| P | - | Pixel |
| K | - | Kernel |
| I | - | Input Pixel |
| f | - | function |

## LIST OF APPENDICES

# CHAPTER 1

# INTRODUCTION

## 1.1 Introduction

With the introduction of image editing and capturing applications on the market, digital image processing is rapidly penetrating nearly all fields, and the demand for higher image quality has also increased. It is a classical problem in computer vision and image processing that depends on the choice of threshold which affects the outcome. Image processing is used in a variety of applications, including robot vision, tumour allocation, and human recognition as shown in Figure 1.1.

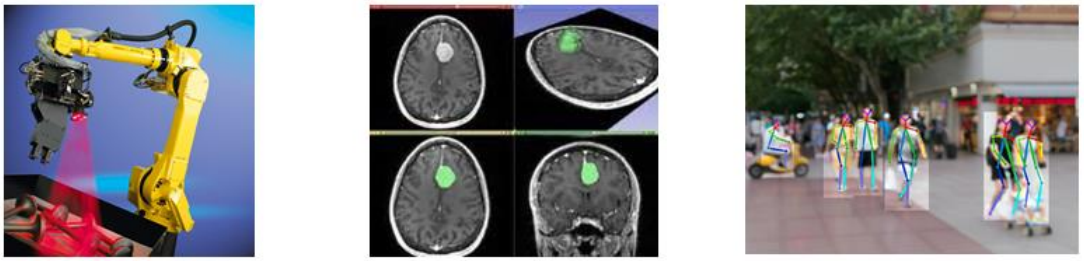

Figure 1.1 Applications of edge detection.

Edge detectors require real-time image processing and the handling of large amounts of data pixels in a short period of time. The Roberts Cross operator is the gradient-based edge detection method used to find edge pixels in an image that performs a simple, quick-to-compute, 2-D spatial gradient measurement on an image [1]. It highlights regions of high spatial frequency, which often correspond to edges. In its most common usage, the input to the operator is a grayscale image, as is the output. At each point of the output, the pixel values show how big the spatial gradient in the input image is thought to be at that point.

Residue Number System (RNS) represents a binary number using a set of residue numbers. Basically, it is converting large numbers into a set of small residue

numbers by each modulus in the moduli set, without having the carry propagation chain length of adders and multipliers especially. Due to the carry-free property of residue numbers, the calculation of the set of residue numbers can be performed in parallel. Therefore, RNS outperforms the conventional binary number system in doing mathematical calculations and is suitable for replacing the traditional arithmetic unit architecture that sacrificed speed and operating frequency. It is used extensively in many applications, like convolution and filtering.

## 1.2 Problem Background

Robert Cross Detector is introduced to CMOS technology due to its circuitry simplicity, low-area consumption, and low cost. Edge Detector relies on kernel convolution to process the data. Consequently, the arithmetic unit will have a substantial effect on RCD performance. The full adder in the design must always consider the carry bit availability of the full adder adjacent to it. In image processing, multiplication is essential due to the convolution of the kernel's requirements. Therefore, high-throughput arithmetic units are always a key element to achieving high-performance in terms of speed and throughput rate application. However, it is expensive and costly, which is proportional to its design complexity and computation. RNS functions are designed to reduce input data into smaller modules and compute fewer bits while operating in parallel to achieve high accuracy. The RNS uses a set of residue numbers to represent a binary number. Essentially, each modulus in the moduli set turns huge numbers into a collection of small residue numbers without requiring the carry propagation chain length of adders and multipliers. The calculation of the set of residue numbers can be done in parallel due to the carry-free quality of residue numbers. Therefore, the problem statements for this work are:

(a) Digital filtering and edge detecting process involve Kernel Computations which are costly in term of speed for mathematical arithmetic units using Positional Number System (PNS).

(b) PNS has propagation between arithmetic blocks during arithmetic operations. This causes speed and frequency of computation to be lower, and higher cost and area.

## 1.3 Research Objective

The ultimate aim of this work is to enhance the speed of Roberts Cross Detector by implementing Residue Number System (RNS).

The following listed the objectives of this project:

(a) To improve the performance of Robert's Cross detector using Residue Number System.

(b) To evaluate the accuracy of Residue Number System based Roberts Cross detector.

(c) To assess, analyze and benchmark the performance of Residue Number System based Robert Cross Detector with Positional Number System based Robert Cross Detector through Power, Performance and Area Analysis.

## 1.4 Scope of Work

The scope of work for this project is:

(a) Design RNS moduli set ($2^{n-1}, 2^n, 2^{n+1}$) where n equals to 4 and 6.

(b) Source 8-bits binary data of the input pixel intensity which converted from grey scale with 256 x 256 image using MATLAB.

(c) Select 180nm SilTerra library using fast database in Synopsys Design Compiler

(d) Select Peak Signal Noise Ratio (PSNR), Signal Noise Ratio (SNR) and Absolute Percentage Error to validate the accuracy of the hardware.

(e) Obtain maximum operating frequency, throughput, power consumption, gate count, energy, and area to evaluate the performance of the designs

## REFERENCES


[1] G. N. Chaple, R. D. Daruwala and M. S. Gofane, "Comparisions of Robert, Prewitt, Sobel operator based edge detection methods for real time uses on FPGA," *2015 International Conference on Technologies for Sustainable Development (ICTSD)*, 2015, pp. 1-4, doi: 10.1109/ICTSD.2015.7095920.

[2] S. Sheikh, B. Suthar, Tamanna and M. Uddin, "Comparative study of noise and digital filters for image processing," *2017 International Conference on Innovations in Control, Communication and Information Systems (ICICCI)*, 2017, pp. 1-6, doi: 10.1109/ICICCIS.2017.8660897.

[3] D. Poobathy, "An Analysis on Edge Detection Algorithms based on Processing Time," vol. 2, pp. 129–132, 2017.

[4] R. M. Yousaf, H. A. Habib, H. Dawood and S. Shafiq, "A Comparative Study of Various Edge Detection Methods," *2018 14th International Conference on Computational Intelligence and Security (CIS)*, 2018, pp. 96-99, doi: 10.1109/CIS2018.2018.00029

[5] Y. Lee, K. -K. Kim, Y. -B. Kim and M. Choi, "Stochastic Edge Detection for Fine-Grained Progressive Precision," *2021 18th International SoC Design Conference (ISOCC)*, 2021, pp. 119-120, doi: 10.1109/ISOCC53507.2021.9614036.

[6] S. R. Faraji and K. Bazargan, "Hybrid Binary-Unary Hardware Accelerator," in IEEE Transactions on Computers, vol. 69, no. 9, pp. 1308-1319, 1 Sept. 2020, doi: 10.1109/TC.2020.2971596.

[7] A. Sharma, R. Dronawat and A. Jhapate, "Automatic Diabetic Retinopathy Detection using Roberts Cross Edge Detection in DIP," *2021 10th IEEE International Conference on Communication Systems and Network Technologies (CSNT)*, 2021, pp. 363-368, doi: 10.1109/CSNT51715.2021.9509675.

[8] J. Dong, C. Tian and Y. Xu, "Face liveness detection using color gradient features," *2017 International Conference on Security, Pattern Analysis, and Cybernetics (SPAC)*, 2017, pp. 377-382, doi: 10.1109/SPAC.2017.8304308

[9] Q. Liu, Y. Huang, S. Goto and T. Ikenaga, "Aliasing Error Reduction Based Fast VBSME Algorithm," *2008 Congress on Image and Signal Processing*, 2008, pp. 85-89, doi: 10.1109/CISP.2008.337

[10] U. N. Thakur *et al*., "FPGA based effecient architecture for conversion of binay to residue number system," *2017 8th IEEE Annual Information Technology, Electronics and Mobile Communication Conference (IEMCON)*, 2017, pp. 700-704, doi: 10.1109/IEMCON.2017.8117238.

[11] N Vivek , K Anusudha, "Design of RNS Based Addition Subtraction and Multiplication Units", International Journal of Engineering Trends and Technology (IJETT) – Volume 10 Number 12 - Apr 2014

[12] S. A. Jothi, N. S. Kumari and M. R. K. Raja, "Residue number system in the VLSI architecture for image processing algorithms — A review," 2015 Online International Conference on Green Engineering and Technologies (IC-GET), 2015, pp. 1-5, doi: 10.1109/GET.2015.7453809.

[13] M. V. N. M. Latha, R. R. Rachh and P. V. Ananda Mohan, "An efficient residue-to-binary converter for the moduli set {2n−1−1, 2n+k, 2n−1}," 2017 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia), 2017, pp. 9-12, doi: 10.1109/PRIMEASIA.2017.8280351.

[14] E. Vassalos and D. Bakalis, "Residue-to-Binary Converter for the New RNS Moduli Set {22n−2, 2n−1, 2n+1} ," 2019 Panhellenic Conference on Electronics & Telecommunications (PACET), 2019, pp. 1-4, doi: 10.1109/PACET48583.2019.8956249.

[15] M. Akkal, P. Siy,A new Mixed Radix Conversion algorithm MRC-II,Journal of Systems Architecture,Volume 53, Issue 9,2007,Pages 577-586,ISSN 1383-7621,https://doi.org/10.1016/j.sysarc.2006.12.006.(https://www.sciencedirect.com/science/article/pii/S1383762106001652)

[16] S. Bi and W. J. Gross, "The Mixed-Radix Chinese Remainder Theorem and Its Applications to Residue Comparison," in *IEEE Transactions on Computers*, vol. 57, no. 12, pp. 1624-1632, Dec. 2008, doi: 10.1109/TC.2008.126.

[17] Dhanabal R, Barathi V, S. K. Sahoo, N. R. Samhitha, N. A. Cherian and P. M. Jacob, "Implementation of floating point MAC using Residue Number System," *2014 International Conference on Reliability Optimization and*

*Information Technology (ICROIT)*, 2014, pp. 461-465, doi: 10.1109/ICROIT.2014.6798385.

[18] D. Younes and P. Steffan, "Efficient image processing application using residue number system," *Proceedings of the 20th International Conference Mixed Design of Integrated Circuits and Systems - MIXDES 2013*, 2013, pp. 468-472.

[19] Z. Ahmadpour and G. Jaberipur, "Up to 8k-bit Modular Montgomery Multiplication in Residue Number Systems with Fast 16-bit Residue Channels," in *IEEE Transactions on Computers*, doi: 10.1109/TC.2021.3086071.

[20] K Anitha, T S Arulananth, R Karthik, and P Bhaskara Reddy, "Design and Implementation of Modified Sequential Parallel RNS Forward Converters," vol. 12, no. 16, pp. 6159–6163, 2017.

[21] P. A. Lyakhov, M. V. Valueva, D. I. Kaplun and A. S. Voznesensky, "A New Method of Sign Detection in RNS Based on Modified Chinese Remainder Theorem," *2021 10th Mediterranean Conference on Embedded Computing (MECO)*, 2021, pp. 1-4, doi: 10.1109/MECO52532.2021.9460255.

[22] A. O. Sharoun, RESIDUE NUMBER SYSTEM, vol. 73, 2013, [Online]. Available: https://yadda.icm.edu.pl/baztech/element/bwmeta1.element.baztech-fb9b52b8-e9be-4f93-8849-4b33a40459d2/c/Sharoun.pdf

[23] A. Ghosh and A. Sinha, "FPGA Implementation of RNS Adder Based MAC Unit in Ternary Value Logic Domain for Signal Processing Algorithm and its Performance Analysis," *2018 IEEE Electron Devices Kolkata Conference (EDKCON)*, 2018, pp. 182-187, doi: 10.1109/EDKCON.2018.8770463.

[24] B. Mohindroo, A. Paliwal and K. Suneja, "FPGA based Faster Implementation of MAC Unit in Residual Number System," *2020 International Conference for Emerging Technology (INCET)*, 2020, pp. 1-4, doi: 10.1109/INCET49848.2020.9154105.

[25] D. Younes and P. Steffan, "A comparative study on different moduli sets in residue number system," IEEE international conference on computer systems and industrial inforamtics, pp. 1–6, December 2012.

[26] N. I. Chervyakov, P. A. Lyakhov, N. N. Nagornov, D. I. Kaplun, A. S. Voznesenskiy and D. V. Bogayevskiy, "Implementation of Smoothing Image

Filtering in the Residue Number System," *2019 8th Mediterranean Conference on Embedded Computing (MECO)*, 2019, pp. 1-4, doi: 10.1109/MECO.2019.8760190.

[27] V. N. Murthy and B. Kala, "Modulo 2n±1 adder/subtractors for DSP applications," 2017 International Conference on Energy, Communication, Data Analytics and Soft Computing (ICECDS), 2017, pp. 715-720, doi: 10.1109/ICECDS.2017.8389530.

[28] L. Sousa, R. Chaves, A universal architecture for designing efficient modulo 2n+1 multipliers. IEEE Trans. Circuits Syst. I 52, 1166–1178 (2005)

[29] Ananda Mohan, P.V. (2016). RNS to Binary Conversion. In: Residue Number Systems. Birkhäuser, Cham. https://doi.org/10.1007/978-3-319-41385-3_5

[30] CHOE YHOU SONG, “STOCHASTIC COMPUTING ROBERT CROSS’S DETECTOR ASIC DESIGN” 2021, University Technology Malaysia