A PARALLEL BUILT-IN SELF-TEST DESIGN FOR PHOTON COUNTING ARRAY

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DEDICATION

This thesis is dedicated to my parents, siblings, supervisor, and my friends.

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ABSTRACT

Test module's architectures and methodologies that would maximize test capability to filter out faulty chip after fabrication is highly demanded for chip cost reduction. A high-speed frequency Built-in Self-test (BIST) module is playing an increasingly large part in overall efficiency and quality of a test solution for testability (DFT). This project is proposing the design of a parallel BIST circuit for a 16x1 photon counting array using 180 nm CMOS technology to improve the fault coverage and reduce testing cost. Almost all the test modules are built into the chip, an external tester will need to provide a start signal for the BIST design to start the testing process. LFSR is used for pseudo-random pattern generator whereas MISR and SISR are used as the output compactors. The BIST design adopts signature analysis to determine faulty chip. The golden signature is produced and being stored in ROM for comparison after fabrication. BIST controller acts as a controller unit (CU) that sends the control signals to every BIST functional block in each state. The entire BIST design is then integrated into the photon counting system for validation and layout generation. This project used bottom-up approach by designing the modules of BIST blocks in SystemVerilog. Performances are then analysed and evaluated by using Synopsys Design Compiler, IC compiler and PrimeTime tools. From the finding, proposed BIST design has managed to enhance in terms of functional reliability and design controllability with the use of SystemVerilog. For test latency, chip area, maximum frequency and power consumption, the design shows great improvements by 67.67 %, 32.26 %, 15.20 % and 48.89 % respectively.

ABSTRAK

Seni bina dan metodologi modul ujian yang akan memaksimumkan keupayaan ujian untuk menapis cip yang rosak selepas fabrikasi sangat dituntut untuk mengurangkan kos cip. Modul Ujian Kendiri Terbina Dalam (BIST) yang berfrekuensi tinggi memainkan peranan yang semakin besar dalam kecekapan dan kualiti keseluruhan penyelesaian ujian untuk kebolehujian (DFT). Projek ini mencadangkan reka bentuk litar BIST selari untuk tatasusunan pengiraan foton 16x1 yang menggunakan teknologi CMOS 180 nm untuk meningkatkan liputan kerosakan dan mengurangkan kos ujian. Hampir semua modul ujian dibina ke dalam cip, penguji luaran perlu menyediakan isyarat mula untuk reka bentuk BIST memulakan proses ujian. LFSR digunakan untuk penjana corak pseudo-rawak, MISR dan SISR digunakan sebagai pemadat keluaran. Reka bentuk BIST ini menggunakan analisis tandatangan untuk menentukan cip yang rosak. Tandatangan emas dihasilkan dan disimpan dalam ROM untuk perbandingan selepas fabrikasi. Pengawal BIST bertindak sebagai unit pengawal (CU) yang menghantar isyarat kawalan ke setiap blok BIST. Keseluruhan reka bentuk BIST kemudiannya disepadukan ke dalam sistem pengiraan foton untuk pengesahan dan penjanaan susun atur VLSI. Projek ini menggunakan pendekatan bawah ke atas dengan mereka bentuk modul blok BIST dalam SystemVerilog. Prestasi kemudiannya dianalisis dan dinilai dengan menggunakan *Design Compiler, IC Compiler* dan *PrimeTime* daripada Synopsys. Hasilnya, reka bentuk BIST yang dicadangkan telah berjaya ditingkatkan dari segi kebolehpercayaan fungsi dan kebolehkawalan reka bentuk dengan penggunaan SystemVerilog. Kependaman ujian, kawasan cip, kekerapan maksimum dan penggunaan kuasa, reka bentuk menunjukkan peningkatan yang hebat masing-masing sebanyak 67.67 %, 32.26 %, 15.20 % dan 48.89 %.

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LIST OF ABBREVIATIONS

BIST	-	Built-in Self-Test
DFT	-	Design for Testability
LFSR	-	Linear Feedback Shift Register
MISR	-	Multiple Input Signature Register
SISR	-	Single Input Signature Register
SPAD	-	Single-photon Avalanche Diodes
GAPD	-	Geiger-mode Avalanche Photodiode
CMOS	-	Complementary Metal-oxide-Semiconductor
DAQ	-	Data Acquisition
VLSI	-	Very Large-scale Integration
PISO	-	Parallel-in Serial Out
KSA	-	Kogge-Stone Adder
CUT	-	Circuit-Under-Test
CU	-	Controller Unit
PRPG	-	Pseudo-random Pattern Generator
ROM	-	Read-Only Memory
BILBO	-	Built-In Logic Block Observer
ASIC	-	Application-specific Integrated Circuit
ATE	-	Automatic Test Equipment
HDL	-	Hardware Description Language
API	-	Application Programmer's Interface
VCS	-	Verilog Compiler Simulator
LVS	-	Layout Versus Schematic
DRC	-	Design Rules Check
RTL	-	Register Transfer Level
DUT	-	Design Under Test
FSM	-	Finite State Machine
STA	-	Static Timing Analysis
IP	-	Intellectual Property
FYP	-	Final Year Project

CHAPTER 1

INTRODUCTION

This chapter starts by describing the background of the proposed project design and provides an overview of the testability parallel photon counting design methodologies and techniques developed. Subsequent sections present the descriptions of the problem raised in high speed photon counting array development using deep-sub micron CMOS technology. The importance of built-in self-test module is then discussed. The objectives and project scopes are explicitly explained with targeted figure of merit performance. Finally, the last section contains a overview describing the structure of this thesis.

1.1 Problem Background

In VLSI design, it is preferable to have a quick diagnosis and have a very high fault coverage testing mechanism. Chip design is always bounded by the balance between performance and cost. It is always trivial to produce a high performance chip yet with little cost. Nothing comes for free. Chip testing efficiency and cost becomes important when a faulty chip need to be identified as early in the design cycle as possible to reduce the prototyping turns cost. This prototyping turn includes the period of redesign until refabricate. If a system or chip is designed without any test methodology being integrated, it is described as *system-foolish* or *chip-wise* [1]. The added testing cost in hardware will be balanced by the maintenance cost or prototyping turn cost. BIST design is also being claimed to have a full fault coverage at about 15% total chip area cost [2].

A large and complex VLSI design is hard to be partitioned and hence difficult to be tested. For an instance, two devices with 100 % fault coverage will lose its fault coverage when they are being cascaded together due to its untestable connection and

redundant hardware [1]. BIST also helps to improve the reject ratio of chips by introducing self-test circuitry in the chips itself and eventually improves the quality of chips. Reject ratio is defined as the fraction of faulty chips from the total of passing chips. It is commonly used for test quality measurement. Low reject ratio indicates high quality test.

High cost of external tester with many input pins promotes the implementation of BIST into the chip. According to Bushnell [1], BIST will save up to $4,800,000 for a 1 GHz system with 800 pins. This is due to the huge initial capital cost for using a high speed ATE for circuitry testing.

1.2 Problem Statement

BIST design is a resource overhead added to the chip for structural integrity check. Reducing the overhead always become a debating topic in VLSI design in order to balance up test quality and chip cost. Complex design with multiple circuitry blocks increases the challenge of chip testing. Multiple circuit-under-tests (CUTs) need to be tested parallelly to reduce the testing time. Testing time becomes critical when the total number of primary inputs (PIs) is relatively large, and more test patterns are needed to achieve good coverage.

In addition to testing time, resource utilization in chip design also needs to be planned wisely. Extra overheads can lead to higher chip cost and higher power consumption. An effective controller is needed in BIST design to ensure the test is robust enough for high coverage yet uses the reasonable numbers of resource overhead.

Pre-silicon validation is important to make sure the design functionality meets the architectural definitions. Same goes to BIST design. Pre-silicon validation needs to be carried out to ensure the design meets BIST functionality and does not miss out any faulty chip after fabrication. An unvalidated BIST design always causes uncertainty and eventually increases the reject ratio of manufacturing. Negative testing

is commonly used approach to increase the design reliability to identify fault chip during testing.

1.3 Research Objectives

The objectives of this project are:

1. To develop an efficient parallel BIST design with improve the resource utilization into DAQ system.
2. To validate the functionality of BIST design with fault injection.
3. To characterize the BIST design at different frequencies up to the maximum frequency of the CUT.

1.4 Research Scopes

The scopes of this projects are:

1. Focusing on improvement of BIST design performance. Design and performance of CUTs from [3] [4] remain unchanged but analysed due to time constraint.
2. Using Vivado HLx from Xilinx for RTL design and pre-silicon validation in SystemVerilog.
3. Using Synopsys IC Compiler for netlist and layout generation using SilTerra's 180nm CMOS process.

1.5 Thesis Outline

This project is made up of five chapters.

This chapter consists of introduction, problem background, problem statement, research objectives, and the project management.

The second chapter of this project focusses on the literature review where the relevant and significant information is gathered.

Chapter 3 highlights the project methodology used throughout the projects and the design flow chart for the tools used.

Chapter 4 focusses on the results where the performance of the BIST design is analyzed and discussed.

The last chapter, Chapter 5, summarizes and concludes the results obtained from this project. Potential future works are also being discussed in this chapter.

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