ACTIVELY QUENCHED SPAD WITH IMPROVED AMPLIFICATION USING DEEP SUBMICRON CMOS TECHNOLOGY

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DEDICATION

This thesis is dedicated to my dear parents; Muslim bin Idrus and Narizah binti Muhamad, followed by lecturers, colleagues, and my fellow course-mates; Adib Md Dan and Lim Calvin for their advice, motivation, and support during my educational journey.

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ABSTRACT

In general, a novel active quenching circuit for a single photon avalanche diode (SPAD) is invented to optimize the light detection and ranging (LiDAR) application, where the modulating performance is subject to specific demands. The LiDAR application favors the incredible and accurate frequency range and flexibility in a wide variety of terrains. The SPAD operates in Geiger mode operation whereby the presence of the photon detection is captured when excess bias voltage is operating above its breakdown voltage. In previous thesis, a passively quenched circuit (PQC) integrated with SPAD employing submicron of 130 nm complementary metal-oxide-semiconductor (CMOS) technology could only operate at a maximum frequency of 1 GHz. To address the limitations of PQC SPAD design, an actively quenched of active quenching circuit (AQC) and active recharge circuit (ARC) integrated with SPAD is proposed in this theses by improving better and excellent amplification strategy based on submicron of 130 nm and 250 nm CMOS technology. The drive of this project is to improve frequency up to 2 GHz operating at low-voltage excess biased and investigate the effects of both passively and actively quenched SPAD. To determine the power dissipation for each quenching design, the drain current is computed. The performance of the proposed solutions are characterized in terms of recovery time, t_r and quenching time, t_q through the resultant waveform of quenching pulse simulation waveforms that yields to dead time, t_d performance. In this project, the functioning of a basic PQC associated with SPAD is re-constructed first using Cadence Design System and LTSpice XVII tools. Then, followed by the development of the suggesteddesign of AQC and ARC integrated with SPAD using LTSpice XVII tool. The amplification scheme of Geiger mode for photon detection is successfully optimized by achieving maximum of 2 GHz from 0.5 GHz using LTSpic XVII tool.

ABSTRAK

Secara umum, litar pelindapkejutan aktif baru untuk diod runtuhan foton tunggal (SPAD) dicipta untuk mengoptimumkan aplikasi pengesanan dan julat cahaya (LiDAR), di mana prestasi pemodulatan tertakluk kepada permintaan khusus. Aplikasi LiDAR mengutamakan julat frekuensi yang luar biasa dan tepat serta fleksibiliti dalam pelbagai jenis rupa bumi. SPAD beroperasi dalam operasi mod Geiger di mana kehadiran pengesanan foton ditangkap apabila voltan pincang beebihan beroperasi di atas voltan pecahnya. Dalam tesis sebelumnya, litar dipadamkan pasif (PQC) yang disepadukan dengan SPAD menggunakan submikron teknologi semikonduktor logam-oksida-oksida (CMOS) pelengkap 130 nm hanya boleh beroperasi pada frekuensi maksimum 1 GHz. Untuk menangani batasan reka bentuk PQC SPAD, litar pelindapkejutan aktif (AQC) dan litar cas semula aktif (ARC) yang disepadukan secara aktif dengan SPAD dicadangkan dalam tesis ini dengan menambah baik strategi penguatan yang lebih baik dan cemerlang berdasarkan submikron 130 nm dan 250 nm teknologi CMOS. Pemacu projek ini adalah untuk meningkatkan frekuensi sehingga 2 GHz yang beroperasi pada lebihan berat sebelah voltan rendah dan menyiasat kesan kedua-dua SPAD yang dipadamkan secara pasif dan aktif. Untuk menentukan pelesapan kuasa bagi setiap reka bentuk pelindapkejutan, arus longkang dikira. Prestasi penyelesaian yang dicadangkan dicirikan dari segi masa pemulihan, t_r dan masa pelindapkejutan, t_q melalui bentuk gelombang terhasil bagi bentuk gelombang simulasi nadi pelindapkejutan yang menghasilkan masa mati, prestasi t_d. Dalam projekini, fungsi PQC asas yang dikaitkan dengan SPAD dibina semula terlebih dahulu menggunakan Sistem Reka Bentuk Cadence dan alat LTSpice XVII. Kemudian, diikuti dengan pembangunan cadangan reka bentuk AQC dan ARC yang disepadukandengan SPAD menggunakan alat LTSpice XVII. Skim penguatan mod Geiger untuk pengesanan foton berjaya dioptimumkan dengan mencapai maksimum 2GHz daripada
0.5 GHz menggunakan alat LTSpic XVII.

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LIST OF ABBREVIATIONS

SPAD	-	Single Photon Avalanche Diode
PQC	-	Passive Quenching Circuit
AQC	-	Active Quenching Circuit
ARC	-	Active Recharge Circuit
CMOS	-	Complementary Metal Oxide Semiconductor
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
PDC	-	Pulse Discriminator Circuit
EDA	-	Electronic Design Automation
TCAD	-	Technology Computer-Aided Design
ADC	-	Analogue to Digital Converter
PMT	-	Photomultiplier Tubes
RC	-	Resistor-Capacitor

LIST OF SYMBOLS

Ω	-	Ohm
V	-	Voltage
A	-	Ampere
W	-	Watts
Hz	-	Herts
t_r	-	Recovery Time
t_q	-	Quenching Time
t_d	-	Dead Time
f	-	Frequency
R_L	-	Quenching Resistor or Load Resistor
R_D	-	SPAD Resistor
R_S	-	Sensing Resistor
V_B	-	Breakdown Voltage
V_{BIAS}	-	Excess Bias Voltage
C_{AC}	-	Junction Capacitance
C_{AS}	-	Stray of Anode Capacitance
C_{CS}	-	Stray of Cathode Capacitance
I_D	-	Drain Current
P_D	-	Power Dissipation

CHAPTER 1

INTRODUCTION

1.1 Introduction

Traditionally, photomultiplier tubes (PMTs) were introduced to be compared favorably to the advanced technological implementation of Silicon Photomultipliers, SiPMs or also known as Silicon Photon Avalanche Diode (SPAD) [14]. PMT was invented over 80 years ago to serve a purpose of detecting light at the single photon level. It offers limited detection efficiency for longer wavelengths and lower frequencies [15]. In the early 2000s, the invention of SPADs have been implemented within CMOS technology. SPAD is a photodetector that has radically increased their performance featuring high internal gain and single photon sensitivity for a significant role in a variety photon counting and photon timing applications. Since, the photon sensitivity of SPAD is high, thus it is favorable in detecting light at a high detecting rate in low light environment. Since the late 1900s, these SPADs applications are increased significantly. For instance, Light Detection and Ranging (LiDAR), quantum computing, quantum cryptography, Fluorescence Lifetime Imaging Microscopy (FLIM), Time-of-Flight (ToF) 3D imaging, and Time Correlated Single Photon Counting (TCSPC) [3]. SPADs are p-n junction, where the operation of the diode is occurred when the reverse bias voltage, V_{BIAS} exceeds the breakdown voltage, V_B [16]. In this state of operation, which is called the Geiger mode, the electrical field across the p-n junctionis extremely high [3]. In order to allow the photon detection in SPAD detector, the quenching process is needed to operate below the excess avalanche breakdown current. When the avalanche current is cut off and V_{BIAS} is reset, then the photon is detected [1].

There are three types of quenching circuits: passive quenching, active quenching, and hybrid. This study will only concentrate into passive and active quenching. The previous project addressed the passive quenching SPAD. Based on previous project,

the passive quenching circuit is implemented using 130 nm and 250 nm by resulting the limitation of the performance in terms of frequency, f where it could onlyoperates at the highest frequency of 1 GHz only which is equivalent to 1 Gcps and 1ns of counting rate and dead time, t_d, respectively [10]. Based on previous passive quenching SPAD, the same design is constructed and simulated using LTSpice tool which is resulting the best frequency could reach up to 0.5 GHz equivalent to t_d of 2 ns. As a result, an active quenching SPAD is chosen for this project to overcome the performance drawbacks. Active quenching SPAD simulation model improves gain using submicron of 130 nm and 250 nm CMOS technology whenever weak photon signal is detected. In this project, the frequency is improved up to 2.0 GHz which is equivalent to 2.0 Gcps and 0.5 ns of counting rate and t_d, respectively. Moreover, the amplification of Geiger mode detection is observed for linear array design to obtain high sensitivity. The amplification scheme for photon detection is optimized from 0.5 GHz to 2.0 GHz.

1.2 Problem Statement

The association of SPAD model and active quenching is fully integrated by resulting more complex design as compared to passive quenching due to the additional components required in the design [5]. In order to detect the incoming photons, the high-speed detection rate is used in SPAD model. The limitation and extension of SPAD model is due to the leakage current [12] and high sensitivity [13], respectively. According to previous design, the implementation of SPAD with passive quenching circuit (PQC) or also known as current-mirror causing drawback of occupying on chip area consumption due to the utilization of high ohmic resistor [11]. Besides, the frequency could only reach at maximum of 1 GHz using Mentor Graphics [10]. Meanwhile, the frequency could obtain at maximum of 0.5 GHz using LTSpice. Furthermore, the PQC yields longer t_d and high power dissipation, P_D [5]. As a result, the SPAD model is ensemble with active quenching circuit (AQC) to overcome the constraints discussed. The frequency is pumped up from 0.5 GHz to 2.0 GHz alongside enhancing the counting rate. The performance of t_d and P_D are also improved. Moving on, the active quenched SPAD with improved amplification is design to achieve low voltage using submicron of 130 nm and 250 nm CMOStechnology. Hence, the suitable tool is required to fulfill the design criteria.

In previous project, the Mentor Graphics Pyxis EDA program and Sil013 standard cell library is utilized to achieve the amplification scheme. A standard cell library used in Mentor Graphics Pyxis Electronic Design Automation (EDA) softwareis sil013 refers to 0.13 μm CMOS process technology under silterra [17]. This softwarecovers the full IC design flow from apprehending through concluding layout verification and analysis. Conversely, an alternative tool that could be used in this project that refer to a standard cell library of 130 nm is Cadence Design System [22]. By following the V_{DD} used in previous project, the value is sustained at 1.2 V for bothprevious and proposed design. The Cadence Design System toolchain is used to mimica conventional 130 nm CMOS technology process [23]. However, these tools require a license, which must be purchased and used within the timeframe specified. In order to resolve the license issue, then the implementation of quenching circuits is continued with 250 nm CMOS technology using LTSpice tool. It is a free computer program that implements a LTSpice simulator for electronic circuits. As a result, the likelihood of encountering a license tool issue as compared to Mentor Graphics and Cadence tools.The LTSpice tool improves the waveform viewer to speed up the simulation of regulators. [18]. The LTSpice tool is well-known for its usage in amplification schemes for avalanche photodiodes with higher supply voltages, such as V_{DD} at 2.5 V operating at 250 nm CMOS technology [19]. The functionality of this tool is similarto Mentor Graphics and Cadence tools which is used for integrated circuit (IC) designenvironments to the most perplex VLSI designs. A standard cell library is imported into the project to import a set of components of resistor-capacitor (RC)-level, and transistor-level such as NMOS and PMOS Metal Oxide Semiconductor Field Effect Transistor (MOSFET).

1.3 Objectives

The goal of this project is to develop an actively quenched SPAD with improved amplification leveraging submicron of 130 nm and 250 nm CMOS technology. The designs are put into action using the Mentor Graphics Pyxis EDA, and Cadence Design System to simulate the constructed passive quenching SPAD circuit at 130 nm. Meanwhile, LTSpice XVII is used to simulate the passive and active quenching SPAD circuits at 250 nm. The objectives of this project are outlined below.

i. To design the association of active quenching circuit with single pixel SPAD circuit using submicron of 130 nm and 250 nm CMOS technology.
ii. To enhance the design by optimizing the amplification scheme of Geiger mode for photon detection operating at 2.0 GHz.
iii. To characterize the performance of the actively quenched SPAD array with the proposed SPAD simulation model.

1.4 Scope of Work

This project is focused on modelling active quenching circuit and active recharge integrated with single pixel SPAD circuit with necessary sizing factor. Initially, the model is designed using 130 nm CMOS process via Mentor Graphics Pyxis EDA and Cadence Design System tool. The width and length size of the transistor used is 350 nm and 130 nm, respectively to quench the SPAD model. However, since the license for both tools got suspended, then the project is continued using LTSpice XVII tool. By sustaining the width size of the transistor, the length size is tuned to minimum of 250 nm. The increment of the length size affects the transistor gates such as it will longer the delay. The design of single pixel SPAD model consist of types of quenching circuits, transistor triggering SPAD or also known as SPAD detector circuit, and two stages amplifier for pulse discriminator circuit (PDC). The sorts of quenching circuits are built using previous and proposed solutions. The earlier design had a passive quenching circuit (PQC). Meanwhile, active quenching circuits (AQC) and passive quenching with active recharging circuit or also known as active recharge circuit (ARC) in short, are used in the recommended designs.

The characterization is carried out in accordance with previous findings and the recommended project design. The outcome will then be compared in order to benchmark performance. The SPAD simulation model is increased by optimizing signal recharging and quenching before transmitting to the PDC. Eventually, the voltage gain, frequency, counting rate, and sensitivity of the design specification will be evaluated. The drain current, I_D is mathematically computed to calculate P_D by sustaining the voltage supply. Simultaneously, the timing analysis and P_D are obtained. The physical layout simulation output is compared to the reference schematic circuit to confirm that both processes provide identical results.

1.5 Thesis Outlines

This thesis offers a research study on enhancing the amplification scheme for Geiger mode operation when a weak photon signal is detected in a low voltage CMOS technology. The outline for five chapters is described briefly below.

The first chapter is an introduction. Essentially, it outlines the context and purpose of the project. Then, it discloses the objectives, pros and cons in the problem statement and scope of work of this project.

Next, the second chapter gives an overview of the theoretical literature review. This chapter discussed and tabulated a strategy for identifying and investigating prior information and knowledge relevant to this thesis. In general, the discovery of diverse performance based on different sorts of length size of transistor in CMOS technology. Additionally, the SPAD detector in CMOS technology in the needed area is explored. The passive and active quenching designs associated with SPAD model are reviewed.

Furthermore, the third chapter describes the research methodology. The employment procedures and strategies in designing previous PQC SPAD and proposed AQC and ARC SPAD are discussed here. The high-level flowchart of the workflow based on project execution is provided to convey a better explanation. Technically, it explains the design steps using Cadence and LTSpice tools. The schematic circuitry for previous and proposed designs are provided here.

In forth chapter, it refers to the data interpretation and performance analysis. The summarization of the collected data such as parameters specification for SPAD quenching circuits and its simulation results of single pixel SPAD is made. The mathematical computation and summary of the parameters reviewed are also captured here.

This project will come to a close in Chapter 5. It summarizes the study findings, discusses the project's accomplishments and limitations. Moreover, it reflects the future recommendation to enhance the performance of the project.

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