SIMULATION OF IN-MEMORY LOGIC CIRCUIT BASED ON PROBABILISTIC MEMRISTOR USING LTSPICE

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DEDICATION

This thesis is dedicated to my father, who taught me that the best kind of knowledge to have is that which is learned for its own sake. It is also dedicated to my mother, who taught me that even the largest task can be accomplished if it is done one step at a time.

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ABSTRACT

Memristors are passive components with a varying resistance that depends on the previous voltage applied across the device. However, limited endurance of memristor devices and variations (both cycle-to-cycle and device-to-device) are important parameters to be considered in the evaluation especially in memristive logic families. There are a lot of factors on memristor variability, such as the influence of temperature, influence of switching the pulse parameters, influence of the concentration of oxygen vacancies, active dielectric layer structure and thickness as well as the influence of the parameters of conducting cell electrodes. In this work, only cycle-to-cycle variation is focus on both the deterministic and probabilistic behaviour in a memristor is being simulated and compared using LTSPICE software. Knowm or Mean Metastable Switch (MMS) SPICE model is being used to present the behaviour of a memristor. Monte Carlo simulation is applied to show the probabilistic behaviour in memristor. In summary, the best practical for probabilistic memristor model is within 50% range in terms of these model parameters (VON, VOFF, RON, ROFF). Besides, the impact of variability of memristors on the performance at in-memory logic circuit using different logic design styles such as Memristor-Aided Logic (MAGIC) and Memristor Ratioed Logic (MRL) are being implemented and analysed based on a universal NOR gate. The performance analysis of implementation of both MAGIC and MRL is carried out with respect to the functionality and sensitivity after applying the fluctuation. In this work, MRL design style is more robust and less affect by the cycle-to-cycle variability.

ABSTRAK

Memristor ialah komponen pasif dengan rintangan yang berbeza-beza yang bergantung pada voltan sebelumnya yang digunakan pada peranti. Walau bagaimanapun, ketahanan terhad peranti memristor dan variasi (kedua-dua kitaran-ke kitaran dan peranti-ke-peranti) adalah parameter penting untuk dipertimbangkan dalam penilaian terutamanya dalam keluarga logik memristif. Terdapat banyak faktor pada kebolehubahan memristor, seperti pengaruh suhu, pengaruh pensuisan parameter nadi, pengaruh kepekatan kekosongan oksigen, struktur dan ketebalan lapisan dielektrik aktif serta pengaruh parameter pengalir elektrod. Dalam kerja ini, hanya variasi kitaran ke kitaran difokuskan pada kedua-dua tingkah laku deterministik dan kemungkinan dalam memristor sedang disimulasikan dan dibandingkan menggunakan LTSPICE. Model SPICE Knowm atau Mean Metastable Switch (MMS) sedang digunakan untuk mempersembahkan gelagat memristor. Simulasi Monte Carlo digunakan untuk menunjukkan tingkah laku kebarangkalian dalam memristor. Secara ringkasnya, praktikal terbaik untuk model memristor kemungkinan adalah dalam julat 10% dari segi parameter model ini (VON, VOFF, RON, ROFF). Selain itu, kesan kebolehubahan memristor terhadap prestasi pada litar logik dalam memori menggunakan gaya reka bentuk logik yang berbeza seperti MAGIC dan MRL telah diterokai dan dianalisis berdasarkan gerbang NOR universal. Analisis prestasi pelaksanaan kedua-dua MAGIC dan MRL dijalankan berkenaan dengan fungsi dan sensitiviti selepas menggunakan turun naik. Dalam kerja ini, gaya reka bentuk MRL lebih teguh dan kurang dipengaruhi oleh kebolehubahan kitaran ke kitaran.

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LIST OF ABBREVIATIONS

FYP	-	Final Year Project
MAGIC	-	Memristor-Aided Logic
MRL	-	Memristor-Ratioed Logic
C2C	-	Cycle-to-cycle
D2D	-	Device-to-device
UTM	-	Universiti Teknologi Malaysia
HRS	-	High Resistance State
LRS	-	Low Resistance State
CMOS	-	Complementary Metal-Oxide Semiconductor
IoT	-	Internet of Things
RRAM	-	Resistive Random Access Memory
VLSI	-	Very Large Scale Integration

LIST OF SYMBOLS

V	-	Voltage
q	-	Elementary Charge
k	-	Boltzmann Constant
f	-	Frequency
R	-	Resistance
τ	-	Time Constant

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CHAPTER 1

INTRODUCTION

1.1 Background

In 1965, Gordon E. Moore, the co-founder of Intel, postulated that the number of transistors on a microchip would double every two years which is referred to as Moore's Law [1]. Over the past few decades, the development of computing system has been the fastest growing technology, rely on shrinking the size of transistor to achieve more powerful device by following Moore's law. However, Moore's law might be ending since the size of transistor is reaching a physical limit. Obviously, an alternative computing approaches or new suitable devices has been explored in order to cope with the future challenges especially nowadays artificial intelligence (AI) application is in high demand which processes large amount of data. On the road towards next-generation chips, memristors, being a very promising technology that are highly scalable, reconfigurable and energy-efficient, could open up a new era in electronics.

The term memristor was described and named in 1971 by Leon Chua, completing the theory of the four basic electrical components which consists of resistor, inductor, and capacitor [2]. In other words, resistor holds the relation between current and voltage, the inductor holds the relationship between current and flux, and the capacitor holds the relation between voltage and charge, while the fourth passive device, memristor, should exist to hold the relationship between magnetic flux and charge. Hewlett Packard Laboratories (HP Lab) did the initial memristor device fabrication in 2008, which comprise of a 5nm stoichiometric TiO_2 and an oxygen-deficient TiO_{2-x} layers covered by two platinum electrodes [3]. When a voltage is applied across the memristor, the oxygen deficiencies in the TiO_{2-x} layers migrate and leads to the changes of the thickness of the oxygen deficient layer and thus, the resistance of the memristor device change. They tend to stay in the same position after

the voltage source is removed due to the oxygen vacancies have a low mobility, this best describing the term, memristor, a contraction of “memory” and “resistor”, where the value of the resistance is retained even after the removal of the acting potential. Hence, memristor is also a non-volatile memory element. This property makes it useful in many important application areas such as digital circuits, biological and neuromorphic systems, computer technology as well as digital memory, neural networks and analog electronics, programmable logic and signal processing. Other than that, memristors are proven to have low power consumption [4] , low computational complexity [5], high endurance [6], fast switching speed [7], CMOS-compatibility for edge computing in IoT [8] as well as excellent scalability [9].

However, this non-volatile memory device shows inherent stochasticity in the operation due to the intrinsic variation in switching conductance caused by the inherent material property in memristor [10]. In this case, it can be classified into cycle-to-cycle (C2C) and device-to-device (D2D) variability. C2C relates to the random physical mechanisms behind the process while D2D links to the technological differences during fabrication process. A huge industrial exploitation of memristors is likely to be hindered by these phenomena, especially when it comes to non-volatile circuits. A better insight to show this fundamental problem is through the application of memristors especially the digital in-memory logic circuit. At present, memristor-based logic circuits can be divided into stateful and non-stateful categories, an example of stateful logic families would be Memristor-Aided Logic (MAGIC) and non-stateful can be represented by Memristor-Ratioed Logic (MRL) design style. Stateful logic is defined when the memristors fulfil two functions: firstly, using resistive states, the input data can be stored during computation; secondly, their internal resistive state is taken into consideration when performing logic computations. [11]

1.2 Problem Statement

As a prospective candidate for future nonvolatile memory, memristors are extensively studied. Memristors has simple structure and great scalability, along with fast switching speed and compatible with silicon complementary metal-oxide-semiconductor (CMOS) technology to be applied for in-memory logic circuits. Some previous work proposed memristor-based logic gate is built upon deterministic model and accurate bit-stream. However, circuit design relies heavily on memristor variability, which needs to be addressed in the modeling context. The creation (set process) and destruction (reset process) of conductive filaments at atomic scale in a memristor are related with diffusion, nucleation and redox which is considered as random processes connected to physical mechanisms, thus results in the resistive switching stochasticity property in memristor device since memristors are based on resistive switching of filamentary nature. However, this project only focuses on the cycle-to-cycle variability in memristor devices which is a more intrinsic problem than the device-to-device variability, because device-to-device variability depends on the fabrication process, and better uniformity control of the processes may improve the device-to-device uniformity. The question in this research would be: How this variability can affect the performance towards different logic design styles of memristor-based logic circuit?

1.3 Research Objectives

The objectives of this project are:

1. To simulate and compare both the deterministic and probabilistic behavior in a memristor using LTSPICE.
2. To implement two memristors-based logic circuit design styles on a universal NOR gate.
3. To compare and analyze the impact of variability of memristors on the performance at in-memory logic circuit using different logic design styles.

1.4 Scope of Project

The scope of project is described as following:

- Knowm SPICE model [12] with Monte Carlo simulation to show probabilistic behavior
- Only consider cycle-to-cycle variation
- Implementation on 3 different logic design styles, such as MAGIC and MRL
- Digital logic circuit used is a NOR gate
- Performance comparison will base on the functionality and sensitivity

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