# AN EFFICIENT MARCH (5n) FSM-BASED MEMORY BUILT-IN SELF-TEST (MBIST) ARCHITECTURE WITH DIAGNOSIS CAPABILITIES

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## DEDICATION

This report is dedicated to my father, who taught me that the best kind of knowledge is learned for its own sake. It is also dedicated to my mother, who taught me that even the largest task can be accomplished if it is done one step at a time.

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**ABSTRACT**

In deep submicron Systems-on-Chip, embedded memories are consuming a growing part of the die area. The manufacturing test of embedded memory is a critical stage in the SoC production process that screens out faulty chips and speeds up the volume production of new manufacturing technology. Memory Build-In Self-Test or MBIST is a standard mechanism to test the memory arrays and potentially detect all of the faults that may be present inside memory cells using an effective collection of algorithms. However, a massive number of memory cells wrapped by BIST logic can result in substantial overhead in wiring and gate area, and also a detrimental influence on memory performance. Therefore, new MBIST designs for advanced SoCs that address the challenges must be explored to reduce the overall cost of manufacturing tests. It is important to choose the appropriate level of algorithmic coverage and diagnosis for a range of array sizes. The March 5n algorithm proven the alternative form of March-based algorithm with better test length has achieved shorter test time than conventional MATS++ algorithms without penalizing the fault coverage. This memory testing algorithm and architecture suit the needs for fast array testing to get the products to market in the quickest fashion. However, the previous work is extendable for inversion coupling fault detection and repair support. Therefore, the March 5n architecture is utilized as the foundation in this project. An improved March 5n architecture is proposed to extend its properties in terms of fault coverage and diagnosis capabilities to allow memory failure analysis. Block of March algorithms, an address generator, data generator, diagnosis module, and redundancy logic are the components of the targeted BIST architecture. Extensive circuitry from the previous architecture will be implemented to achieve the goals. The additional logic will accumulate the fault information and its corresponding diagnosis results will report during the memory testing. Synopsys Electronic Design Automation tools (VCS, Design Compiler and Verdi) are utilized in synthesising and evaluating the performance in terms of speed, area, power and fault coverage. Several reports and waveforms are generated and simulated for evaluation. The outcome of this project has demonstrated that adding more logic can enhance the capability for diagnosis and enable redundant programming to replace the defective cell. Besides, the inversion coupling fault coverage using the March 5n is verified to be functioning as intended. Speed up of the redundant memory space allocation in a repair mechanism is achieved with the proposed architecture due to the ability to keep track of each failure signature of memory when tested. In comparison to earlier work, the improved architecture has generally enhanced maximum clock speeds by almost 8% and decreased power dissipation by about 6%. However, higher speed and functionality are obtained at the cost of 4% of the area overhead.

## ABSTRAK

Dalam submicron Systems-on-Chip yang mendalam, memori tertanam memakan bahagian yang semakin meningkat dari kawasan cetakan. Ujian pembuatan memori terbenam ialah peringkat kritikal dalam proses pengeluaran SoC yang menapis cip yang rosak dan mempercepatkan volum pengeluaran teknologi pembuatan baharu. Ujian Kendiri Binaan Memori atau MBIST ialah mekanisme standard untuk menguji tatasusunan memori dan berkemungkinan mengesan semua kerosakan yang mungkin terdapat di dalam sel memori menggunakan koleksi algoritma yang berkesan. Walau bagaimanapun, sejumlah besar sel memori yang dibalut oleh logik BIST boleh mengakibatkan overhed yang besar dalam kawasan pendawaian dan pintu, dan juga pengaruh yang memudaratkan pada prestasi ingatan. Oleh itu, reka bentuk MBIST baharu untuk SoC termaju yang menangani cabaran mesti diterokai untuk mengurangkan kos keseluruhan ujian pembuatan. Adalah penting untuk memilih tahap liputan dan diagnosis algoritma yang sesuai untuk julat saiz tatasusunan. Algoritma March 5n membuktikan bentuk alternatif algoritma berasaskan March dengan panjang ujian yang lebih baik telah mencapai masa ujian yang lebih singkat daripada algoritma MATS++ konvensional tanpa menghukum liputan kerosakan. Algoritma dan seni bina ujian memori ini sesuai dengan keperluan untuk ujian tatasusunan pantas untuk memasarkan produk dengan cara yang paling pantas. Walau bagaimanapun, kerja sebelumnya boleh dilanjutkan untuk pengesanan kerosakan gandingan penyongsangan dan sokongan pembaikan. Oleh itu, seni bina March 5n digunakan sebagai asas dalam projek ini. Seni bina March 5n yang dipertingkatkan dicadangkan untuk melanjutkan sifatnya dari segi liputan kerosakan dan keupayaan diagnosis untuk membolehkan analisis kegagalan ingatan. Algoritma Blok March, penjana alamat, penjana data, modul diagnosis dan logik redundansi ialah komponen seni bina BIST yang disasarkan. Litar yang luas daripada seni bina sebelumnya akan dilaksanakan untuk mencapai matlamat. Logik tambahan akan mengumpul maklumat kesalahan dan keputusan diagnosis yang sepadan akan dilaporkan semasa ujian ingatan. Alat Automasi Reka Bentuk Elektronik Synopsys (VCS, Design Compiler dan Verdi) digunakan dalam mensintesis dan menilai prestasi dari segi kelajuan, kawasan, kuasa dan liputan kerosakan. Beberapa laporan dan bentuk gelombang dijana dan disimulasikan untuk penilaian. Hasil projek ini telah menunjukkan bahawa menambah lebih logik boleh meningkatkan keupayaan untuk diagnosis dan membolehkan pengaturcaraan berlebihan menggantikan sel yang rosak. Selain itu, liputan kerosakan gandingan penyongsangan menggunakan March 5n disahkan berfungsi seperti yang dimaksudkan. Mempercepatkan peruntukan ruang memori yang berlebihan dalam mekanisme pembaikan dicapai dengan seni bina yang dicadangkan kerana keupayaan untuk menjejaki setiap tandatangan kegagalan memori apabila diuji. Berbanding dengan kerja terdahulu, seni bina yang dipertingkatkan secara amnya telah meningkatkan kelajuan jam maksimum sebanyak hampir 8% dan mengurangkan pelesapan kuasa sebanyak kira-kira 6%. Walau bagaimanapun, kelajuan dan kefungsian yang lebih tinggi diperoleh dengan kos 4% daripada overhed kawasan.

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| | | |
|---|---|---|
| AF | - | Address-decoder Fault |
| BIRA | - | Built-In Repair Analysis |
| CFin | - | Inversion Coupling Fault |
| DPM | - | Defect Per Million |
| ECC | - | Error Correction Code |
| EDA | - | Electronic Design Automation |
| MBIST | - | Memory Built-In Self-Test |
| SAF | - | Stuck-At Fault |
| SoC | - | System-on-Chip |
| SRAM | - | Static Random-Access Memory |
| TF | - | Transition Fault |

## LIST OF SYMBOLS

| | | |
|---|---|---|
| ↑ | - | Rising transition of a memory cell |
| ⇑ | - | Increasing memory addressing order |
| ↓ | - | Falling transition of a memory cell |
| ⇓ | - | Decreasing memory addressing order |
| ↕ | - | Complement contents of a memory cell |
| ⇳ | - | Either increasing or decreasing memory address order |
| r0 | - | Read a 0 from the memory location |
| r1 | - | Read a 1 from the memory location |
| ra | - | Read address value from the memory location |
| rb | - | Read complement address value from the memory location |
| w0 | - | Write a 0 to the memory location |
| w1 | - | Write a 1 to the memory location |
| wa | - | Write address value to the memory location |
| wb | - | Write complement address value to the memory location |

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# CHAPTER 1

# INTRODUCTION

## 1.1 Problem Background

Memory arrays are essential parts of microprocessors and System-on-Chips (SoC). As Moore's Law is driving the CMOS technology scaling, it brings a linear improvement in SRAM density. As a result, the demand for memories and their size in these products has constantly grown throughout the years. Memory failures are more common than logic faults because memories are dense and designed limited to the technology [1]. Thus, verification of functional memories is an important aspect of any SoC design cycle as it allows the designer to identify possible memory faults ahead of time. Effective memory testing and rapid memory problem diagnostics are important in the competition to bring another next-generation device to the market. In a high-density SRAM, the timing margins and a large number of states are highly prone to faults like Stuck-At-Faults, Address-decoder-Faults and Transition-Faults which are caused by gross significant flaws. All of them must be screened to meet the product's low Defect Per Million (DPM) goals.

The common method utilized to test embedded memories automatically is Memory Built-in Self-Test (MBIST) solutions. MBIST is a standard approach to test the embedded memory arrays for functionality and potentially detect all of the faults that may be present inside the memory cells by performing reads and writes sequences using an effective collection of algorithms. MBIST offers low cost in tests due to the reduction of dependency on external electrical testing using an Automatic Test Equipment (ATE). As memory cells are made up of transistors or capacitors, logic gates cannot be used to model them. Memory testing cannot use structural tests based on gate-level netlists. Memory cores have a very regular structure due to equivalent memory blocks and incredibly basic functional operations which are mainly read and write, making them ideal for functional testing. Functional test programmes for

embedded memory cores may be built via compact and flexible on-chip test pattern generators, unlike random logic testing, which requires a huge library of deterministic test patterns to get the needed fault coverage. Additionally, as written data in a fault-free memory remains unchanged, predicted responses can be simply re-generated on-chip, and output responses could be checked using minimal overhead comparison circuitry. As a result, the memory BIST circuit has fewer components than the logic BIST circuit. Memory BIST has developed as a state-of-the-art technique in the industry due to its deterministic nature.

Embedded memory arrays have the same test issues as SOCs since they are components of a SOC. The cost of testing embedded memory, on the other hand, has its characteristics, which are determined by three primary factors including cost of ATEs, manufacturing testing time and BIST area overhead. Reduced testability, high amount of test data, heterogeneous IP cores and at-speed testing are all difficulties that may be overcome by using programmable embedded memory BIST systems. However, because a single SOC may have dozens or hundreds of different memory cores, power-constrained test scheduling is required to save testing time. Furthermore, a large number of memory blocks surrounded by BIST circuitry will result in significant routing and gate area overhead, as well as a negative impact on memory performance. To minimise the total cost of manufacturing tests, new memory BIST designs for complex SOCs that meet the foregoing concerns must be investigated.

## 1.2 Problem Statement

As the density of transistors keeps increasing with the advancement of technology, the demand for larger memories is also increasing and thus making memory array testing becomes a challenging task. The memory tests are expected to deliver the best fault coverage possible and short Time-To-Market and low DPM. However, existing algorithms offer high coverage but are usually coupled with a long test time. The test time highly depends on the operation count of an algorithm. A higher operation count of a test consumes a longer test time. A complex algorithm provides a good fault coverage but a long test time. To reduce test time, simply increasing

operating frequency is not an ideal option since it may cause signatures in the memory to be corrupted. MBIST may begin to experience unintended errors at a higher frequency, which may result in unexpected behaviour [2]. Furthermore, testing every Byte of memory on an SoC becomes time expensive due to a large amount of memory present. Therefore, an optimum balance between fault coverage and test time is necessary to identify possible memory faults. MBIST mechanism has to be optimised for faster memory validation to reduce the time-to-market of the product.

The growing memory content of SoCs has a proportional influence on-chip yield, demanding comprehensive testing of all integrated memories. Thus, simply detecting memory defects in SoCs is no longer sufficient to get a high yield [3]. One approach to address this issue is to add redundant memory locations to the memory. The address mapping of the fault-free working memory can be programmable within certain restrictions. To accomplish memory repair, a diagnosis module is required to identify the faulty location [4]. Fault address and data collection are carried out during testing to allow the redundancy programming but area overhead will induce by the additional circuity. Thus, the balance trade-off between speed, area and power of the MBIST architecture with the repairable feature are important criteria to achieve this goal. Hence, MBIST design is more beneficial from low area overhead redundancy logic to improve the yield.

## 1.3 Research Goal

### 1.3.1 Research Objectives

The objectives of the research are:

1. To design an improved March 5n MBIST architecture (from the previous work) with better fault coverage and diagnosis capabilities by implementing a diagnosis module.

2. To simulate and evaluate the proposed March 5n and MATS++ MBIST design in terms of speed, power, area, and fault coverage with the previous work using Synopsys EDA tools.

## 1.4 Research Scopes

The scope of this study has been narrowed to clarify the issue and conduct a more thorough investigation. The scope of this project included:

1. Fault diagnosis coverage in this project is focusing on Stuck-At Faults, Address Decoder Faults, Transition Faults and Inversion Coupling Faults only.

2. MBIST performance evaluation is based on the improved March 5n FSM-Based architecture and the memory used for validation is 1kb ($32\times2^5$) and 2kb ($32\times2^6$).

3. Synopsys EDA tools are utilized for synthesis and the target library is *cb13fs120_tsmc_max* (130 nm technology).

4. The design constraints in this project are proliferated from previous work [5].

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