RELIABILITY ANALYSIS OF JUNCTIONLESS FIN FIELD EFFECT TRANSISTOR (JL-FINFET)

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DEDICATION

This thesis is dedicated to my father, who taught me that the best kind of knowledge to have is what is learned for its own sake. It is also dedicated to my mother, who taught me that even the largest task can be accomplished if it is done one step at a time.

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ABSTRACT

When scaling down of transistors reaches below 20nm, the reliability of a device becomes more important due to the device's needs to sustain its performance while also being able to endure reliability degradation effects. Junctionless Fin Field Effect Transistor (JL-FinFET) provides a solution for conventional MOSFET problems such as the short channel effects while displaying better performance. In this project, the two most notable reliability issues of MOSFET which is Negative Bias Temperature Instability (NBTI) and Hot Carrier Injection (HCI) will be analysed on the proposed device structure of JL-FinFET. The structure of the JL-FinFET was constructed using a 15nm gate length (L_g), the fin width and fin height used were 10nm while the doping concentration for the source and drain terminal for N-type and P-type were fixed at $1.5x10^{19}cm^{-3}$. The work function for the N-Type and P-Type JL-FinFET were set to 4.6eV and 4.65eV respectively and the oxide thickness used for the structure was 1nm. An analytical study of JL-FinFET concerning the degradation of threshold voltage (ΔV_{th}) and on-current (ΔIon) by varying different device parameters such as they will be carried out between before and after stress applications. The reliability test for the reliability issues were carried out by varying stress voltage of 1.2V to 2.5V for HCI and 1.8V to 3.0V for NBTI for a stress time up to 10,000 seconds. ΔV_{th} and ΔI_{on} are the difference of the threshold voltage and on-current before and after stress application. This project aims to provide data on the degradation mechanism of NBTI and HCI on JL-FinFET and therefore, predict the lifetime estimation up to 10 years of extrapolation of the JL-FinFET by using the power-law extrapolation method. This can be achieved by simulating the JL-FinFET's device structure and applying stress tests on the proposed device. To analyse the degradation effect on the device, several sets of stress voltage will be applied to the proposed device; to the gate terminal to observe the NBTI degradation and to the drain terminal to analyze the HCI degradation. Results show when stress is applied to the drain or gate terminal the V_{th} will increase thus increasing the voltage to turn on the device which signifies degradation. As the stress voltage applied increased the V_{th} also increase, which exhibits the degradation process will be faster if a higher stress voltage is applied. Results obtained show for the stress voltage of 1.8V the change of the V_{th} shift was 41.45% for HCI while for NBTI at stress voltage -1.8V the V_{th} was 15.7% indicating a faster degradation rate for HCI compared to NBTI.

ABSTRAK

Bila masa proses mengecilkan transistor menjangkaui kurang daripada 20nm, kebolehharapan peranti tersebut menjadi lebih penting disebabkan peranti tersebut perlu mengekalkan prestasinya dan juga mengelak dari kesan keboleharapan tersebut. Junctionless Fin Field Effect Transistor merupakan penyelesaian untuk masalah konvensional MOSFET seperti "Short Channel Effect (SCE)" disamping menunjukkan peningkatan dalam prestasinya. Dalam projek ini, dua isu kebolehharapan yang sering terjadi kepada MOSFET ialah Negative Bias Temperature Instability (NBTI) dan Hot Carrier Injection (HCI) akan dikaji untuk struktur yang dicadangkan iaitu JL-FinFET. Struktur JL-FinFET dibina menggunakan 15nm gate length (L_g), kelebaran Fin dan Tinggi Fin digunakan ialah 10nm manakala doping concentration untuk source and drain terminal for N-type and P-type ditetapkan kepada $1.5x10^{19}cm^{-3}$. Work function yang digunakan untuk N-Type and P-Type JL-FinFET masing-masing ditetapkan kepada to 4.6eV and 4.65eV dan akhirnya oxide thickness yang digunakan ialah 1nm. Kajian analisis berkenaan JL-FinFET melibatkan kemerosotan Threshold voltage (ΔV_{th}) dan on-current (ΔI_{on}) dengan menggunakan parameter peranti yang berbeza-beza akan di jalankan terhadap peranti sebelum aplikasi tekanan dan selepeas aplikasi tekanan dalam bentuk voltan. Ujian keboleharapan yang dijalankan menggunakan voltan tekanan berbeza-beza iaitu 1.2V sehingga 2.5V untuk HCI dan 1.8V sehingga 3.0V untuk NBTI untuk tempoh masa sehingga 10,000 saat. Projek in bertujuan untuk mengumpul informasi berkenaan mekanisme keboleharapan NBTI dan juga HCI terhadap JL-FinFET dan seterusnya meramalkan jangka hayat JL-FinFET menggunakan kaedah power-law extrapolation. Proses in boleh dicapai dengan simulasi struktur JL-FinFET dan ujian aplikasi voltan tekanan kepada peranti tersebut. Untuk menganalisa kesan keboleharapan terhadap peranti tersebut beberapa aplikasi tekanan voltan yang berbeza akan diberikan kepada peranti tersebut; aplikasi tekanan kepada "gate terminal" untuk kemerosoton NBTI dan aplikasi tekanan kepada "drain terminal" untuk kemerosoton HCI. Hasil daripada simulasi menunjukkan aplikasi tekanan voltan kepada "drain" dan "gate" "terminal" akan menyebabkan perubahan "threshold voltage" (ΔV_{th}) menunjukkan terdapatnya proses kemerosotan. Apabila tekanan voltan yang diberikan ditingkatkan ΔV_{th} juga akan meningkat menunjukkan bahawa proses kemerosotan akan meningkat jika tekanan voltan yang diberikan juga meningkat. Keputusan yang diperolehi menunjukkan untuk voltan tekanan 1.8V perubahan V_{th} ialah 41.45% untuk HCI manakala untuk NBTI di voltan tekanan -1.8V peruabahan V_{th} ialah 15.7% menunjukkan kadar kemerosoton yang lebih pantas untuk HCI berbanding NBTI.

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LIST OF ABBREVIATIONS

V_{th}	-	Threshold Voltage
I_D	-	Drain Cuurent
FinFET	-	Fin Field Effect Transistor
JL-FinFET	-	Junctionless Fin Field Effect Transistor
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
TDDB	-	Time Dependent Dielectric Breakdown
UTM	-	Universiti Teknologi Malaysia
NBTI	-	Negative Bias Temperature Instability
HCI	-	Hot Carrier Injection
SOI	-	Silicon on Insulator
BOI	-	Body on Insulator
UTBB	-	Ultra-Thin Body and Buried Oxide
SS	-	Subthreshold Swing
DIBL	-	Drain Induce Barrier Lowering
JNT	-	Junctionless Transistor
IM	-	Inversion Mode
AM	-	Accumulation Mode

CHAPTER 1

INTRODUCTION

1.1 Problem Background

As the demand for faster processing speed and increasing performance rose the need of scaling down the transistor has continue to be a critical factor due to the need of more transistor to be able to be integrated into a single microchip to get an improve performance. According to Moore's law by Gordon Moore the number of transistors that can be integrated on microchips will double every two years. Meaning that for every two years there is potential of increasing of performance of computers since the greater number of transistors in the chips will give a faster switching speed. Base on this Figure 1.1 we can see a trend of increase number of transistor in a single microchip every two years by semiconductor company to support the Moore's law.

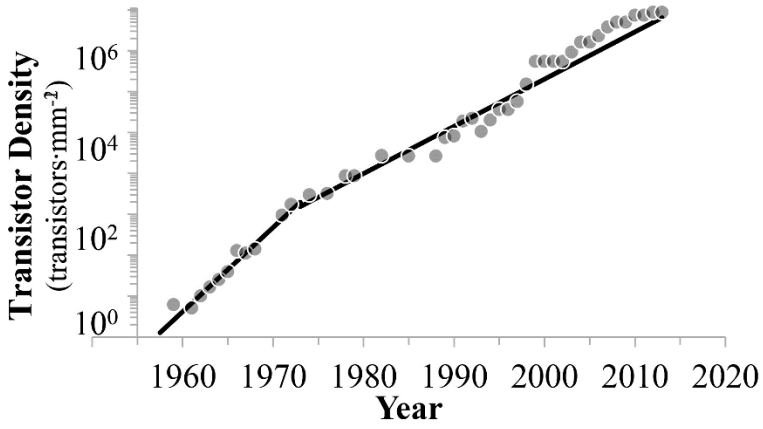

Figure 1.1 Moore's Law [1]

Despite this, researchers have run into a stumbling block in order to keep up with the trend of the Moore's law due to problems arose from scaling down the transistor. When the scaling down process continues the conventional FinFET that is widely used reaches its limitation due to occurring reliability issues, leakage currents

and scalability of the threshold voltage. In order to overcome this problem researches have come up with a new technology called the Junctionless Fin Field Effect Transistor (JL-FinFET). When the size of such transistors shrinks, the junctions will get closer, resulting in difficulty such as the short channel effect when the size is lowered to the nanoscale scale. Realizing junctionless transistors is one of the potential solutions to this problem. Figure 1.2 shows an example of the JL-FinFET structure.

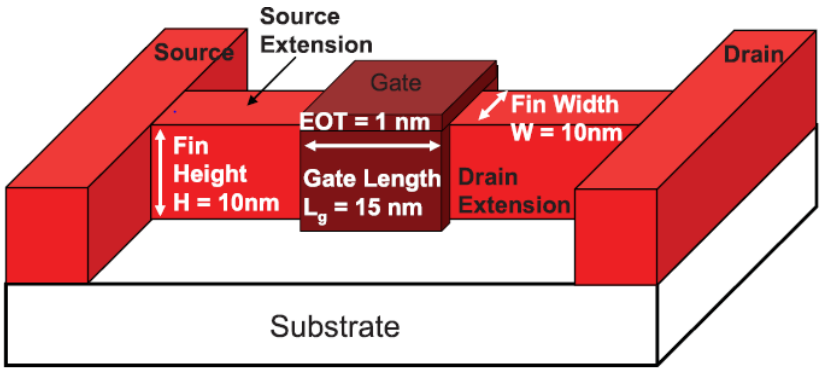

Figure 1.2 JL-FinFET Structure [2]

A junctionless is a type of transistor when the same doping type is applied to the source, drain, and channel regions thus the doping concentration gradient is completely minimized due to the same doping concentration. When compared to conventional methods, the fabrication process is easier since now the doping type and doping concentration across the source channel and drain are all the same. A junctionless transistor provides less threshold voltage to turn on and the on/off current ratio is quite high.

1.2 Problem Statement

Continuous scaling down of transistors below 20nm makes the reliability of a device becomes more important due to the device needs to sustain its performance while also being able to endure reliability degradation effects. The most notable reliability issues of FinFET are Negative Bias Temperature Instability (NBTI) and Hot Carrier injection (HCI). However, the information regarding reliability issues of JL-FinFET is still lacking due to it being a new develop structure which is why continuous study on the reliability is important to ensure its potential as a future replacement for FinFET technology.

1.3 Research Goal

To design and simulate the JL-FinFET and investigate the effect of Negative Bias Temperature Instability (NBTI) and Hot Carrier Injection (HCI) when stress voltage is applied to the device for period amount of time.

1.4 Research Objectives

The objectives of the research are:

1. To simulate and analyse electrical performances of 15nm, 12nm and 9nm Junctionless Fin Field Effect Transistor (JL-FinFET)
2. To study the degradation effect of Negative Bias Temperature Instability (NBTI) on p-channel JL-FinFET and Hot Carrier Injection (HCI) on n-channel JL-FinFET.
3. To estimate the lifetime prediction of JL-FinFET by using power-law extrapolation method.

1.5 Research Scope

1. Simulation and Design of JL-FinFET using Synopsis Sentaurus TCAD
2. Simulation of 15nm, 12nm and 9nm N-channel, P-channel JL-FinFET
3. Reliability test covers HCI and NBTI
4. HCI application done by stress application of voltage from 1.2V-2.5V on drain terminal of n-channel JL-FinFET
5. NBTI application done by stress application of voltage from 1.8V-3.0V on gate terminal of p-channel JL-FinFET
6. Stress time application for HCI and NBTI is for 10000s
7. Lifetime estimation up to 10 years of extrapolation of device by using power-law extrapolation method

1.6 Research Gap

The identified gap in this project is the lack of study regarding the reliability test of Negative Bias Temperature Instability and Hot Carrier Injection on the Junctionless Fin Field Effect Transistor. Previous literatures have shown some studies regarding the NBTI and HCI however the studies were only done on the conventional FinFETs and conventional MOSFETs and only for a small range of stress voltage for a short amount of time. The project done in this report will hope to fill this gap and provide further information on the reliability of JL-FinFET

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