EXPLICIT CHARGE-BASED MODEL FOR STRAINED-SILICON GATE-ALL-AROUND MOSFET INCLUDING QUANTUM AND SHORT CHANNEL EFFECTS

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DEDICATION

To my beloved family

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ABSTRACT

In the recent development of advanced nanoelectronic devices, strain application on silicon Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) has been identified as a key factor towards the improvement of device performance. Strained-silicon is preferred due to less impact of the short channel effects, enhanced the carrier mobility and lower the threshold voltage . Besides, strained-silicon can be applied to the non-planar multi-gate structures such as Gate All Around (GAA) MOSFET. Charge-based modelling (Q_m) technique is widely been used for unstrained GAA MOSFET. However, in this research work, the approach is exercised for strained-silicon GAA MOSFET and subsequently to characterise its electrical behaviour in long and short channel devices. The model is solved explicitly using a smoothing function to avoid the convergence issue compared to the numerical model. For one-dimensional (1D) strained silicon GAA MOSFET, the geometry scaling in the radial direction which includes the radius and oxide layer thickness of the silicon layer can contribute to the quantum effects. In order to improve the accuracy of the model, quantum capacitance and threshold voltage were integrated into the long channel explicit model to facilitate the quantum effect. For the short channel model, second-order physical effects were included such as velocity saturation, channel length modulation and threshold voltage roll-off to resemble the behaviour of the short channel device. Afterwards, the results from the constructed models are compared against the Technology Computer Aided Design (TCAD) simulation and published data. A good agreement was achieved between model and simulated data indicates that the physical mechanisms of quantum and short channel effects used in the model are valid. Besides, it is shown that the existence of quantum starts to exhibit for radius and oxide layer less than 10 nm and 14 nm, respectively, regardless of the channel length being used in the device structure. For device optimisation, gate stack with SiO_2/HfO_2 configuration is preferred due to its smaller leakage current. The most optimised dimension is attained with the gate length of 40 nm attributed to the enhanced overall electrical performances. The extracted threshold voltage and on-state current obtained as 0.164 V and 8000 uA/um, accordingly, where the values outperform the IRDS benchmarking for low power application device.

ABSTRAK

Pada era pembangunan peranti nanoelektronik pada masa kini, penegang silikon semikonduktor oksida logam transistor kesan medan (MOSFET) telah dikenal pasti sebagai penyumbang utama kepada peningkatan prestasi bagi peranti semikonduktor. Teknologi ini telah mendapat sambutan dikalangan penggiat semikonduktor disebabkan oleh pengurangan kesan pengecilan saiz saluran, peningkatan dalam kebolehgerakan cas pembawa dan merendahkan voltan ambang . Disamping itu juga, penegang silikon boleh digunakan untuk peranti semikonduktor berasaskan pelbagai dimensi get seperti GAA MOSFET. Pemodelan berasaskan cas pembawa (Q_m) telah digunakan secara meluas untuk peranti get-silinder menyeluruh (GAA MOSFET) tanpa kesan penegang silikon. Walaubagaimanapun, dalam kajian ini, teknik pemodelan tersebut digunakan untuk peranti get-silinder menyeluruh dengan kesan penegang silikon (strained-silicon GAA MOSFET) bertujuan untuk menganalisa parameter elektriknya termasuk peranti saluran panjang dan pendek. Model tersebut boleh diselesaikan dengan mendapatkan formula eksplisit menggunakan fungsi pelicinan (smoothing function) untuk mengelak masalah penumpuan ketika simulasi berbanding model berangka yang lain. Untuk peranti tegangan silikon 1D GAA MOSFET, penskalaan geometri pada arah radial termasuk radius dan ketebalan lapisan penebat silikon boleh menyumbang kepada kesan kuantum. Untuk meningkatkan ketepatan model, model kapasitan dan voltan ambang perlu mengambil kira kesan fizik kuantum. Untuk model peranti yang menggunakan saluran pendek, kesan fizik seperti kesan kelajuan tepu, perubahan panjang saluran, dan pengurangan voltan ambang turut dipertimbangkan kerana fenomena ini wujud dalam saluran pendek. Seterusnya, perbandingan hasil simulasi diantara matematik model, TCAD dan jurnal yang telah diterbitkan dilakukan untuk tujuan pembuktian model. Melalui kaedah tersebut, simulasi untuk setiap data adalah selari . Disamping itu, kesan quantum mulai wujud apabila radius dan ketebalan penebat kurang daripada 10 nm dan 14 nm. Untuk mengoptimumkan prestasi peranti, penebat bertingkat menggunakan kombinasi SiO_2/HfO_2 dipilih kerana mampu mengurangkan arus bocor. Dimensi yang paling optimum diperoleh dengan menggunakan saluran panjang 40 nm disebabkan oleh peningkatan keseluruhan prestasi elektrik. Nilai voltan ambang dan arus yang diekstrak adalah $0.164\,V$ dan $8000\,uA/um$, dimana nilai tersebut mengatasi nilai rujukan IRDS bagi peranti yang menggunakan kuasa rendah.

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LIST OF ABBREVIATIONS

CMOS	–	Complementary Metal-Oxide-Semiconductor
GAA	–	Gate-All-Around
GAA MOSFET	–	Gate-All-Around Metal-Oxide-Semiconductor field-effect transistor
MOSFET	–	Metal-Oxide-Semiconductor field-effect transistor
IRDS	–	International Roadmap of Devices and Systems
ERM	–	Emerging Research Materials
ITRS	–	International Technology Roadmap for Semiconductors
MATLAB	–	Matrix Laboratory
NTRS	–	National Technology Roadmap for Semiconductors
TB	–	Tight Binding
SS	–	Subthreshold Slope
3D	–	Three Dimensional
2D	–	Two Dimensional
1D	–	One Dimensional
BSIM	–	Berkeley Short-Channel IGFET Model
CBM	–	Charge Balance Model
CLM	–	Channel Length Modulation
DIBL	–	Drain Induced Barrier Lowering
EOT	–	Effective Oxide Thickness
FD	–	Fully-depleted
GS	–	Gate stack
GCA	–	Gradual Channel Approximation

TCAD	–	Technology Computer Aided Design
BQP	–	Bohm Quantum Potential
SRH	–	Shockley Read Hall
SCE	–	Short Channel Effect
High-k	–	Dielectric with high value of k
IoT	–	Internet of Thing
CESL	–	Contact etch stop linear
SOI	–	Silicon on Insulator
SSOI	–	Strained-Silicon on Insulator
HH	–	Heavy hole
LH	–	Light hole
SO	–	Split off
tri-gate	–	Triple gates
FinFET	–	Fin Field Effect Transistor
HiSIM	–	Hiroshima-University STARC IGFET Model
MM 11	–	MOS Model 11
SP	–	Surface Potential
ACM	–	Advanced Compact Models
EKV	–	Enz-krummenacher-Vittoz Model
BSIM	–	Berkeley Short-channel IGFET Model
IGFET	–	Independent Gate Field Effect Transistor
EOT	–	Effective Oxide Thickness
CNT	–	Carbon Nanotube
SRAM	–	Static Random Access Memory

LIST OF SYMBOLS

L_g	–	Gate length
$\triangle L_g$	–	Variation of channel length due to channel length modulation
I_{off}	–	Off-state current
I_{on}	–	On-state current
V_{th}	–	Threshold Voltage
v_{th}	–	Termal Voltage
v_{sat}	–	Velocity saturation
V_{th_long}	–	Threshold Voltage for long channel
ϕ_s	–	Surface Potential of silicon
V_{ox}	–	Voltage across oxide layer
V_{fb}	–	Flat-band Voltage
$(\phi_s)_{s-Si}$	–	Surface Potential of strained-silicon
$\left(V_{fb}\right)_{s-Si}$	–	Flat-band Voltage of strained-silicon
n_i	–	Instrinsic carrier
$n_i^{Si_{1-x}Ge_x}$	–	Instrinsic carrier in SiGe region
$n_i^{strained-Si}$	–	Instrinsic carrier in Strained-Silicon region
ΔE_c	–	Conduction band shift
N_a	–	Acceptor doping
N_d	–	Donour doping
ΔE_g	–	Energy band shift
ΔV_{fb}	–	Flat-band shift
ϕ_{Si}	–	Workfunction for Silicon
ϕ_m	–	Workfunction for Gate

χ_{Si}	–	Electron Affinity of Silicon
q	–	Electronic charge
λ_c	–	Natural length
λ_a	–	Velocity overshoot
l_c	–	Reference length
t_{ox}	–	Oxide thickness
t_{high-k}	–	Oxide thickness of high-k material
t_{si}	–	Body thickness of the silicon
R	–	Radius
a_x	–	Lattice constant in horizontal direction
a_y	–	Lattice constant in vertical direction
x	–	Germanium fraction
$\triangle_2$	–	Two-fold degenerate
$\triangle_4$	–	Four-fold degenerate
k	–	Wave factor
χ	–	Electron Affinity
Si_3N_4	–	Silicon Nitride
HfO_2	–	Hafnium Oxide
Al_2O_3	–	Aluminium Oxide
Si	–	Silicon
SiO_2	–	Silicon-oxide
I_{ds}-V_{ds}	–	Drain Current versus Drain Voltage
I_{ds}- V_{gs}	–	Drain Current versus Gate Voltage
V_{gs}	–	Gate source voltage
ε_{SiO_2}	–	Permittivity of oxide layer
ε_{high-k}	–	Permittivity of high-k

ε_{si}	–	Permittivity of silicon
Q_i	–	Inversion charge
Q_d	–	Depletion charge
Q_f	–	Fixed oxide charge
Q_{is}	–	Inversion charge at source end
Q_{id}	–	Inversion charge at drain end
ΔV_{th}	–	Threshold Voltage shift
ΔV_{th_sc}	–	Threshold Voltage shift with short channel effect
V_{ch}	–	Fermi potential along the channel
μ_{sc}	–	Mobility of the carrier with short channel effect
μ_{eff}	–	Effective mobility of the carrier
μ	–	Mobility of the carrier
W_d	–	Width of the channel
Δz	–	The changes of centroid position
z	–	The position of centroid position
C_{ox}	–	Gate capacitance
C_{oxeff}	–	Effective gate capacitance
Q_{in_ss}	–	Inversion charge of strained-silicon
Q_{insc_ss}	–	Inversion charge of strained-silicon with short channel effect
V_{th_ss}	–	Threshold voltage of strained-silicon
V_{thq_ss}	–	Threshold voltage of strained-silicon with quantum effect
V_{thsc_ss}	–	Threshold voltage of strained-silicon with short channel effect
α	–	Alpha
γ	–	Gamma
h	–	Planck's constant
n	–	carrier density

M^{-1}	–	Inverse effective mass
μ_{n0}	–	Electron low field mobilities
E	–	Electric field
$BETAN$	–	Mobility
v_{satn}	–	Velocity saturation of electron
E_g	–	Energy bandgap
ϕ_b	–	Barrier height
$SiGe$	–	Silicon Germanium
SiC	–	Silicon Carbon
Ge	–	Germanium
$InGaAs$	–	Indium Gallium Arsenide
$III-V$	–	Three-five material
Cu	–	Copper
V_{dd}	–	Power supply

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CHAPTER 1

INTRODUCTION

1.1 Research Background

For decades, the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) has become the core building block for almost all computing devices. A tremendous demand in electronic appliances due to massive economic growth has enforced the semiconductor player to provide a high-quality product with higher processing speed, smaller size and lower in power consumption of the MOSFETs. This remarkable evolution of semiconductor technology is motivated by Moore's Law and coupled with Dennard Law for both device and power consumption scaling [1-2]. According to Moore's Law which introduced by Gordon Moore, the number of transistors on a chip will be doubled for every two years when the gate length reduced by a factor of 0.7 as shown in Figure 1.1.

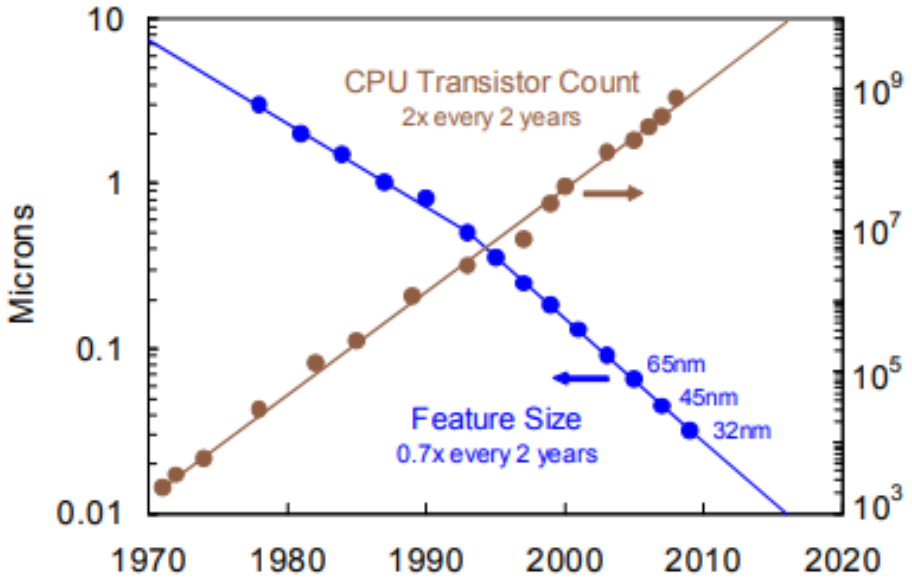

Figure 1.1 Transistor scaling based on Moore's Law prediction.

However, as the channel length of the MOSFET reaches nanometer scale, the scaling constraint such as higher leakage current starts to limit the device scaling further. Thus, a standard semiconductor roadmapping provider such as IRDS is introduced to look for more alternative and addressed possible issue occurred in the near future. Previously, NTRS and ITRS were the organisations that have been appointed to set the roadmap of the transistors and the community members mostly semiconductor expert, working closely with the semiconductor industries. Besides, the previous roadmappings were merely focusing on the alternatives emerging device (Table1.1) and improvement on the performance of the transistor but less attention is given on the application. Therefore, some of the guidelines in IRDS are taken from ITRS and added with some benchmark on the emerging architecture and systems which may relate to the evolution of cloud storage, seamless interaction of big data and instant data [3].

Since IRDS is given responsibilities for providing guidelines and directions to sustain the scaling technology, thus, the focus teams from IRDS community have outlined challenges and potential solutions related to device and transistor-level into several groups such as the More Moore, Beyond CMOS and Emerging Research Materials. Figure 1.2(a) shows the paradigm of an electronics industry has started to use emerging materials from device to architecture levels rather than the conventional MOSFET, as reported in ITRS 2012. Moreover, these technology shift is driven by the novel computing paradigms which require a system to operate with higher performance and better efficiency as well as capable to integrate with more functionality to accommodate for a future era of computing application (big data, IoT, artificial intelligence) as depicted in Figure 1.2(b).

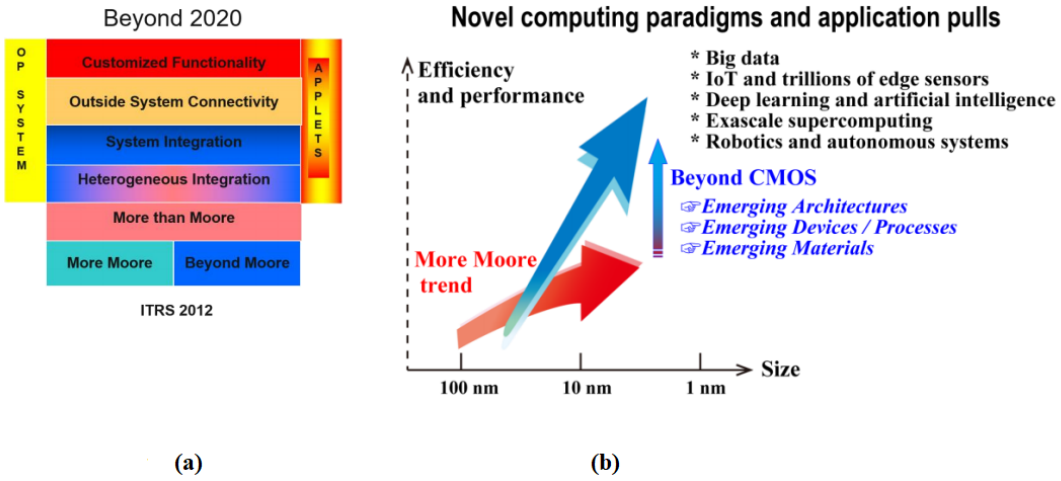

Figure 1.2 (a) The new paradigm of the electronic industry based on emerging devices. (b) Application of emerging device at all levels of electronic systems addressed by focus teams of Beyond-CMOS [4].

Table 1.1 List of emerging devices [5-7].

Advanced MOSFETs	
Structure	Vertical MOSFET, Double Gate, Double Gate, FinFET, Trigate, Omega gate and Gate All Around (Silicon Nanowire).
Material	Graphene, Carbon Nanotube(CNT), III-V material group and Cadmium Arsenide.

Some of the challenges and hurdles for emerging and current applied device have been addressed meticulously by a focus team of More Moore for further improvement and prevention in the future. These challenges cover for both near-term and long-term plans as listed in Table 1.2. Simultaneously, some potential solutions based on the issues highlighted in Table 1.2 have been discussed further. These solutions are expected to solve four targeted criteria: performance, power, area, and cost. For near-term solutions that related to the evaluation of device performance, the gate drive loss due to power supply scaling can be improved alternately by inducing strain to the channel, employed stress boosters and high-k metal gate, lowering contact resistance through new materials and wrap-around contact besides improving the electrostatics. Gate All Around (GAA)

device can be used to control the electrostatic effectively and expected to be adopted into the industry in 2021 [3] as being predicted in near term challenge. However, as the gate length is scaled-down less than 10 nm, the parasitics resistance and capacitance will be more dominant terms and caused the performance loss. This drawback is solved by addressing the solutions into long term challenges using vertical GAA structure. Besides, the substrate can be tailored using high-mobility materials such as Ge and III-V. Power reduction in vertical GAA using lower V_{dd} operation can be attained using highly-parallel 3D architectures. On the other hand, sequential integration of vertical GAA would enable stacking of the device on top of each other to reduce area and cost during the fabrication process. Based on challenges and advantages particularly related to Silicon Nanowire or GAA MOSFETs highlighted in Table 1.2 and 1.3, there is a necessity to further explore the capability and benefits for such devices. One of the alternative is to study the behaviour of the device through a physical model.

Table 1.2 Difficult challenges and potential solutions highlighted by focus team of More Moore [5-7].

Duration	Scope of Scaling Challenges	Potential Solutions
Near Term (2017-2024)	Power scaling	Improved device performance by applying strain to channel; stress booster, high-k metal gate, reduce contact resistance through new material and wrap-around contact, and improving electrostatic with GAA architecture.
	Parasitic scaling	
	Cost reduction	
	Integration enablement for SRAM-cache applications	
	Interconnect scalability	
Long Term (2025-2033)	Power scaling	Applied stacking vertical GAA structure to compensate performance loses, employed alternate high-mobility substrate materials, and using parallel 3D architecture.
	Vertical Structure	
	Thermal issue	
	Cost reduction with 3D integration	
	Integration of non-Cu metallization to replace Cu	

Table 1.3 Material for transistor scaling and integration by focus team of Emerging Research Material [5-7].

Application	Potential Emerging Material	Potential Advantages
High mobility semiconductor	InGaAs, InSb, strained III-V on silicon for p-channel	High hole mobilities for complementary MOSFETs.
	n-channel Ge	High electron mobilities for complementary MOSFETs.
	Co-integration of III-V and Ge	High electron and hole mobility
High mobility and steep subthreshold transistors	Si or Ge nanowires	High gate control of leakage current, possibly low surface scattering, and promise for 3D monolithic integration.
	III-V nanowires	High electron mobility with high gate control of leakage current. Promise for 3D monolithic integration.
	Carbon nanotubes [1–9]	High mobility with good channel control.
	Other 2D materials (MoS_2, WSe_2, germanene, silicene, etc.)	High mobility, good channel control, possibility of heterostructure and tunneling devices
Ultra high-k gate dielectric	TiO_2 or $SrTiO_2$	Improved transistor performance with low gate leakage and improved energy efficiency

Relentless device scaling has contributed to the deterioration in on-state current and the increment of leakage current due to the short channel effects and consequently, it degrades the electrical performance of the device. Several high mobility materials such as InGaAs, InSb, and strained III-V have been presented by a focus team of Emerging Research Material in Table 1.3, which advantages to increase the drive current. Besides that, performance loses due to device and power scaling also can be compensated with the incorporation of strain in the silicon channel which classified under high mobility material. Moreover, due to its benefits, abundant of strain application in the multi-gate devices have been reported in the literature indicate that such devices have growing interest among the researchers [8-11]. Since GAA structure acknowledges as a device with good electrostatic control, strain incorporation in the channel can further improve its electrical performance comprehensively such as on current (I_{on}), threshold (V_{th}), subthreshold swing (SS) and drain induced barrier lowering (DIBL). The privilege of GAA with a high mobility channel will increase the mobility of the device without dependent much on the doping level and allowed further downscale the channel length of the transistor [10-11]. Even though a heavily doped channel able to improve the carrier mobility, but, it will cause an increment in leakage current and unacceptable for certain applications [12]. Thus, the silicon channel of multigate-structures with high mobility materials is good potential to be implemented as a future nanoscale device.

1.2 Problem Statement

Strain applications have received positive feedbacks after being implemented into conventional MOSFET as a performance booster [13-15]. Due to the advantages of the electrical performance on transistors as being reported in previous works, the application has been extended to advanced MOSFET such as multi-gate device [16-20]. GAA MOSFET is considered as the best structure among the multi-gate devices due to its advantages which offers better electrostatic control and less short channel effects. Moreover, the introduction of strain on GAA MOSFETs recognised as one of the potential candidates in the application of transistors and believed to be a notable contribution toward the future nanoscale device. Besides, it also has been addressed

as part of the solution to overcome drive current degradation in the near term of IRDS (More Moore).

Previous researches have revealed that strained-silicon GAA MOSFET beneficial to be investigated due to its advantages which help to increase the mobility of the carriers notably and exhibiting tunable threshold voltage for high-speed application for MOSFETs [21-24]. Thus, fundamental and physical studies should be conducted at the device level. The analysis needs to address the impact of strain on its electrical performance such as threshold voltage and transfer characteristic (I-V). On the other hand, the physical model for long channel and short channel for strained-silicon GAA MOSFETs should be developed separately since the model involved with the different physical mechanisms. Besides, the integration of the gate stack can assist in lowering the leakage current effectively [25-28].

Therefore, to further investigate the advantages of this device, the research work should concentrate on the methodology that can be used to access its electrical properties. The literature reviews that highlighted in Chapter 2 (section 2.5.2) can serve as a baseline in finding the strengths and constraints of the published work in which may helps to identify the potential research gap that could be initiated in this work. Based on the literature, there are several scopes of researches question in strained GAA MOSFET yet to be revealed and uncertain in prior modelling work. These limitations acknowledged as a critical problem that needs to be solved through this work as summarised as follows:

1.2.1 Physical compact model of strained-silicon GAA MOSFET

There are several ways to examine and investigate the behaviour of a device such as a numerical model and analytical model. However, the analytical model is more favourable to be used by the industry due to its advantages such as shorter execution time and easy to be implemented. The analytical model can be expressed using a physical compact model and can be solved explicitly. In Gate All Around (GAA) MOSFET, the explicit method is widely been used attributed by the simplicity

of the model itself [23,47-49]. Nonetheless, for strained-silicon GAA MOSFET, there are inadequate literature based on the compact model have been reported. Kumar et al.,(2017) [23] and Sharma et al.,(2018) [40] have introduced the analytical model for strained Silicon/Silicon-Germanium GAA MOSFET structure using 2D Poisson's model and subsequently obtain its transfer characteristic solution for the short channel device. In these works, Silicon and SiGe are located at the outer and inner shell of the channel, respectively. Nevertheless, the structure is not practical to be utilised in a real-world as being reported by Hasmie et al.,(2008) [20] even though the model is formulated for strained GAA based on charge model.

Likewise, Zhang et al.,(2016) [22] and Liu et al.,(2012) [21] have used the same approach to model the strained GAA MOSFET but different device structure is applied as compared to the one that has been adopted in [20], where the strain effect is induced on the channel without the existence of the SiGe layer, and the channel is assumed in the form of strained-silicon. Moreover, the model is solved numerically based on the threshold voltage. Even though the device structure in [21,22] resemble with the one that has been fabricated device by Hasmie et al.,(2008) [20] but the physical model and analysis for strained GAA MOSFET still insufficient due to the complexity of the numerical model if being utilised in circuit simulator and hence can discouraging the technology transfer. Besides, there are fewer number of publication that addressed the physical mechanism of strain effect using a charge-based model which is important for circuit application.

1.2.2 Physical mechanisms that will affect the device performance

For a realistic compact model, the physical mechanism such as quantum effect should be taken into account in the model regardless of modelling frameworks that have been used to represent a MOSFET. Neglecting this effect may cause inaccuracy in data characterisation for a particular case. In conventional MOSFET, the condition for a quantisation effect to occur in the device when the doping channel more than $1x10^{18}\ cm^{-3}$ and oxide thickness scale down less than $2\ nm$ [41-43]. When a transistor encountered evolution from conventional to advanced MOSFET, the quantisation effect

would persist but may change based on device geometries. Thus, for multi-gate structures, the quantisation effect appears when the body thickness of the channel less than 10 nm [23,44]. Moreover, this effect is likely to occur in both the long channel and short channel devices [45-46].

Meanwhile, short channel effects are dominant in a short channel device due to the influence of the horizontal electric field in comparison to the vertical field. Generally, the velocity of the electron directly proportional to the strength of electric fields. As the gate length gets narrower, this effect would be significant. Besides that, other short channel effects need to be considered are the threshold roll-off, channel length modulation and mobility degradation [48-49]. Venugopalan et al.,(2012) [46] and Kumar et al.,(2017) have presented the modelling framework for long channel devices for unstrained and strained Si/SiGe GAA MOSFET, respectively. In different cases, the strained-silicon GAA model worked by Zhang et al.,(2016) and Liu et al.,(2012) have neglected the quantum effects in their model which may misinterpret the device operation and characterisation of electrical parameters such as threshold voltage, capacitance and inversion charge which gives strong effect on device transfer characteristic. Even though the model has considered the short channel effect, but the physical mechanism is limited for the threshold roll-off. Other circumstances such as velocity saturation, channel length modulation and mobility degradation [48-49] are remarkably important which determine the accuracy of the device model.

1.2.3 Alternative solutions to reduce leakage current

GAA MOSFETs are recognised as an ideal nanoscale device due to its outstanding electrical performance and received ample attention through numerous publications. Inducing strain effect on the silicon channel of GAA structure can enhance its electrical achievement further such as poses a higher driving current and lower threshold voltage. Based on the previous works, as the strain effect increases at a certain level of Ge fraction, it would reduce the operating voltage, DIBL and SS but slightly increased the subthreshold leakage current [33]. Based on these findings, the strain effect is beneficial in enhancing overall device performance except the leakage

current. Since the increment in on-state current is higher compared to off-state current, thus producing a higher current ratio. Based on this trend, leakage current increment due to strain effect is a trade-off with the rise of on-state current. However, for the sake of device reliability, gate stack (GS) insulator layer is introduced to scale down the leakage current. According to researches related to the application of GS are explained in Chapter 2 (refer section 2.5.3), it was found that leakage current and the short channels are mitigated significantly [50-51]. There are abundant of investigations pertaining to the impact of gate stack on multi-gate structures that have been highlighted in the publication. Most of the work concentrated on double-gate, trigate and GAA MOSFET [50-54]. Moreover, for strain application, the existing works only limited to the double gate and trigate structure [24,27-28,50,53-54]. However, the effect of gate stack on strained-silicon GAA MOSFET is yet to be highlighted and uncertain. Thus, it is crucial to perform the characterisation of the gate stack for such structure which important in lowering the leakage current.

1.3 Research Objectives

The primary purposes of this research are to model and simulate the characteristic of 1D of Strained-Silicon GAA MOSFETs for both long channel and short channel devices. In conjunction with the shortcomings and research gaps addressed in the previous section, the objectives are summarised as follow:

1. Compact model of long channel strained-silicon GAA MOSFET :-
   (a) To explicitly solve the mobile charge density including the trap charge and quantum effects for a wide range of body doping.
   (b) To obtain continuous drain current expression.
   (c) To study the impact of inversion charge and centroid charges based on the radius, doping and strain levels.

2. Compact model of short channel strained-silicon GAA MOSFET :-
   (a) To obtain continuous drain current expression based on quantum and short channel effects.
   (b) To investigate the impact of a short channel on the transfer characteristic of the device.
3. Characterisation of Gate Stack Strained Silicon GAA MOSFET :-
   (a) To determine and optimise the best gate stack combination for strained-silicon GAA MOSFET in lowering the leakage current and short channel effects.
   (b) To evaluate and benchmark the performance of the device with published work.

1.4 Research Scopes

The scopes of this research are addressed as below:

1. Analytical Modelling for long channel model: It involves obtaining the explicit solution of the mobile charge densities for the core model of strained-silicon GAA MOSFET. Subsequently, the correction charge model based on quantum effect is determined before solving the current continuity model. The condition for the quantum effect is considered when the radius and oxide thickness of GAA structure less than 10 *nm* and 14 *nm*, respectively.
2. Analytical Modelling for short channel model: The quantum and short channel effects are incorporated into a long channel of current continuity model . Besides that, the short channel effects include the velocity saturation, threshold roll-off, channel length modulation and mobility degradation. The model is limited for the gate length less than 100 *nm*.
3. Computational simulation: The mathematical derivations in the analytical model are performed using Mathematica simulation tool and the analysis are conducted through MATLAB. Meanwhile, the validity of the models is tested by comparing them with published work and 3D device simulation. In the TCAD tool, a model for the quantum model is invoked using the Bohr Quantum

Potential Model; meanwhile, for short channel device, velocity saturation model is employed.

4. Simulation work: For gate stack optimisation of strained-silicon GAA MOSFETs, a 3D device structure is used to compare with the analytical model earlier is extended and incorporated with gate stack for further performance improvement. Moreover, the quantum and velocity saturation models are invoked to accommodate the circumstances of a short channel device. Variations of gate stack combination using silicon nitride (Si_3N_4) , hafnium oxide (HfO_2) , and aluminium oxide (Al_2O_3) are tested and its final configuration is selected in which giving the smallest leakage current and better electrical performance such as SS, $DIBL$, V_{th} and current ratio.

1.5 Research Contributions

The significant contributions of this work are summarised as below:

1. Explicit and continuous compact model of long channel strained-silicon GAA devices: The analytical model for long channel strained-silicon GAA is formulated in the form of a charge-based model which simplified explicitly. Afterwards, the correction on charge-based model is performed to accommodate for smaller radius and oxide thickness of the device. After solving the charge model, the current continuity model is obtained for further analysis of the strain effect on the GAA structure.

2. Explicit and continuous compact model of short channel strained-silicon GAA devices: The model accomplished from the long channel device is then extended to further characterise the short channel device. Several physical mechanisms are used to represent such a device include the channel length modulation, velocity saturation, threshold-roll off and mobility degradation. These mechanisms are vital phenomena related to short channel effects. Based on this model, the behaviour of short channel strained-silicon GAA MOSFET is adequate to be used to analyse the transfer characteristic.

3. Optimisation of gate stack strained-silicon GAA MOSFET for low power application: 3D structure of strained-silicon GAA MOSFET is used to validate the compact model earlier that has been integrated with the gate stack configuration. Various high-k (Si_3N_4, HfO_2, Al_2O_3) material are examined to find the best combination of GS which gives the smallest leakage current and yet better overall electrical performance. The optimised device can serve for a low power application since it is used for low operating voltage and a higher driving current.

1.6 Thesis Organization

Chapter 1 provides the fundamental knowledge for this research. A comprehensive background of the roadmapping in the semiconductor field is highlighted with the challenges and potential solutions that can serve as a baseline to manage the research directions in nanoscale devices. After identifying the strength and weakness of previous works through the critically reviewing process, the problem statements related to the research direction are deduced. In conjunction with the problem statements, research objectives are identified. Subsequently, the scope of this research work is discussed further based on the existing literature and the available tools. Finally, the contributions of this work are explained briefly.

In Chapter 2, the literature reviews that related to fundamental of strain application on the transistors are discussed meticulously. Moreover, the strain evolutions from conventional to advanced MOSFETs are reviewed extensively to understand the concept and the techniques used to induce strain effect in different device structures and technology. On the other hand, the modelling framework also being highlighted to identify the appropriate model in describing the strain effect in GAA structure. Besides, the incorporation of the gate stack in a multi-gate device also being addressed concisely.

Chapter 3 elaborates the research method used to conduct this research work using general research flow and modelling flowchart in accomplishing the objectives.

In this section, the modelling frameworks used in Chapter 4 and Chapter 5 is discussed concisely. Other than that, the model used in the TCAD tool also emphasised.

Chapter 4 comprises the modelling framework for long channel strained GAA MOSFET. The model is formulated in term of the charge-based model and accounts the quantum effect due to aggressive scaling in gate oxide thickness and radius of the channel. Besides, the analysis discussed in this chapter has investigated the influence of strain on surface potential, inversion charge, centroid charge and transfer characteristic of the device.

Chapter 5 presents the compact model for the short channel strained-silicon GAA MOSFET. The model has incorporated the quantum and short channel effects to accommodate the physical mechanism as a short channel device. In this section, the analysis covers the impact of a short channel on the transfer characteristic of the device. Meanwhile, further investigation on the 3D structure of gate stack strained-silicon GAA MOSFET is performed by varying the thickness of the gate stack layer with various of the high-k material based on effective oxide thickness (EOT). The most optimised EOT is chosen in which giving the lowest leakage current and better electrical properties.

Chapter 6 summarised the essential findings and the contributions based on objectives discussed in Chapter 1. Besides, the future works are recommended to improve and ensure the continuation of the proposed device beneficial for compact model users which coming among the researchers and industries and afterwards might be used as a potential candidate in future CMOS application.

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