

COMPARISON OF SEVEN LEVELS SYMMETRIC H-BRIDGE MULTILEVEL  
INVERTER AND SEVEN LEVELS CASCADED  
H-BRIDGE MULTILEVEL INVERTER

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requirements for the award of the degree of  
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## **DEDICATION**

This project is dedicated to my father, who instilled in me the belief that there is no better type of wisdom than that which we acquire for its own sake. I also trust my mother, who taught me that I could fulfil any fantastic endeavour one step at a time. Additionally, my wife, Zatul Hijanah Bte Che Amat, has always supported me in completing my project, and she is always by my side when I am done.

## **ACKNOWLEDGEMENT**

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## **ABSTRACT**

An inverter is a power converter that transforms DC power to AC power using controlled power semiconductor switches. The inverter is categorized into many types based on output, source, type of load etc. This proposal focused on voltage source inverters. Voltage Source Inverter is further classified as a two-level inverter or classical multilevel inverter. Two-level inverter exhibits many harmonic components in output voltage and must utilize a bulky filter to produce pure sinusoidal voltage waveform. Nowadays, large manufacturing demands extensive and high power. The double-level inverter is not suitable for high power since it need to handle high voltage stress. A Multilevel Inverter topology was introduced to improve the constraints of the traditional inverter. However, Multilevel Inverter exhibit several significant limitations. One drawback is that at larger output voltage levels, the number of necessary semiconductor power switches will increase exponentially. The increased number of semiconductor switches harms system overall efficiency and reliability. This research aims to compare a seven-level Symmetric H-Bridge Multilevel Inverter with Cascaded H-Bridge Multilevel Inverter in terms of several semiconductor switches, AC output Voltage Levels, AC output current, THD, and Voltage stress at buttons. This project aims to design and simulate both topologies using MATLAB/Simulink and compare their performance. It is expected that the Symmetric H-Bridge MLI use a fewer quantity of components and use power switches with lower voltage rating as compared to Cascaded Multilevel Inverter.

## ABSTRAK

Inverter adalah penukar kuasa yang mengubah kuasa dc kepada kuasa ac menggunakan suis semikonduktor kuasa terkawal. Inverter dikategorikan kepada banyak jenis berdasarkan output, sumber, jenis beban dan lain-lain. Cadangan ini memberi tumpuan kepada penyongsang sumber voltan. Inverter Sumber Voltan dikelaskan lagi sebagai penyongsang dua tingkat atau penyongsang bertingkat bertingkat. Penyongsang dua tingkat menunjukkan banyak komponen harmonik dalam voltan keluaran dan mesti menggunakan penapis besar untuk menghasilkan bentuk gelombang voltan sinusoidal tulen. Pada masa kini, pembuatan besar memerlukan kuasa yang luas dan berkualiti dalam julat megawatt. Penyongsang dua tingkat tidak sesuai untuk daya tinggi kerana perlu menahan tekanan voltan tinggi. Untuk mengatasi keterbatasan inverter klasik, topologi inverter bertingkat diperkenalkan. Walau bagaimanapun, penyongsang bertingkat menunjukkan beberapa batasan yang ketara. Salah satu batasannya ialah bilangan suis kuasa semikonduktor yang diperlukan akan meningkat secara eksponensial untuk jumlah tahap voltan keluaran yang lebih tinggi. Peningkatan bilangan suis semikonduktor merosakkan kecekapan dan kebolehpercayaan keseluruhan sistem. Penyelidikan ini bertujuan untuk membandingkan Inverter Multilevel Symmetric H-Bridge tujuh tingkat dengan Inverter Multilevel Cascaded H-Bridge dari segi beberapa suis semikonduktor, Tahap Voltan output AC, arus keluaran AC, THD, dan tegangan voltan pada butang. Projek ini bertujuan untuk merancang dan mensimulasikan kedua-dua topologi menggunakan MATLAB/Simulink Software dan membandingkan prestasinya. Dijangkakan bahawa Symmetric H-Bridge Multilevel Inverter menggunakan lebih sedikit bilangan komponen dan menggunakan suis kuasa dengan penarafan voltan yang lebih rendah berbanding dengan Cascaded Multilevel Inverter

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## LIST OF ABBREVIATIONS

MLI	-	Multi-Level Inverter
BBTHB	-	Back-To-Back Modified T-Type Half-Bridge
AC	-	Alternating Current
DC	-	Direct Current
VSI	-	Voltage Source Inverter
CSI	-	Current Source Inverter
SPWM	-	Sinusoidal Pulse Width Modulation
SHE	-	Selective Harmonic Elimination
CHB	-	Cascaded H-Bridge
FC MLI	-	Flying capacitor Multi-Level Inverter
NPC MLI	-	Neutral Point Clamp Multi-Level Inverter
UPS	-	Uninterruptible Power Supply

## LIST OF SYMBOLS

V	-	Voltage
I	-	Current
S	-	Switch
$v$	-	Velocity

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# CHAPTER 1

## INTRODUCTION

### 1.1 Project Background

A power inverter is a power system or circuit that transfers direct current to alternating current (DC)- (AC). The device or circuit design regulates the input voltage, output voltage, frequency and overall power handling. The inverter DC power supplies provide no energy. A power inverter can be solely electrical or a mixture of electronic and mechanical effects (e.g. rotary equipment). No shift transfer components are used in static inverters. Control inverters are mainly used for electric power applications with high currents and voltages; circuits of a similar role are known as oscillators for electronic signalling with shallow currents and voltages. The inverter may be built as a stand-alone unit or an energy reserve source utilizing separately charged batteries for applications such as solar power. The second principle is whether it is part of a larger circuit such as a power supply or Uninterruptible Power supply. The inverter input DC is in this situation from the rectified AC in the Power Supply Unit when the rectified AC in the UPS and the batteries are used if the power failure is triggered. Different inverter types depend on the shape of the waveform. The inverter produces an ac voltage of dc energy sources and is helpful to control electronics and electrical appliances graded on the ac mains voltage. They have different circuit configurations, efficiencies, advantages and disadvantages. Inversion phases are widely used in the power supplies of switched-mode. The circuits are separated by waveform, frequency and output waveform switching technologies. There are two types of the inverter of roots, the Current Source Inverter and the Voltage Source Inverter. The entry is a new inverter source. This sort of inverter is used in medium voltage industrial applications, which involve high-quality waveforms. But existing inverter outlets are rare. The input is an inverter voltage source. This inverter is used in all applications because its dynamic solution is more



reliable, consistent and quicker. Without de-rating, VSI will control engines. Two-level inverter exhibits many harmonic components in output voltage and must utilize a bulky filter to produce pure sinusoidal voltage waveform. An MLI topology has been presented to address the shortcomings of the two-level inverter. The power transfer regulation causes the input dc voltages to be applied to the output to achieve high voltage levels. During inverter operation, the semiconductor switches can endure reduced voltage tension. Over the past three decades, MLI has been a crucial technology in current electricity conversion systems and have successfully been implemented in medium and high voltage applications. Multilevel inverters have recently been explored and evolved even higher. However, research and development are still ongoing, and more modern multilevel circuit inverter topologies have recently been presented.

## **1.2 Problem Statement**

Lately, multilevel inverters (MLIs) are increasingly focusing on both architectures and control strategies. MLI has many benefits compared to traditional two-tier inverters, including versatile operation, higher performance efficiency, lower harmonic distortion, lower electromagnetic interference and lower power switch tension. The multilevel inverters are preferred for extending the electrical transfer of energy in high power applications by resolving the two-level inverter limitations.

MLIs, though, have some significant restrictions. One of the drawbacks is that the amount of necessary semiconductor control switches would exponentially increase with a more considerable number of output voltage levels. The growing number of semiconductor switches has a detrimental influence on overall system performance and reliability. Therefore, MLI topology with reduced components is needed. It is undeniable that a significant range of modern multilevel inverters has recently been proposed with reduced features. However, comprehensive literature found that most of them had some problems, such as a high total TVB and inflexible structure of the dc sources in symmetrical and asymmetrical configurations.

This research work aims to compare a Seven Levels Symmetric H-Bridge MLI with Cascaded H-Bridge MLI in terms of AC output Voltage Levels, AC output current, number of switches, THD, and Voltage stress at switches.

### **1.3 Objectives of Research**

The main aims of this research are:

- i. To compare the number of semi-conductor switches between Seven Levels Symmetric H-Bridge MLI and Cascaded H-Bridge MLI.
- ii. To discuss both topology on the basis of various parameters such as voltage levels, Ac output current, number of switches, THD level and voltage stress at switches.

### **1.4 Scope of Research**

- i. Seven Level MLI with different topology which is Seven Levels Symmetric H-Bridge MLI and Cascaded H-Bridge MLI is designed and developed.
- ii. Design SPWM with Alternate Phase Opposition Disposition-Pulse Width Modulation (APOD-PWM) switching scheme.
- iii. Both topology is to be designed by using the MATLAB/Simulink Software as a verification and simulation tool.

## 1.5 Organization of Report

This thesis consists of five chapters described as follows:

- Chapter 2 : The conventional multilevel converter topologies, their operating concepts and contrasts are discussed. The advantages and limitations of these literature-based topologies are also presented for each inverter. Terminology and evaluation MLIs are addressed briefly. It also presents multilevel inverter topologies and their qualitative analysis. It includes the merits and merits of the various inverter topologies
- Chapter 3 : This section details the circuits and modes of operation for the Seven Levels Symmetric H-Bridge Multilevel Inverter and Cascaded H-Bridge Multilevel Inverter. The values of various parameters such as voltage levels, Ac output current, Ac output voltage, number of switches, THD level and voltage stress at switches is defined.
- Chapter 4 : Demonstrate simulation results using both topologies of the multilevel inverter. Simulation circuit is often addressed to illustrate the efficiency of the multilevel inverter topology suggested. The results are analysed and compared for various parameters.
- Chapter 5 : The findings on results are discussed based on the objectives and Scope of this project. The conclusion on the overall effect is briefly explained and concluded along with a future recommendation for this project.

## REFERENCES

- Babaei, E., & Hosseini, S. H. (2008). New multilevel converter topology with minimum number of gate driver circuits. *2008 international symposium on power electronics, electrical drives, automation and motion* (pp. 792–797). IEEE. <https://doi.org/10.1109/SPEEDHAM.2008.4581263>
- Bahravar, S., Babaei, E., & Hosseini, S. H. (2012). New cascaded multilevel inverter topology with reduced variety of magnitudes of dc voltage sources. *2012 IEEE 5th India international conference on power electronics* (pp. 1-6). IEEE. <https://doi.org/10.1109/IICPE.2012.6450408>
- Chulan, M. A., & Mohammed Yatim, A. H. (2014). Design and implementation of a new H-bridge multilevel inverter for 7-level symmetric with less number of switches. *2014 IEEE international conference on power and energy* (pp. 348-353). IEEE. <http://doi.org/10.1109/PECON.2014.706249>
- Chulan, M. A., Abdul Aziz, M. J., Mohammed Yatim, A. H., & Daud, M. Z. (2017). Seven levels symmetric H-bridge multilevel inverter with less number of switching devices. *International Journal of Power Electronics and Drive Systems*, 8(1), 109–116. <http://doi.org/10.11591/ijpeds.v8.i1.pp109-116>
- Dekka, A., Ramezani, A., Ounie, S., & Narimani, M. (2019). A new 5-level voltage source inverter. *2019 IEEE applied power electronics conference and exposition* (pp. 2511–2515). IEEE. <https://doi.org/10.1109/APEC.2019.8721809>
- Hosseinzadeh, M. A., Sarbanzadeh, M., Sarbanzadeh, E., Rivera, M., & Gregor, R. (2018). Back-to-back modified T-type half-bridge module for cascaded multilevel inverters with decreased number of components. *2018 IEEE international conference on electrical systems for aircraft, railway, ship propulsion and road vehicles and international transportation electrification conference* (pp. 6–11). IEEE. <https://doi.org/10.1109/ESARS-ITEC.2018.8607596>
- Kamaldeep, & Kumar, J. (2016). A new cross switched cascaded multilevel inverter topology with reduced number of switches. *2016 IEEE 7th power India international conference* (pp. 1-6). IEEE. <https://doi.org/10.1109/POWERI.2016.8077426>

- Kamani, P. L., & Mulla, M. A. (2016). A new multilevel inverter topology with reduced device count and blocking voltage. *2016 IEEE 16th international conference on environment and electrical engineering* (pp. 3–8). IEEE. <https://doi.org/10.1109/EEEIC.2016.7555722>
- Kashid, V. B., Jadhav, H. T., & Thorat, A. R. (2016). An improving feasibility and performance of multilevel inverter using battery balancing unit. *2016 international conference on circuit, power and computing technologies* (pp. 1-6). IEEE. <http://doi.org/10.1109/ICCPCT.2016.7530366>
- Ling, Z., Zhang, Z., Li, Z., & Li, Y. (2016). State-of-charge balancing control of battery energy storage system based on cascaded H-bridge multilevel inverter. *2016 IEEE 8th international power electronics and motion control conference* (pp. 2310–2314). IEEE. <http://doi.org/10.1109/IPEMC.2016.7512657>
- Luciano, C., Aganah, K. A., Ndoye, M., & Oni, B. (2018). New switched-multi-source inverter topology with optimum number of used switches. *2018 IEEE PES/IAS PowerAfrica* (pp. 414–419). IEEE. <https://doi.org/10.1109/PowerAfrica.2018.8521070>
- Nik Ismail, N. F., & Hashim, N. (2021). Analysis of different levels for generalized multilevel current source inverter (MCSI) with different SPWM methods. *2021 IEEE international conference in power engineering application* (pp. 24–29). IEEE. <http://doi.org/10.1109/ICPEA51500.2021.9417855>
- Prem, P., & Bharanikumar, R. (2018). A new multilevel inverter topology with reduced switch count for domestic solar PV units. *International Journal of Innovative Technology and Exploring Engineering*, 8(2), 127–131.
- Rahman, M. M., Hossain, S., & Rezwan, S. (2019). Seven-level cascaded H-bridge inverter and fault-tolerant control strategy. *2019 2nd international conference on innovation in engineering and technology* (pp. 23–24). IEEE. <http://doi.org/10.1109/ICIET48527.2019.9290714>
- Sahoo, R., Kasari, P. R., Mishra, M. R., Chakraborti, A., Kumar, A. D., & Das, B. (2018). A seven level cascaded H-bridge inverter topology with reduced sources. *2018 2nd international conference on inventive systems and control* (pp. 655–660). IEEE. <http://doi.org/10.1109/ICISC.2018.8398879>
- Samadaei, E., Sheikholeslami, A., Gholamian, S. A., & Adabi, J. (2018). A square T-type (ST-Type) module for asymmetrical multilevel inverters. *IEEE Transactions on Power Electronics*, 33(2), 987–996.

<https://doi.org/10.1109/TPEL.2017.2675381>

Sujitha, N., & Ramani, K. (2012). A new hybrid cascaded h-bridge multilevel inverter - Performance analysis. *2012 international conference on advances in engineering, science and management* (pp. 46–50). IEEE.

Yarlagadda, A. K., Eate, V. K., Babu, Y. S. K., & Chakraborti, A. (2018). A modified seven level cascaded H bridge inverter. *2018 5th IEEE Uttar Pradesh section international conference on electrical, electronics and computer engineering* (pp. 1-6). IEEE. <http://doi.org/10.1109/UPCON.2018.8597096>



### Appendix A Gantt Chart for FYP 1

ACTIVITIES	FINALY YEAR PROJECT 1 (week)														
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Literature Review	█	█	█	█	█	█	█	█	█	█	█	█	█	█	█
Project synopsis preparation		█	█	█	█										
Submission of project synopsis and approval by supervisor						█									
Submit project synopsis to school s postgraduate							█								
Analyse of simulation results								█	█	█					
Submission of seminar material											█	█			
Presentation of seminar												█	█		
Report preparation and submission													█	█	█

### Appendix B Gantt Chart for FYP2

ACTIVITIES	FINALY YEAR PROJECT 2 (week)														
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Develop Multilevel Inverter Design using Matlab	█	█	█	█	█	█									
Analyse of Matlab result							█	█	█	█	█				
Seminar material preparation										█	█	█	█		
Submission of seminar material													█		
Presentation of seminar														█	
Project report writing						█	█	█	█	█	█	█	█	█	
Submission of Final report															█