# CHARACTERIZATION OF NANOSHEET TRANSISTOR LOGIC AND ITS PERFORMANCE

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CHARACTERIZATION OF NANOSHEET TRANSISTOR LOGIC AND ITS PERFORMANCE

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# DEDICATION

This thesis is dedicated to my beloved family.

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# ABSTRACT

Considering Moore's law requires transistor scaling, we have now entered the nanoscale era, which brings with it new challenges. Fin-shaped Field-Effect Transistors (FinFETs), the current transistor technology, is not up to the challenge when we descend below the 7 nm scale. The short channel effect downgrades the system performance and reliability as the MOSFET is scaled down further. For 5 nm technology node and beyond, nanosheet FET (NSFET) is an alternative architecture that compensates for this limitation due to superior short channel control at a smaller footprint. NSFET can give more effective width, and therefore current, by stacking nano sheet atop one another. In this project, the research gap and past efforts on showing the superiority of NSFET over FinFET were discussed. Using the Sentaurus tool from Synopsys, a three-stacked NSFET 3D structure with sheet thickness of 7nm was created and characterised. The NSFET is being build based on the parameters as per suggested from the reference. The simulation is being validated to the reference. This work is focus on the characteristic of a p-channel NSFET and the analog parameters of the NSFET. Simulation of the electrical characteristics for the NSFET includes current voltage characteristics and extract the electrical parameters such as threshold voltage (Vt), ON-current (Ion), OFF-current (Ioff) ON-OFF current ratio (Ion/Ioff), subthreshold slope (SS), transconductance (gm) and output resistance (Ro). The data collected to be utilised to develop NSFET circuits A p-type and n-type NSFET is being combined to build an inverter. Under the same footprint, NSFETs are expected to have superior current drivability and gate-to-channel controllability than FinFETs, resulting in higher intrinsic gain for circuit applications.

# ABSTRAK

Dalam pertimbangan undang-undang Moore memerlukan penskalaan transistor, kami kini telah memasuki era skala nano, yang membawa bersamanya cabaran baharu. Transistor Kesan Medan berbentuk sirip (FinFETs), teknologi transistor semasa, akan menghadapi cabaran apabila kita turun di bawah skala 7 nm. Kesan saluran pendek menurunkan prestasi dan kebolehpercayaan sistem apabila MOSFET diperkecilkan lagi. Untuk nod teknologi 5 nm dan seterusnya, nanosheet FET (NSFET) adalah seni bina alternatif yang mengimbangi had ini, disebabkan kawalan saluran pendek yang unggul pada jejak yang lebih kecil. NSFET boleh memberikan lebih banyak Weff, dan oleh itu terkini, dengan menyusun helaian nano atas satu sama lain. Dalam projek ini, jurang penyelidikan dan usaha lepas untuk menunjukkan keunggulan NSFET berbanding FinFET telah dibincangkan. Menggunakan Sentaurus daripada Synopsys, struktur 3D NSFET tiga susunan dengan ketebalan kepingan 7nm telah dicipta dan dicirikan. NSFET dibina berdasarkan parameter seperti yang dicadangkan daripada rujukan. Simulasi tersebut disahkan berbanding dengan rujukan. Kerja ini memberi tumpuan kepada ciri NSFET saluran p dan parameter analog NSFET. Simulasi ciri elektrik untuk NSFET termasuk ciri voltan semasa dan mengekstrak parameter elektrik seperti voltan ambang (Vt), arus ON (Ion), arus OFF (Ioff) nisbah arus ON-OFF (Ion/Ioff), subambang. cerun (SS), transkonduktans (gm) dan rintangan keluaran (Ro). Data yang dikumpul untuk digunakan untuk membangunkan litar NSFET NSFET jenis p dan jenis n sedang digabungkan untuk membina penyongsang. Di bawah jejak yang sama, NSFET dijangka mempunyai kebolehgerakan arus yang unggul dan kebolehkawalan pintu ke saluran berbanding FinFET, menghasilkan keuntungan intrinsik yang lebih tinggi untuk aplikasi litar.

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# CHAPTER 1

# INTRODUCTION

This chapter will discuss about the introduction of the project including project background, problem statement, objectives and scope of study of the project.

## 1.1 Problem Background

The current microprocessor is one of the most complicated systems in the world, but, inside this complicated system is only the very simple device, which is the transistor. In today's microprocessors, there are billions of them, and they're practically all the same. As a result, the most basic approach to make microprocessors and the computers work better and less power consumption is to improve their performance and density. Nowadays, Moore's Law no longer has a clear physical definition, although it does indicate the degree to which integrated circuit features and devices are downsized.

Since the invention in 1959, the metal oxide semiconductor field-effect transistor, or MOSFET, the type of transistor used in microprocessors has included the same basic structures: the gate stack, the channel region, the source electrode, and the drain electrode, despite changes in shape and materials. We need both the n-type and p-type transistors of the CMOS technology to build up today’s computer chips.[1][27][28]

On the other hand, making smaller and better transistors is growing more difficult and costly. When we get below the 7nm size, fin-shaped Field-Effect Transistors (FinFETs), a transistor technology that has been used in the industry since

2011, are no longer up to the task [1]. Figure 1.1 displays the three-dimensional construction of a FinFET device, in which the gate surrounds the channel region on three sides, providing better control and preventing current leakage as compared to a planar transistor.

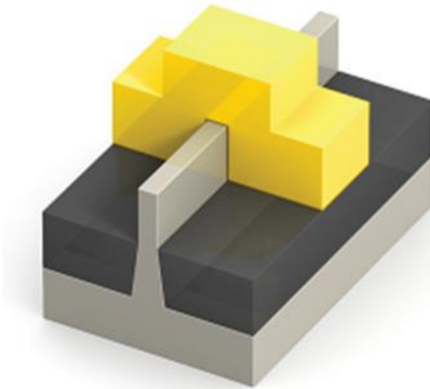

Figure 1.1 3D structure of FinFET device [1]

There is always a trade-off, more width allows you to drive more current and turn off a transistor more quickly, but this also leads to a more complex and costly manufacturing procedure. In a planar device, you can achieve this trade-off by altering the channel shape. Fins, on the other hand, do not provide as much flexibility. Metal interconnects that connect transistors together to construct circuits are built in layers above the transistors. Another drawback of the FinFET is that the gate only surrounds the rectangular silicon fin on three sides, leaving the bottom side connected to the silicon body. When the transistor is turned off, some leakage current can flow. Many experts believed that, to complete control over the channel region, the gate required to entirely enclose it. [1][29][30]

From here, Nano Sheet FET (NSFET) comes into the picture as to compensate the weakness of FinFET. The nanosheet structure is a good candidate to replace FinFET at the 5 nm technology node and beyond. [2][25][26] It offers more Weff per active footprint and better performance than FinFET, as well as a simpler modelling method based on EUV lithography [1]. NSFETs can produce more Weff and consequently current by stacking nanosheets on top of one another, as seen in Figure 1.2. The gate must completely wrap the channel region to gain absolute control over it, as seen in the NSFET device structure in Figure 1.2. The gate now surrounds the channel regions from all sides completely, providing even better control than the FinFET. NSFETs are expected to have better current drivability and gate-to-channel controllability than FinFETs in the same footprint, resulting in higher intrinsic gain for circuit applications, which is the focus of this research.

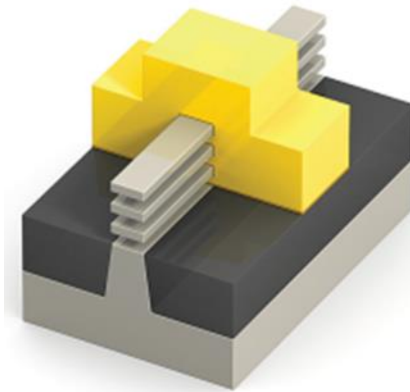

Figure 1.2 3D structure of a stacked Nano Sheet FET (NSFET) [1]

## 1.2 Problem Statement

NSFET devices in the 7nm and below nodes have been the subject of numerous studies. NSFET's applicability had already been proved in previous experiments on a variety of device configurations. However, there is a knowledge gap in this area since additional research into the electrical circuit parameters of NSFETs is required. From the literature, we could see that the researchers mostly discuss on the n-channel NSFETs, there are less study on the p-channel as there are still a lot on study going on. The research will mainly focus on p-channel NSFET as there are the similar research study on n-channel NSFET. Characterization of p-channel NSFET is done in the study.

## 1.3 Research Objectives

The objectives of the research are:

(a) To generate the NSFET device structure (n-channel, p-channel)

(b) To study the characteristic of a p-channel NSFET

(c) To analyse the analog parameters of NSFET

(d) To build the NSFET-based inverter

## 1.4 Research Scopes

This research focuses on the analysis of electrical properties of NSFET based circuit. The research scopes of this study are listed as follows:

a) Generate the NSFET devices with 3 stacks of Nano Sheet and device parameters as suggested in previous study.

b) Simulation of the electrical characteristics for the NSFET includes current-voltage characteristics and extract the electrical parameters such as threshold voltage (Vt), ON-current (Ion), OFF-current (Ioff) ON-OFF current ratio (Ion/Ioff), subthreshold slope (SS), transconductance (gm) and output resistance (Ro).

c) Build of inverter with the n-channel and p-channel NSFET

## 1.5 Report Outline

There are five chapters in this report. In Chapter 1, there have include project introduction, problem background, problem statement, research objectives, study scopes and report outline. The literature review on the FinFET's limitations and NSFET's strengths based on device and circuit performance on the 10 nm and lower manufacturing nodes of prior work studies will be discussed in Chapter 2.

In Chapter 3, the research approach for building an NSFET device's structure, validating, and simulating both the device and inverter, as well as project planning, will be detailed. The major tool for conducting the designs and simulations is also covered in this chapter. In Chapter 4, the result and discussion work are presented. Finally, Chapter 5 presents the research's conclusion and future recommendations.

## REFERENCES


[1] Ye, Peide, Thomas Ernst, and Mukesh V. Khare. "The last silicon transistor: nanosheet devices could be the final evolutionary step for Moore's Law." IEEE Spectrum 56.8 (2019): 30-35.

[2] Loubet, N., et al. "Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET." 2017 Symposium on VLSI Technology. IEEE, 2017.

[3] Choi, Yunho, et al. "Simulation of the effect of parasitic channel height on characteristics of stacked gate-all-around nanosheet FET." Solid-State Electronics 164 (2020): 107686.

[4] G. Chalia and R. S. Hegde, "Study of Self-Heating Effects in Silicon Nano-Sheet Transistors," 2018 IEEE International Conference on Electron Devices and Solid State Circuits (EDSSC), 2018, pp. 1-2, doi: 10.1109/EDSSC.2018.8487097.

[5] Bardon, M. Garcia, et al. "Dimensioning for power and performance under 10nm: The limits of FinFETs scaling." 2015 International Conference on IC Design & Technology (ICICDT). IEEE, 2015.

[6] Divakaruni, Rama, and Vijay Narayanan. "(Keynote) Challenges of 10 nm and 7 nm CMOS for Server and Mobile Applications." ECS Transactions 72.4 (2016): 3.

[7] Razavieh, A., et al. "Scaling challenges of FinFET architecture below 40nm contacted gate pitch." 2017 75th Annual Device Research Conference (DRC). IEEE, 2017.

[8] Das, Uttam Kumar, and Tarun Kanti Bhattacharyya. "Opportunities in device scaling for 3-nm node and beyond: FinFET versus GAA-FET versus UFET." IEEE Transactions on Electron Devices 67.6 (2020): 2633-2638.

[9] Mohan, Chander, Sumit Choudhary, and B. Prasad. "Gate all around FET: An alternative of FinFET for future technology nodes." Int. J. Adv. Res. Sci. Eng. 6.7 (2017): 563-569.

[10] Yoon, Jun-Sik, et al. "Systematic DC/AC performance benchmarking of sub-7-nm node FinFETs and nanosheet FETs." IEEE Journal of the Electron Devices Society 6 (2018): 942-947.

[11] Sikder, Orthi, and Peter J. Schubert. "First Principle and NEGF Based Study of Silicon Nano-wire and Nano-sheet for Next Generation FETs: Performance, Interface Effects and Lifetime." 2020 IEEE 20th International Conference on Nanotechnology (IEEE-NANO). IEEE, 2020.

[12] Yoon, Jun-Sik, and Rock-Hyun Baek. "Device design guideline of 5-nm-Node FinFETs and nanosheet FETs for analog/RF applications." IEEE Access 8 (2020): 189395-189403.

[13] Jegadheesan, V., K. Sivasankaran, and Aniruddha Konar. "Impact of geometrical parameters and substrate on analog/RF performance of stacked nanosheet field effect transistor." Materials Science in Semiconductor Processing 93 (2019): 188-195.

[14] Razavieh, Ali, et al. "Effective drive current in scaled FinFET and NSFET CMOS inverters." *2018 76th Device Research Conference (DRC)*. IEEE, 2018.

[15] Valasa, Sresta, Shubham Tayal, and Laxman Raju Thoutam. "Optimization of design space for vertically stacked junctionless nanosheet FET for Analog/RF applications." *Silicon* (2022): 1-10.

[16] Kumar, Priyesh, Sarita Yadav, and Pankaj Kumar Pal. "Analysis of Nanosheet Field Effect Transistor (NSFET) for device and circuit perspective." *2019 Women Institute of Technology Conference on Electrical and Computer Engineering (WITCON ECE)*. IEEE, 2019.

[17] Yoon, Jun-Sik, et al. "Sensitivity of source/drain critical dimension variations for sub-5-nm node fin and nanosheet FETs." *IEEE Transactions on Electron Devices* 67.1 (2019): 258-262.

[18] Tayal, Shubham, et al. "Investigation of Nanosheet-FET Based Logic Gates at Sub-7 nm Technology Node for Digital IC Applications." *Silicon* (2022): 1-7.

[19] Neelam, Aruna Kumari, and P. Prithvi. "Performance Evaluation of GAA Nanosheet FET with Varied Geometrical and Process Parameters." (2021).

[20] Banchhor, Shashank, et al. "A new aspect of saturation phenomenon in FinFETs and its implication on analog circuits." *IEEE Transactions on Electron Devices* 66.7 (2019): 2863-2868.

[21] Valasa, Sresta, Shubham Tayal, and Laxman Raju Thoutam. "Optimization of design space for vertically stacked junctionless nanosheet FET for Analog/RF applications." *Silicon* (2022): 1-10.

[22] Yoon, Jun-Sik, and Rock-Hyun Baek. "A novel sub-5-nm node dual-workfunction folded cascode nanosheet FETs for low power mobile applications." *IEEE Access* 8 (2020): 196975-196978.

[23] Miyata, T., et al. "150 GHz FMAX with high drain breakdown voltage immunity by multi gate oxide dual work-function (MGO-DWF)-MO SFET." *2015 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2015.

[24] Lee, H-J., et al. "Implementation of high power RF devices with hybrid workfunction and OxideThickness in 22nm low-power FinFET technology." *2019 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2019.

[25] Bangsaruntip, Sarunya, et al. "High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling." *2009 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2009.

[26] Mertens, Hans et al. “Vertically stacked gate-all-around Si nanowire CMOS transistors with dual work function metal gates.” *2016 IEEE International Electron Devices Meeting (IEDM)* (2016): 19.7.1-19.7.4.

[27] Thompson, Scott E., et al. "A 90-nm logic technology featuring strained-silicon." *IEEE Transactions on electron devices* 51.11 (2004): 1790-1797.

[28] Khatami, Yasin, and Kaustav Banerjee. "Steep subthreshold slope n-and p-type tunnel-FET devices for low-power and energy-efficient digital circuits." IEEE transactions on electron devices 56.11 (2009): 2752-2761.

[29] Buitrago, Elizabeth, et al. "The top-down fabrication of a 3D-integrated, fully CMOS-compatible FET biosensor based on vertically stacked SiNWs and FinFETs." *Sensors and Actuators B: Chemical* 193 (2014): 400-412.

[30] Chen, Li, and Douglas M. Gingrich. "Study of N-channel MOSFETs with an enclosed-gate layout in a 0.18/spl mu/m CMOS technology." *IEEE Transactions on Nuclear Science* 52.4 (2005): 861-867.