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The Effect of Channel Variation for Long Channel GaAs Junctionless Gate-All-Around Transistor

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Since the Moore era, the use of advanced nanomaterial device architecture has been introduced to improve its electrical performance. This paper reports on the study of performance of a long channel gallium arsenide (GaAs) nanowire Junctionless Gate-All-Around (JGAA) transistor, including the quantum mechanical effect. In order to include the quantum mechanical effect, the Poisson density gradient model is used to conduct the analysis. Therefore, the channel radius (R_{chn}), oxide thickness (T_{OX}) and carrier concentration (N_d) were varied to study the electrical performances of the proposed device. Through simulation, it was found that the on-current (I_{on}) increases significantly by 54 % with a smaller oxide thickness and channel radius. This paper also highlights the drawback of the classical model, in which it is impossible to capture the quantum effect, where the current deviations show a 12 % difference between the classical model and the quantum model. The results presented here indicate the possibility of using JGAA transistor for future nanoelectronic device application.

Keywords: Short channel effects, Quantum mechanical effects, Advanced material and structure.

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1. INTRODUCTION

For decades, the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has become the core building block for all electronic devices. A tremendous demand in electronic appliances due to massive economic growth has enforced to provide a high-quality product with higher processing speed, smaller size and low power consumption devices. This evolution has led to follow the Moore's Law, which states that the number of transistors will double every two years on a single chip [1]. However, as the channel length of the transistor has reached a nanoscale dimension, there are several issues that need serious attention as many performances of the device start to exhibit electrical degradation [2]. Therefore, new structures and materials were introduced as an alternative to overcome this problem following the guideline provided by International Roadmap for Devices and Systems (IRDS) such as FinFET, gate-all-around, carbon nanotube, III-V materials and graphene [3-8].

The Gate-All-Around (GAA) transistor is considered the best structure among multigate devices where it can be used to effectively control electrostatic electricity with less short channel effects (SCEs), and it is also expected to replace the FinFET transistor in the semiconductor industry in 2021. For example, Sachdeva et al. [9] showed GAA MOSFET as a promising solution as it can reduce SCEs and improve the device reliability. In another work, Jena et al. [10] revealed that a cylindrical architecture with a surrounded gate encapsulating the channel body provides better gate control. Due to their advantages in electrical performance, GAA structures have been extended to the Junctionless MOSFET. Recent research on nanoelectronic devices has also been devoted to junctionless transistors [11]. This is due to the simpler process involved in the fabrication, as well as use of a simple architecture. Essentially, the Junctionless transistor operated with a uniform heavily doped source, channel and drain. These architectures have proven that they could improve the on-current and high early voltage [12]. It has many advantages such as no *p-n* junction which makes the structure simple, eliminates the doping concentration gradient and produces better SCEs.

III-V materials are predicted to be a good candidate to replace silicon. IRDS has mentioned that this kind of material will be used in future nanoelectronic devices [13]. III-V materials such as GaAs have aggressively been developed due to their unique properties to enhance device dimensions [14]. In addition, III-V materials are also capable in reducing the tunnelling current due to it higher mobility. In addition, it also can increase the drive current. Numbers of researchers have shown the flexibility to design III-V materials as channel and produce high performance transistor [15-17]. Nevertheless, III-V devices suffer from SCEs. As a solution, 3D devices such as GAA can be used. Since the GAA structure is recognized as a device with good electrostatic control, III-V materials incorporation in GAA devices can further improve its electrical performance such as the drive current (I_{on}), threshold voltage (V_{th}) and current ratio (I_{on}/I_{off}).

Therefore, in this paper, performance of a long channel GaAs Junctionless Gate-All-Around (JGAA) transistor is assessed based on the inclusion of Quantum Mechanical Effect (QME). In the simulator, a drift-diffusion transport model in combination with a quantum potential solver such as the density-gradient model was used to define the quantum effect. The simulated result was studied in terms of its physical variation such as the channel radius (R_{chn}), oxide thickness (T_{OX}) and doping concentration (N_d). It should be noted that

the quantum effects are essential at a thinner channel radius and an oxide thickness approximately less than 10 nm [18, 19]. Therefore, it is important here to vary the physical parameters in order to study the effects on the electrical performances. Neglecting this effect may cause inaccuracy in describing the quantization effect and would cause misinterpreting the data characterization. This effect is likely to occur in both short and long channel devices. The electrical characteristic is computed to evaluate the electrical parameters focusing on the threshold voltage (V_{th}), drive current (I_{on}) and (I_{off}). In the next section, the process and device structure development are described in detail.

2. DEVICE STRUCTURE AND SIMULATION MODEL

The schematic diagram of the GaAs JGAA MOSFET structure used in this simulation is shown in Fig. 1 and Fig. 2. The 3D schematic diagram and cross-sectional view of the GaAs JGAA transistor with a cylindrical cross section can be seen in Fig. 1 and Fig. 2, respectively. Table 1 shows the list of parameters used in the simulation. The simulation is carried out with the Sentaurus device simulator, a simulator from Synopsis TCAD. Sentaurus can analyze and predict the behavior of devices without requiring any cost to manufacture the real device. The gate length L_G is fixed at 100 nm which can be considered as long channel devices according to IRDS specifications for the technology node used. Silicon dioxide is used as the dielectric material. The metal gate work function of 4.8 eV is applied to the metal gate. The performance variations of the JGAA transistor strongly depends on the doping concentration where the doping level must be higher. The parameters that will be varied to analyze the performance are the channel radius (R_{chn}), oxide thickness (T_{OX}) and doping concentration (N_d). Since the cross-section of the device is smaller and a higher doping level is applied, the quantum effect must be considered in the simulator. We consider the solution of the drift-diffusion and density gradient model in the simulator without ignoring the quantum effect. The current-voltage characteristic of the GaAs JGAA MOSFET is extracted and discussed in section 3.

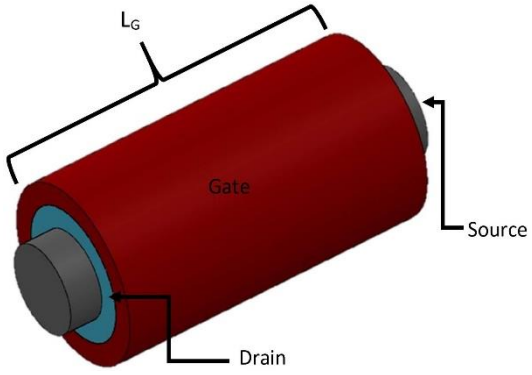

Fig. 1 – Schematic structure of GaAs JGAA MOSFET

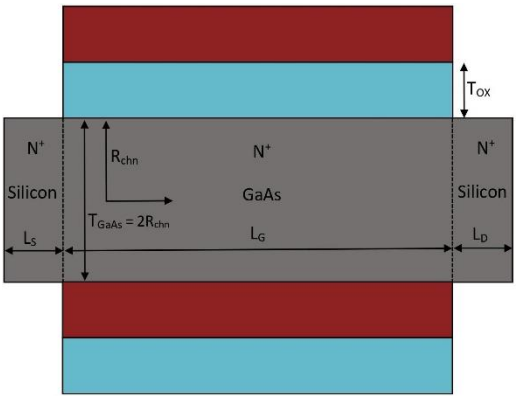

Fig. 2 – 2D cross-sectional view of GaAs JGAA MOSFET

Table 1 – Parameters used for the simulation

Parameter symbol	Technology parameter	Value
L_G	Gate length	100 nm
R_{chn}	Channel radius	4-10 nm
T_{GaAs}	GaAs film thickness	$2R_{chn}$
T_{OX}	Oxide thickness	2-14 nm
N_d	Impurity doping concentration for source, drain and channel	1×10^{18}-1×10^{19} cm^{-3}

3. RESULTS AND DISCUSSION

In this section, the analysis was done to study the device performance on the long channel GaAs JGAA MOSFET without neglecting the quantum effect. The density gradient model was used to present the quantum effect in the simulator. To validate the importance of including quantum effects, the comparison between the classical model and the quantum model was conducted, as illustrated in Fig. 3. Fig. 3 shows the comparison of the current-voltage (I-V) characteristics between these two models on long channel GaAs JGAA MOSFET using the following parameters: $L_G = 100$ nm, $R_{chn} = 5$ nm, $T_{OX} = 2$ nm and $N_d = 1 \times 10^{19}$ cm^{-3}. Based on Fig. 3, it is found that the classical model is not able to capture the quantum effect on the device channel. The current deviations between the classical (drift-diffusion) model and the quantum mechanical (density gradient) model are estimated as 12 %. This result shows the inaccuracy of the classical model to interpret the carrier charge moving along the channel. A similar trend has been proven by Vimala et al. [20]. The result demonstrated here shows the necessity to include the quantum effect when applying a smaller channel radius and thinner oxide thickness.

Further studies were carried out on the DC performance of GaAs JGAA MOSFET to estimate the device characteristics specifically on the on-current, threshold voltage and I_{on}/I_{off} ratio. Our TCAD results take into account the quantum effect to describe accurately the electrical behaviors and measure our device limits. The I_d-V_g curves in the saturation region of the GaAs JGAA transistor for two sets of radii, $R_{chn} = 4$ nm and 8 nm,

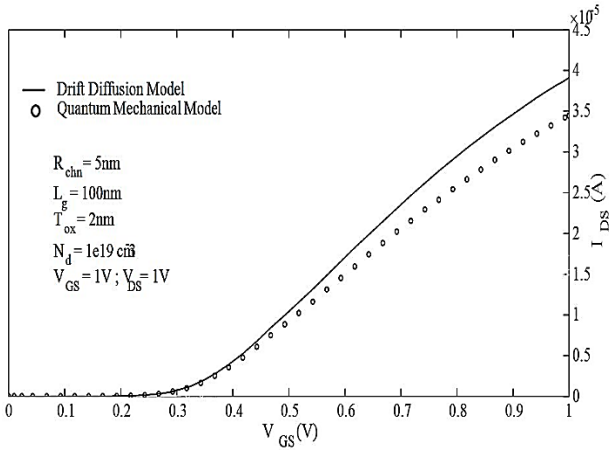

Fig. 3 – *I-V* characteristics in comparison between the classical (drift-diffusion) model and the quantum mechanical (density gradient) models in GaAs JGAA MOSFET

were chosen using two different oxide thicknesses which are 2 and 14 nm, respectively, while keeping the doping level constant at 1×10^{19} cm^{-3} (Fig. 4). The on-current for $T_{OX} = 2$ nm is approximately 54 % higher compared to $T_{OX} = 14$ nm for both $R_{chn} = 4$ nm and $R_{chn} = 8$ nm. By varying the oxide thickness, the value of the on-current is noted to be higher with decreasing the oxide thickness. We note that the oxide thickness should be reduced with decreasing the channel length to have lower SCEs.

To further evaluate the electrical performance, the value of V_{th} is extracted. The plot indicates that when larger gate oxide is applied, it will induce a greater threshold voltage roll-off. As the oxide thickness changes from 14 to 2 nm, the threshold voltage increases. The gate loses control over the channel when the gate oxide thickness increases. It will resist the electric field from the gate into the channel resulting in degradation of threshold behavior. Hence, to avoid this, a thin gate oxide is required. This may lead to better performances, but very small oxide thickness cannot be obtained because direct tunnelling through very thin oxide becomes noticeable.

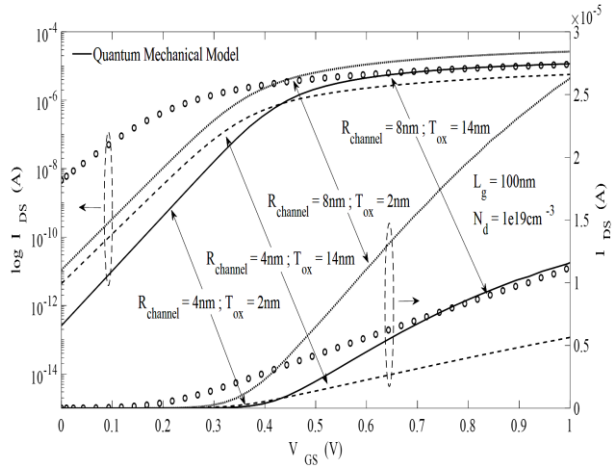

Fig. 4 – Comparison of I_d-V_g for different channel radii with two sets of oxide thicknesses of 100 nm GaAs JGAA MOSFET

Fig. 5 shows the effect of varying the channel radius at fixed $L_G = 100$ nm and $T_{OX} = 2$ nm. As can be seen from Fig. 5, the on-current increases while the threshold voltage of GaAs JGAA MOSFET decreases when the channel radius increases. The same figure shows increment on the on-current by 55 % from $R_{chn} = 5$ nm to $R_{chn} = 10$ nm. As the radius increases, the enhancement of I_{on} is observed due to the larger volume of the channel, allowing more current to flow. Moreover, the unique properties of GaAs, which has higher mobility in the gate region, help to boost the number of electrons moving through the channel. There is a remarkable decrease in V_{th} with decreasing channel radius from 10 to 5 nm. In contrast, I_{on} increases while I_{off} slightly increases that results in higher I_{on}/I_{off} ratio as we change the nanowire radius. As the channel radius was reduced, this may contribute to the quantum effect.

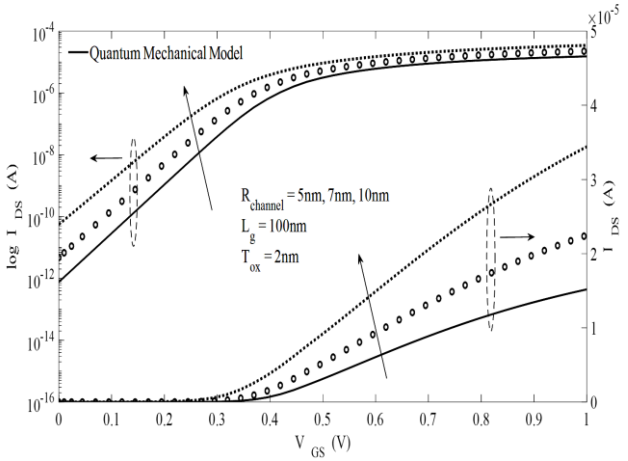

Fig. 5 – Comparison of I_d-V_g for different channel radii with two sets of oxide thicknesses of 100 nm GaAs JGAA MOSFET

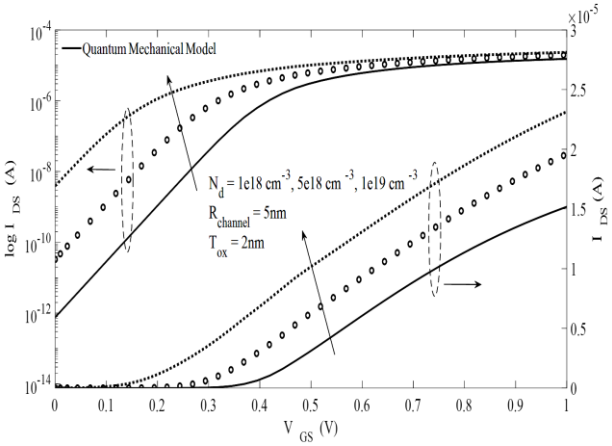

Fig. 6 – Comparison of I_d-V_g for different doping levels of 100 nm GaAs JGAA MOSFET

Fig. 6 shows the I_d-V_g characteristics for different doping levels of GaAs JGAA MOSFET. The following parameters: $L_G = 100$ nm, $T_{OX} = 2$ nm, $R_{chn} = 5$ nm were considered to study the effect of a wide range of doping levels of GaAs JGAA MOSFET. Three sets of doping levels were studied from 1×10^{18} to 1×10^{19} cm^{-3}. It is seen, as the doping level increases, the on-current increases, while the threshold voltage is reduced. For

example, for $N_d = 1 \times 10^{18}$ cm^{-3}, the on-current I_{on} is 1.5×10^{-5} A and the threshold voltage V_{th} is 0.35 V, and for $N_d = 1 \times 10^{19}$ cm^{-3}, the on-current is slightly higher 2.4×10^{-5} A producing smaller $V_{th} = 0.15$ V. The increment reached 37 % for the on-current and about 57 % for the threshold voltage drop. Higher concentration helps to increase the electron mobility, therefore the on-current increases. In addition, the increment of channel doping becomes a catalyst which increases the degree of band bending. Thus, more carriers will be occupied on the channel of the device.

The main contribution of this work is to study the long channel GaAs JGAA transistor including the quantum effect. The analysis indicates that III-V material is one of most promising candidates due to its potential to boost the electrical performances especially on the on-current.

4. CONCLUSIONS

A GaAs Junctionless Gate-All-Around (JGAA) transistor has been studied with a wide range of performance using Sentaurus TCAD tools. In this work, Poisson density gradient solver was used as a transport device in the simulator to show that quantum effect is not neglected. The electrical performances for various types of parameters were tested, such as channel radius, oxide thickness and doping level. The electrical performances include V_{th}, I_{on} and I_{off} and are compared. III-V materials are expected to further enhance the device on-current. This work shows a 54 % increment of the on-current with smaller channel radius and oxide thickness. Further increment of the doping level also provides a 37 % improvement in the on-current with a 57 % decrement of the threshold voltage. The valuable data from the previous work highlights the importance of applying high mobility channel to replace silicon as a promising successor. This work is a preliminary study and more work needs to be done to further evaluate the feasibility of using III-V material as a channel material in advanced transistor architecture.

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Ефект зміни каналу для довгоканального GaAs GAA транзистора без переходів

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Починаючи з епохи Мура, для покращення електричних характеристик було введено використання передової архітектури пристроїв з наноматеріалів. У роботі повідомляється про дослідження характеристик довгоканального GaAs JGAA транзистора, включаючи квантово-механічний ефект. Для включення квантовомеханічного ефекту при проведенні аналізу використовується модель градієнта густини Пуассона. Тому радіус канала (R_{chn}), товщину оксиду (T_{OX}) і концентрацію носіїв (N_d) змінювали для вивчення електричних характеристик пропонованого пристрою. За допомогою моделювання

було виявлено, що струм включення (I_{on}) збільшується на 54 % при менших товщині оксиду та радіусу каналу. У роботі також висвітлюється недолік класичної моделі, в якій неможливо охопити квантовий ефект, де поточні відхилення показують 12 % різницю між класичною моделлю та квантовою моделлю. Наведені тут результати вказують на можливість використання JGAA транзистора для майбутніх додатків наноелектронних пристроїв.

Ключові слова: Короткоканальні ефекти, Квантовомеханічні ефекти, Удосконалений матеріал і структура.