SWITCHED CAPACITOR MULTILEVEL INVERTER USING PWM TECHNIQUE

ABDIRIZAK ABDIHAFID MOHAMED

A thesis submitted in fulfilment of the
requirements for the award of the degree of
Master of Engineering (Electrical Power)

School of Electrical Engineering
Faculty of Engineering
Universiti Teknologi Malaysia

JULY 2021

ACKNOWLEDGEMENT

I would like to thank my supervisor Dr. Shahrin Bin Md. Ayob for his guidance throughout this process, without his support and guidance it would not have been possible to make it until here. Dr. Shahrin was very kind-hearted, was very humble during all this process, and used to give sample time for research and used to correct in many ways so that the research cannot have distracted.

I would like to remember my father who passed away during my first year in this world and my mother in 2002. It was tough to pursue my studies but my beloved uncles Abdullahi and Hassan their blessings kept my nerves to continue although my uncle Abdullahi passed away on 14 July 2007. May Allah bless them all my mother, father and uncle with the highest place in Jannah.

ABSTRACT

For the last decades, the increasing demand for renewable energy resources and their applications of high voltage, multilevel inverter (MLI) become very popular and globally recognized for several industrial applications and it has been under research and development with successful industrial applications due to its capacity to produce high levels of voltage output, low THD, low EMI and reduced switching stress on switching devices. However, renewable energy resources such as solar and wind energy for their output are not always fixed due to changes of their input constantly. To boost their output and to convert into alternate current (AC) at the same time with one circuit, switched capacitor inverter is required. In this project, a Switched-Capacitor multilevel inverter with 7-level output comparing between different kinds of pulse width modulation (PWM) technique namely, phase disposition (PD-SPWM), phase opposition disposition (POD-SPWM), and Alternate phase opposition disposition (APOD-SPWM) has been proposed. The main objectives of this project are to simulate the modelled 7-level switched capacitor multilevel inverter using pulse width modulation technique with different modulation index, to observe the performance of the switching patterns of various switches, output voltage, and FFT analysis of modified multilevel inverter, to perform analysis of the charging and discharging time of the capacitors and to analyze using PD-SPWM for pure resistive load and RL load and step change of load from no load to RL load and from low RL load to high RL load. The proposed topology uses a smaller number of switches and produces less harmonic output voltage using the strategy of pulse width modulation (PWM). To validate the viability of the proposed topography and its strategy of switching, a circuit for seven-level MLI is developed and done in MATLAB/SIMULINK software tool.

ABSTRAK

Selama beberapa dekad yang lalu, permintaan yang semakin meningkat untuk sumber tenaga yang boleh diperbaharui dan penggunaan voltan tinggi, penyongsang pelbagai tahap (MLI) menjadi sangat popular dan diiktiraf di seluruh dunia untuk beberapa aplikasi industri dan telah diteliti dan dikembangkan dengan aplikasi industri yang berjaya kerana kapasitinya untuk menghasilkan output voltan tahap tinggi, THD rendah, EMI rendah dan tekanan tegangan pengurangan pada peranti beralih. Walau bagaimanapun, sumber tenaga boleh diperbaharui seperti tenaga suria dan angin untuk outputnya tidak selalu diperbaiki kerana perubahan input mereka sentiasa. Untuk meningkatkan output mereka dan menukar menjadi arus bolak balik (AC) pada satu masa dengan satu litar, diperlukan penyongsang kapasitor yang diubah. Dalam projek ini, penyongsang bertingkat Kapasitor Beralih dengan output 7 tingkat yang membandingkan antara pelbagai jenis teknik modulasi lebar denyut (PWM) iaitu, disposisi fasa (PD-SPWM), disposisi penentangan fasa (POD-SPWM), dan penentangan fasa Alternatif pelupusan (APOD-SPWM) telah dicadangkan. Objektif utama projek ini adalah untuk mensimulasikan inverter bertingkat bertingkat kapasitor 7 tingkat yang dimodelkan menggunakan teknik modulasi lebar nadi dengan indeks modulasi yang berbeza, untuk memerhatikan prestasi corak pensuisan pelbagai suis, voltan keluaran, dan analisis FFT penyongsang bertingkat bertingkat , untuk melakukan analisis masa pengisian dan pemuatan kapasitor dan untuk menganalisis menggunakan PD-SPWM untuk beban resistif murni dan beban RL dan perubahan langkah dari beban tanpa beban ke beban RL dan dari beban RL rendah ke beban RL tinggi. Topologi yang dicadangkan menggunakan bilangan suis yang lebih sedikit dan menghasilkan voltan keluaran yang kurang harmonik menggunakan strategi modulasi lebar nadi (PWM). Untuk mengesahkan daya maju topografi yang dicadangkan dan strategi penukarannya, rangkaian untuk MLI tujuh peringkat dikembangkan dan dilakukan dalam alat perisian MATLAB / SIMULINK.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

MLI	-	Multilevel Inverter
DC	-	Direct Current
AC	-	Alternate Current
VSI	-	Voltage Source Inverter
CSI	-	Current Source Inverter
EMI	-	Electromagnetic Interference
SCMLI	-	Switched Capacitor Multilevel Inverter
UTM	-	Universiti Teknologi Malaysia
PD	-	Phase Disposition
POD	-	Phase Opposition Disposition
APOD	-	Alternate Phase Opposition Disposition
PWM	-	Pulse Width Modulation
SPWM	-	Sinusoidal Pulse Width Modulation
DCMLI	-	Diode Clamped Multilevel Inverter
FCMLI	-	Flying Capacitor Multilevel Inverter
CMLI	-	Cascaded Multilevel Inverter
SRS	-	Sinusoidal Reference Signal
TRS	-	Trapezoidal Reference Signal
ZSIRS	-	Zero Sequence Injected Reference Signal
PS	-	Phase Shift
IGBT	-	Insulated-gate Bipolar Transistor
GTO	-	Gate Turn-off Thyristor
BJT	-	Bipolar Junction Transistor
MOSFET	-	Metal Oxide Semiconductor Field-effect Transistor
THD	-	Total Harmonic Distortion
PV	-	Photovoltaic
PDS	-	Power distribution Systems

CHAPTER 1

INTRODUCTION

1.1 Problem Background

Multilevel inverter (MLI) topology has played significant interest in renewable energy and power electronics researchers due to its numerous ranges of potentially useful applications and increasing demands of power and efficiency. Many observations have been done in shaping these challenges with continued evolution for the last two decades. The considerations of high dynamic, demanding applications and high power with quality and efficiency of multilevel inverter may become modest clarifications. It is used a wide range of multi-megawatts [1].

Our daily power consumption resources include coal, natural gas, and coal crude oil, one of the most dependable resources for many countries for the last couple of years. Their resources are decreasing day by day with their high consumption. These resources have many environmental problems; for these obstacles, there is a necessary high need for renewable energy resources. Many countries have many potential capabilities of applying renewable energy resources such as solar energy and wind energy. These sources generate direct current (DC) voltage and current for their output. Inverters are required to convert the dc voltages to ac supply.

Inverter topology refers to the conversion from direct current input to alternative current output into pair of cycles. Voltage source inverter (VSI) can be called the inverter when the input is a voltage source. Similarly, when the input is a current source, the inverter is called a current source inverter (CSI). In contrast, a multilevel inverter (MLI) is the inverter used to synthesize desired sinusoidal output voltage from several levels of DC source [2-4]. The sources can be derived from batteries, renewable energy systems, etc.

Due to the lower rating voltage of power semiconductor devices for high voltage generation, small filter size, Lower EMI, improved performance, reduced content of harmonic, and many more, multilevel inverters have their significance in medium and high voltage applications[5]. Figure 1.1 and Figure 1.2 show typical single-phase CSI and VSC circuit diagrams

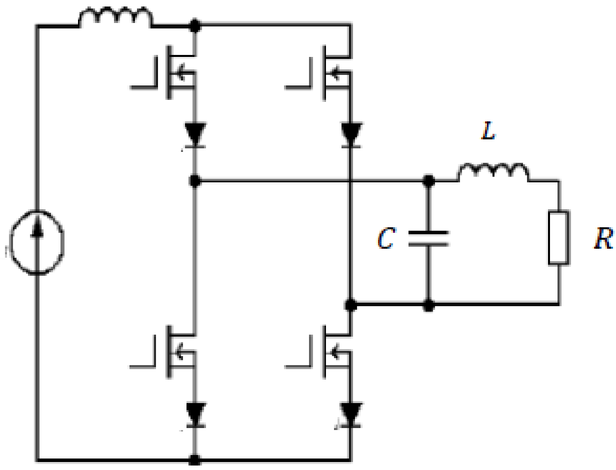


Figure 1.1 Current Source inverter

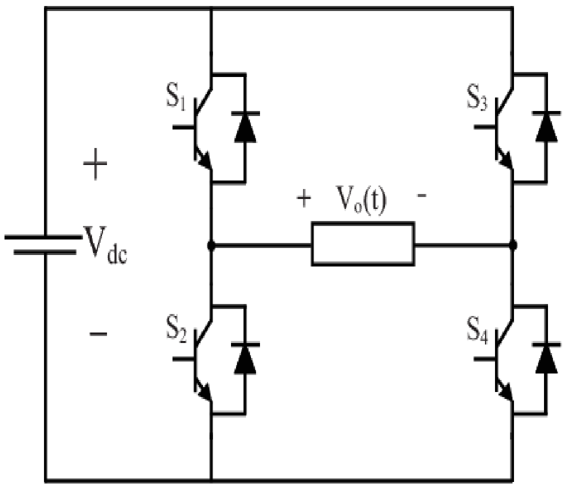


Figure 1.2 Voltage Source inverter

1.2 Multilevel Inverter classification

Mainly multilevel inverters are classified into three main kinds:

a. Cascaded H-Bridge (CHB)
b. Neutral-Point Clamped (NPC)
c. Flying-Capacitor (FC)

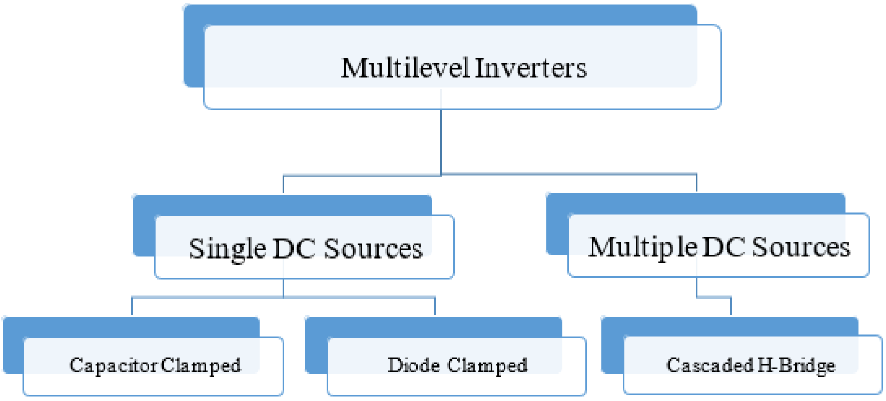


Figure 1.3 Multilevel Inverter classification

1.3 Problem Statement

For the last two decades, with the increasing demand for renewable energy sources and their application in high voltage applications, power electronic converters play a vital role in the suitability of power conversion for each application. Due to the lower rating voltage of power semiconductor devices for high voltage generation, small filter size, Lower EMI, improved performance, reduced content of harmonic, and many more, multilevel inverters have their significance in medium and high voltage applications [5]. The basic principle of MLIs is to generate a staircase voltage waveform near sinusoidal with high power quality. The desired staircase voltage waveform is synthesized using the appropriate combination of different switches, which can reduce the voltage stress of power switches and total harmonic distortion (THD)[6, 7].[8]

The output of some renewable energy resources such as solar and wind energy are not always fixed due to change in their input continuously. For solar energy, the output voltage varies with the temperature and irradiance, while wind energy output voltage varies with the speed of the wind. Hence, there will be a possibility of the output voltage is lower than the utility grid. The conventional multilevel inverter is not able to deal with these problems.

To boost their output and convert into alternate current (AC) simultaneously with one circuit, switched capacitor inverter is required. In this project, a Switched-Capacitor multilevel inverter with 7-level output has been proposed to overcome the aforementioned issues.

1.4 Objectives

The objectives of this study are:

a. To simulate the modelled 7-level switched multilevel capacitor inverter using pulse width modulation technique
b. To observe the performance of the switching patterns of various switches, output voltage, and FFT analysis, to analyze the circuit by using PD-SPWM for both steady-state and transient state of load with capacitor design for seven-level SCMLI.

1.5 Scope of work

The research scopes of this project can be described as below;

a. The focus of this thesis project is about seven-level MLI topology.
b. The modulation strategy that will be used as switching techniques are phase disposition pulse width modulation technique (PD-SPWM),

phase opposition disposition pulse width modulation strategy (POD-SPWM), alternate phase opposition disposition pulse width modulation strategy (APOD-SPWM)

c. The model will be simulated using MATLAB/SIMULINK software.

1.6 Thesis organization

This thesis consists of five chapters that are listed below: -

Chapter 1 presents the fundamental basics of MLI and highlights the reputation of using switched capacitor multilevel inverter.

Chapter 2 discusses the overall view of different multilevel inverter topologies, including merits and demerits. It also presents the discussion of using different pulse width modulation techniques and their total harmonic distortion spectrum.

Chapter 3 focuses on the proposed seven-level switched capacitor multilevel inverter with a thorough, detailed explanation of the principle mode of operation of the proposed circuit and the design of the capacitors. It also provides a detailed concept of level-shifted pulse width modulation techniques that will implement during this thesis project.

Chapter 4 gives the simulation results, which describe the validation of the proposed switched capacitor MLI and the results are analyzed accordingly.

Chapter 5 concludes the thesis with statements that answers the objectives of the research.

REFERENCES

1. Suvetha Poyyamani Sunddararaj, S.S.R., Subashini N, *An Extensive Review of Multilevel Inverters Based on Their Multifaceted Structural Configuration, Triggering Methods and Applications.*
2. Suresh, R.A.K.a.L.P., *A brief review on multi level inverter topologies.* International Conference on Circuit, Power and Computing Technologies (ICCPCT), 2016.
3. S.Ravivarman, M.R.a., *Review on Voltage Balancing Solutions in Multilevel Inverters.* Indonesian journal of electrical engineering and computer science, 2016. **vol.1,No**: p. 53-59.
4. S.Shalini, *Voltage Balancing in Diode Clamped Multilevel.* International Journal of Engineering Trends and Technology (IJETT), 2013. **volume 6,No2**.
5. Siddique, M.D., et al., *A New Single Phase Single Switched-Capacitor Based Nine-Level Boost Inverter Topology With Reduced Switch Count and Voltage Stress.* IEEE Access, 2019. **7**: p. 174178-174188.
6. Rodriguez, J., L. Jih-Sheng, and P. Fang Zheng, *Multilevel inverters: a survey of topologies, controls, and applications.* IEEE Transactions on Industrial Electronics, 2002. **49**(4): p. 724-738.
7. Gupta, K.K., et al., *Multilevel Inverter Topologies With Reduced Device Count: A Review.* IEEE Transactions on Power Electronics, 2016. **31**(1): p. 135-151.
8. Axelrod, B., Y. Berkovich, and A. Ioinovici, *A cascade boost-switched-capacitor-converter - two level inverter with an optimized multilevel output waveform.* IEEE Transactions on Circuits and Systems I: Regular Papers, 2005. **52**(12): p. 2763-2770.
9. Nabae, A., I. Takahashi, and H. Akagi, *A New Neutral-Point-Clamped PWM Inverter.* IEEE Transactions on Industry Applications, 1981. **IA-17**(5): p. 518-523.
10. Riya G. Barapatre1, S.Y.T., Samir D.Landge1, Shubhendu B.Mukherji1 ,, *Design and Implementation of Five Level Diode Clamped Inverter.*

International Journal of Innovations in Engineering and Science, 2019. **Vol. 4, No.7**(Impact Factor Value 4.046).

11. Kumar, R., R.A. Gupta, and K.S. Pratap. *Implementation and Analysis of Five-Level inverter with Space Vector PWM Algorithm*. in *2006 IEEE International Conference on Industrial Technology*. 2006.
12. Bin, W. and N. Mehdi, *Voltage Source Inverter Fed Drives*, in *High-Power Converters and AC Drives*. 2017, IEEE. p. 287-308.
13. Tolbert, L.M., P. Fang Zheng, and T.G. Habetler, *Multilevel converters for large electric drives.* IEEE Transactions on Industry Applications, 1999. **35**(1): p. 36-44.
14. Siddique, M.D. and A. Sarwar. *Performance analysis of carrier based PWM technique for three level diode clamped multilevel inverter with different reference signals*. in *2016 IEEE 7th Power India International Conference (PIICON)*. 2016.
15. Meynard, T.A., et al., *Multicell converters: basic concepts and industry applications.* IEEE Transactions on Industrial Electronics, 2002. **49**(5): p. 955-964.
16. Chang-xin, M., et al., *Flying capacitor multilevel inverters with novel PWM method.* Procedia Earth and Planetary Science, 2009. **1**(1): p. 1554-1560.
17. Escalante, M.F., J. Vannier, and A. Arzande, *Flying capacitor multilevel inverters and DTC motor drive applications.* IEEE Transactions on Industrial Electronics, 2002. **49**(4): p. 809-815.
18. Koshti, A.K. and M.N. Rao. *A brief review on multilevel inverter topologies*. in *2017 International Conference on Data Management, Analytics and Innovation (ICDMAI)*. 2017.
19. Xiaoming, Y., H. Stemmler, and I. Barbi, *Self-balancing of the clamping-capacitor-voltages in the multilevel capacitor-clamping-inverter under sub-harmonic PWM modulation.* IEEE Transactions on Power Electronics, 2001. **16**(2): p. 256-263.
20. Manjrekar, M.D. and T.A. Lipo. *A hybrid multilevel inverter topology for drive applications*. in *APEC '98 Thirteenth Annual Applied Power Electronics Conference and Exposition*. 1998.

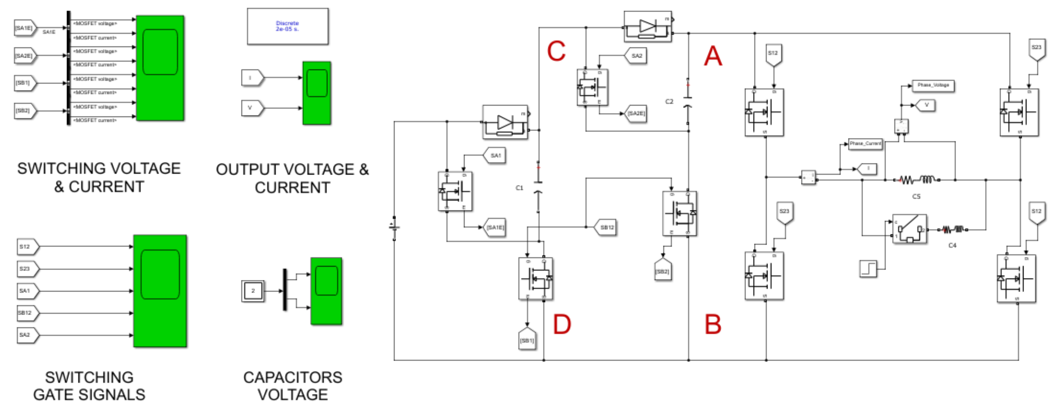
21. Taleb, R., et al. *A comparative analysis of multicarrier SPWM strategies for five-level flying capacitor inverter*. in *2016 8th International Conference on Modelling, Identification and Control (ICMIC)*. 2016.
22. Ranjan, A.K., D.V. Bhaskar, and N. Parida. *Analysis and simulation of cascaded H-bridge multi level inverter using level-shift PWM technique*. in *2015 International Conference on Circuits, Power and Computing Technologies [ICCPCT-2015]*. 2015.
23. Rashid, M.H., *Power electronics: circuits, devices and applications*.
24. Dixon, J., et al., *High-Power Machine Drive, Using Nonredundant 27-Level Inverters and Active Front End Rectifiers.* IEEE Transactions on Power Electronics, 2007. **22**(6): p. 2527-2533.
25. Liu, Y., et al., *Small-Signal Model-Based Control Strategy for Balancing Individual DC Capacitor Voltages in Cascade Multilevel Inverter-Based STATCOM.* IEEE Transactions on Industrial Electronics, 2009. **56**(6): p. 2259-2269.
26. Jain, K.K.G.a.S., *Topology for multilevel inverters to attain maximum number of levels from given DC sources.* IET Power Electron, 2012. **Vol. 5**(Iss.4): p. pp. 435– 446.
27. Glinka, M. *Prototype of multiphase modular-multilevel-converter with 2 MW power rating and 17-level-output-voltage*. in *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*. 2004.
28. Barrena, J.A., et al., *Individual Voltage Balancing Strategy for PWM Cascaded H-Bridge Converter-Based STATCOM.* IEEE Transactions on Industrial Electronics, 2008. **55**(1): p. 21-29.
29. Tsunoda, A., Y. Hinago, and H. Koizumi. *A grid connected inverter with switched capacitor inverter using series/parallel conversion*. in *2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC)*. 2012.
30. Hinago, Y. and H. Koizumi, *A Switched-Capacitor Inverter Using Series/Parallel Conversion With Inductive Load.* IEEE Transactions on Industrial Electronics, 2012. **59**(2): p. 878-887.
31. Kanimozhi, M. and P. Geetha. *A new boost switched capacitor multilevel inverter using different multi carrier PWM techniques*. in *2014 International*

Conference on Circuits, Power and Computing Technologies [ICCPCT-2014]. 2014.

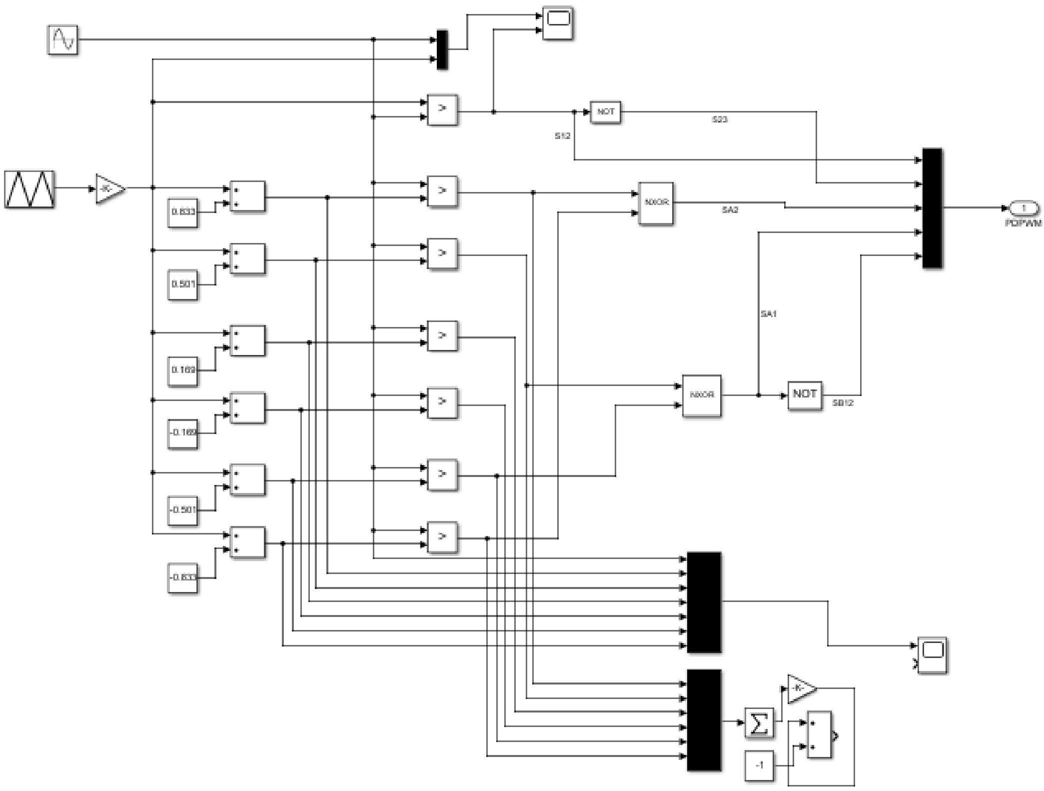
32. Raman, S.R., K.W.E. Cheng, and J. Hu. *A seven level switched capacitor multilevel inverter with asymmetric input sources for microgrids*. in *2017 20th International Conference on Electrical Machines and Systems (ICEMS)*. 2017.
33. Liu, J., K.W.E. Cheng, and Y. Ye, *A Cascaded Multilevel Inverter Based on Switched-Capacitor for High-Frequency AC Power Distribution System.* IEEE Transactions on Power Electronics, 2014. **29**(8): p. 4219-4230.
34. Raman, S.R., Y. Ye, and K.W.E. Cheng. *Switched-capacitor multilevel inverters for high frequency AC microgrids*. in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*. 2017.
35. Ye, Y., et al., *A Step-Up Switched-Capacitor Multilevel Inverter With Self-Voltage Balancing.* IEEE Transactions on Industrial Electronics, 2014. **61**(12): p. 6672-6680.
36. Jain, P., et al., *A Review of High-Frequency Power Distribution Systems: For Space, Telecommunication, and Computer Applications.* IEEE Transactions on Power Electronics, 2014. **29**(8): p. 3852-3863.
37. Kishore, P.M. and R. Bhimasingu. *A split source boost switched capacitor multilevel inverter for low power applications*. in *2017 National Power Electronics Conference (NPEC)*. 2017.
38. Mohan D., K.S.B., *A Comparative Analysis of Multi Carrier SPWM Control Strategies using Fifteen Level Cascaded H- Bridge Multilevel Inverter.* International Journal of Computer Applications (0975-8887), March 2012. **41,No.21.**
39. Bhagyalakshmi, P.S., B.M. Varghese, and B.M. Jos. *Switched capacitor multilevel inverter with different modulation techniques*. in *2017 International Conference on Innovations in Information, Embedded and Communication Systems (ICIIECS)*. 2017.

APPENDIX

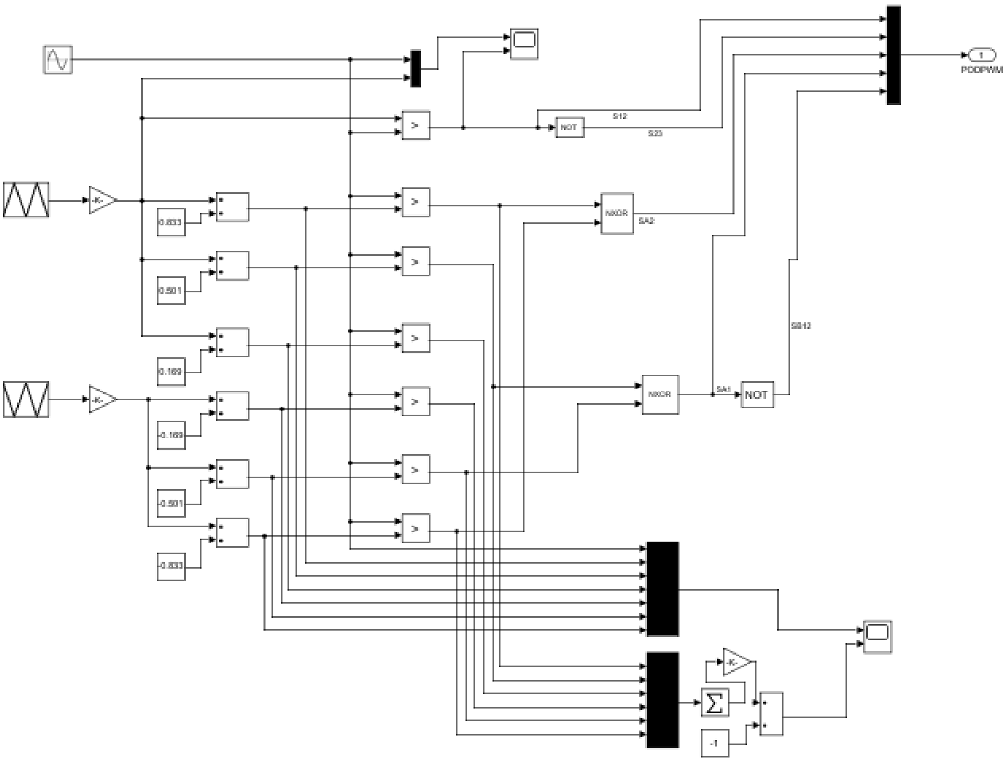
Modelled diagram of 7 level Switched Capacitor MLI MATLAB/SIMULINK



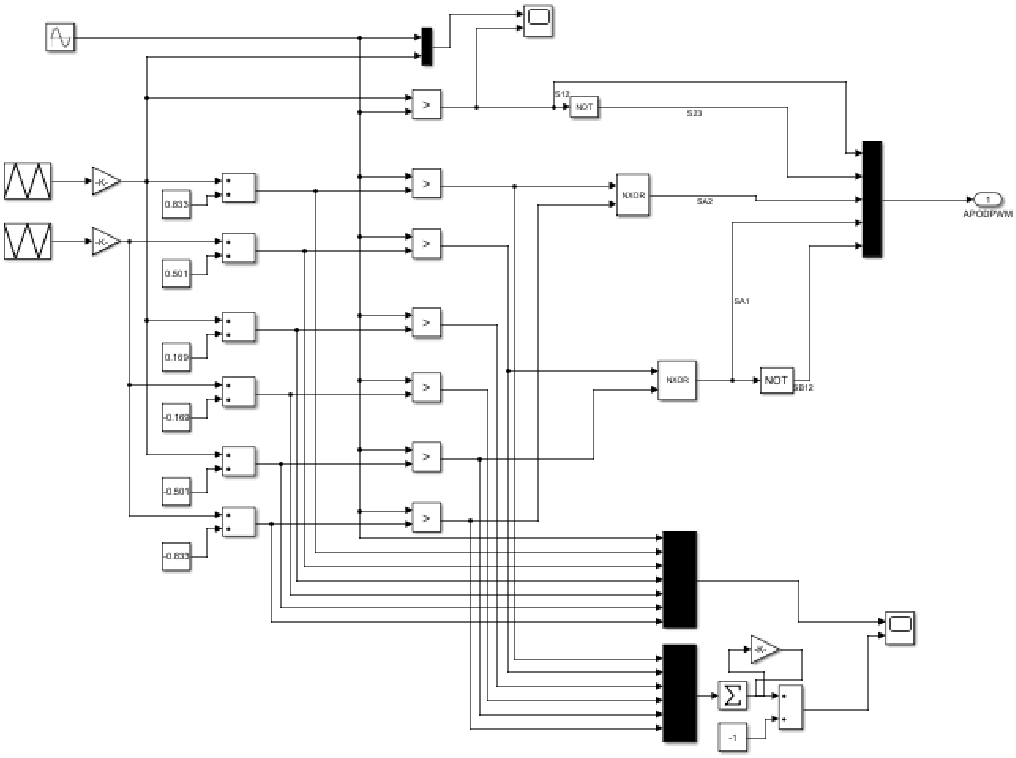
PD-SPWM model diagram MATLAB/SIMULINK

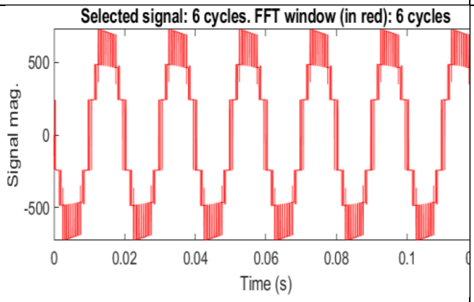
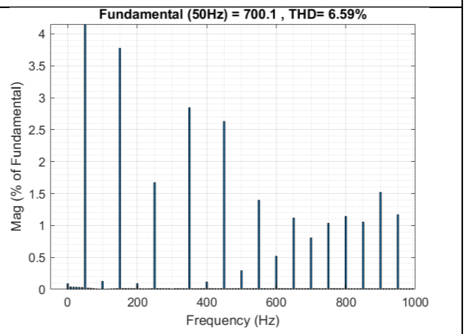
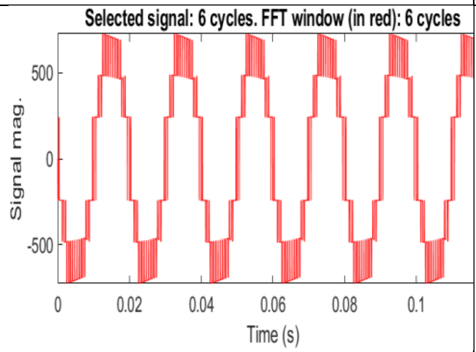
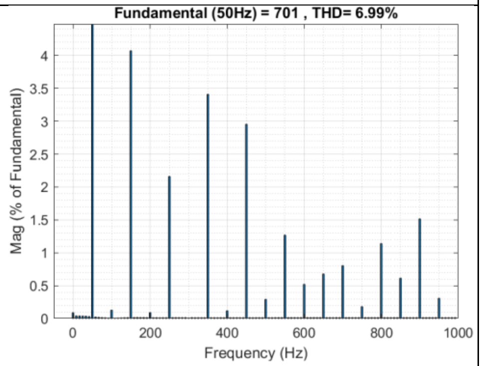
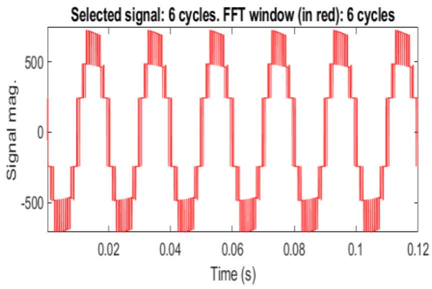
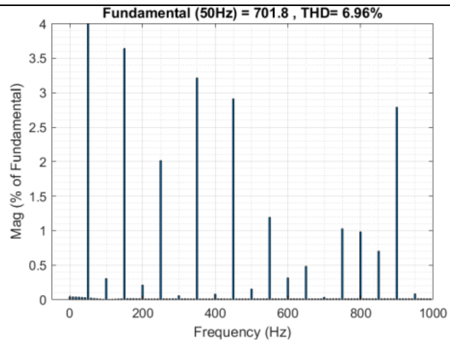
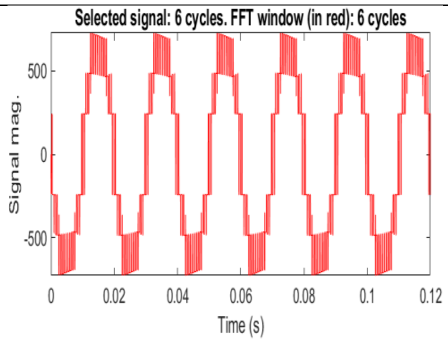
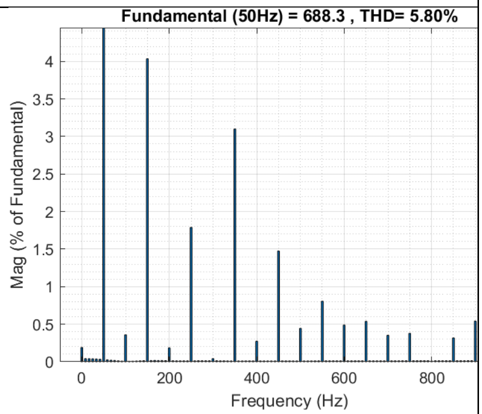


PD-SPWM model diagram MATLAB/SIMULINK

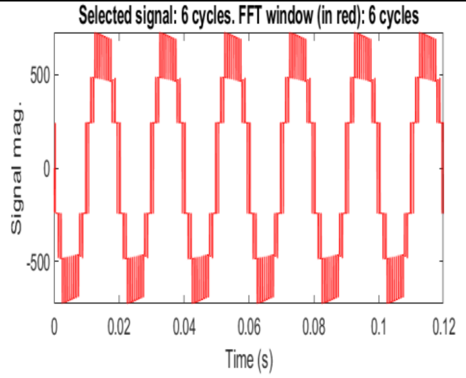


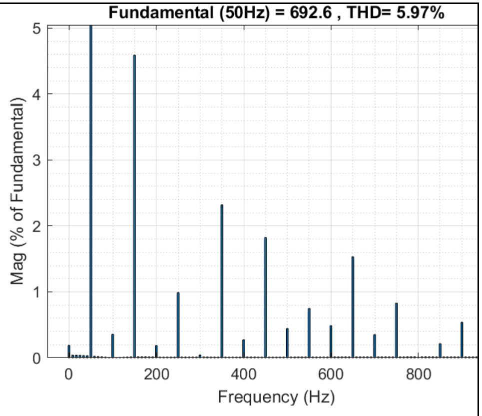
APOD-SPWM model diagram MATLAB/SIMULINK



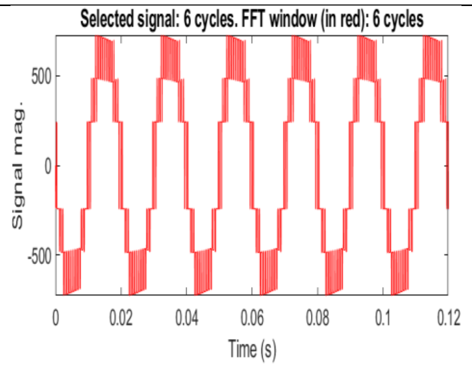
<table>
<tr><th>Mi</th><th>Output Voltage Wave form</th><th>THD% Spectrum</th></tr>
<tr><td>M = 0.8</td><td></td><td></td></tr>
<tr><td>PD</td><td>
</td><td>
</td></tr>
<tr><td>POD</td><td>
</td><td>
</td></tr>
<tr><td>APOD</td><td>
</td><td>
</td></tr>
<tr><td>M = 0.6</td><td></td><td></td></tr>
<tr><td>PD</td><td>
</td><td>
</td></tr>
</table>

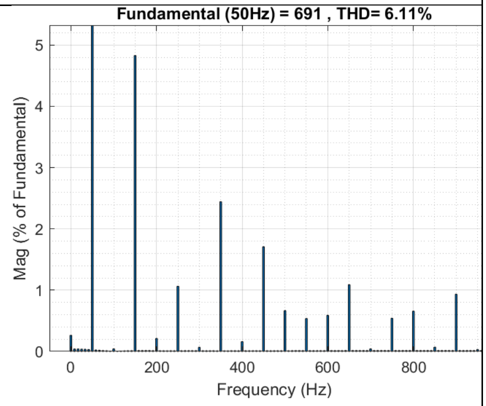
POD





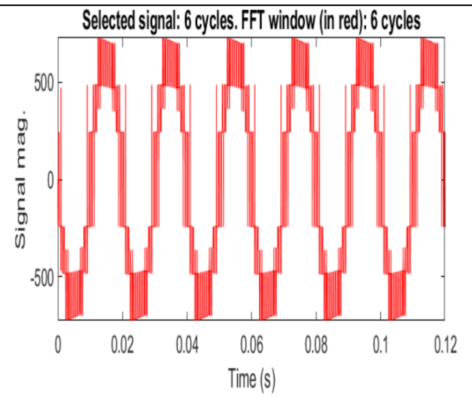
APOD

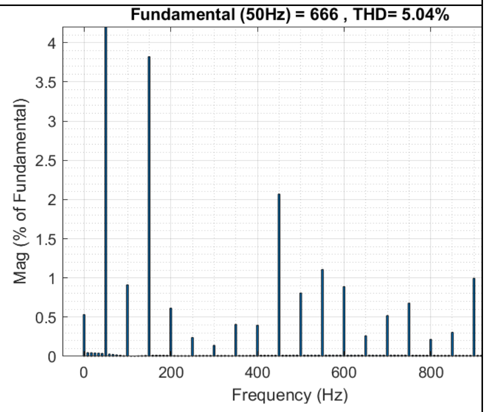




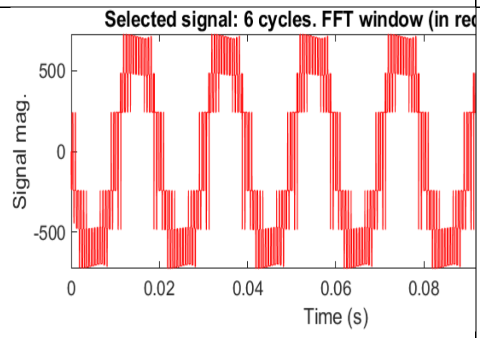
M = 0.4

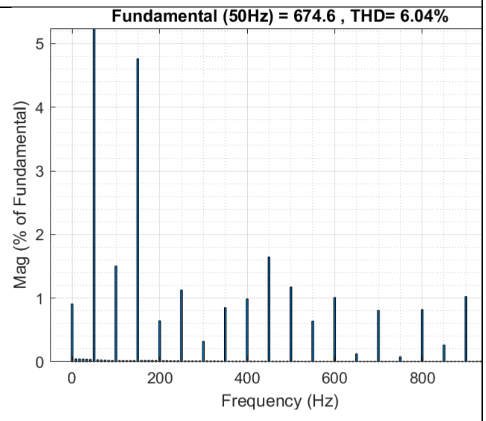
PD

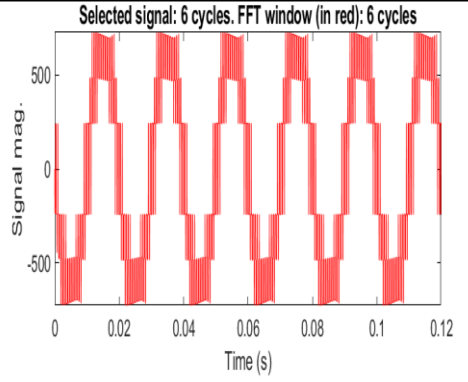
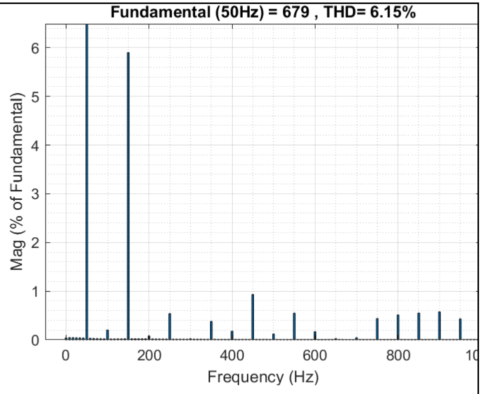
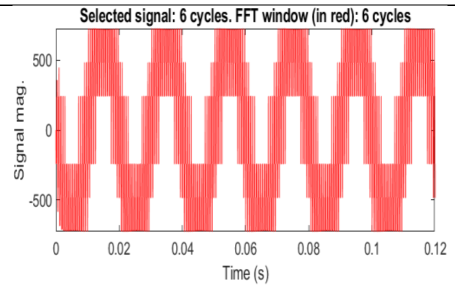
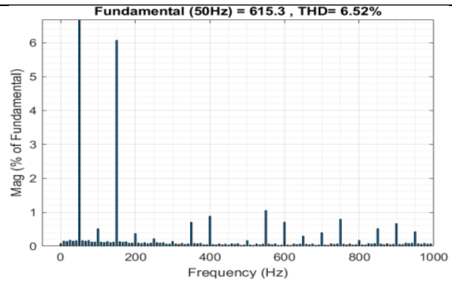
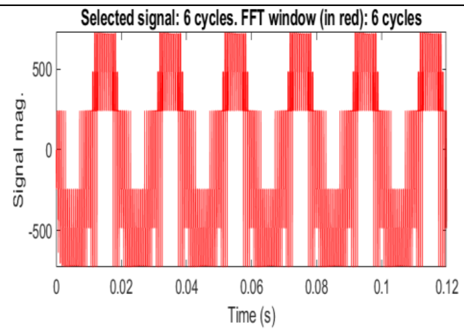
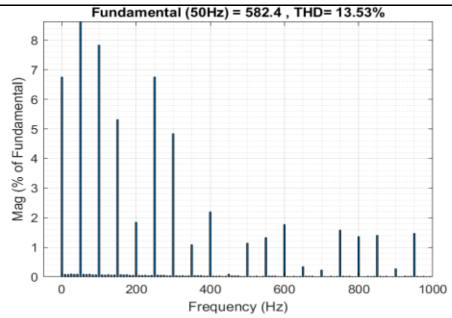
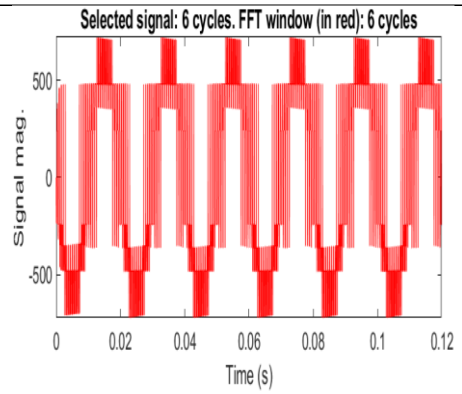
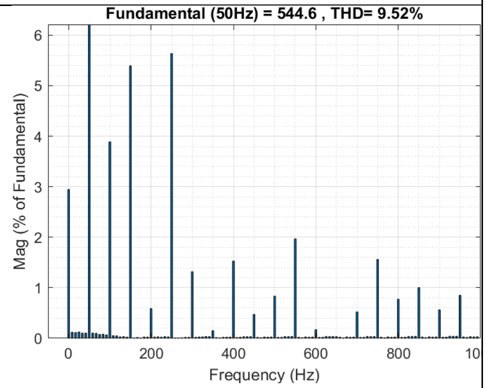




POD





<table>
<tr><td>APOD</td><td>
</td><td>
</td></tr>
<tr><td>M = 0.2</td><td></td><td></td></tr>
<tr><td>PD</td><td>
</td><td>
</td></tr>
<tr><td>POD</td><td>
</td><td>
</td></tr>
<tr><td>APOD</td><td>
</td><td>
</td></tr>
</table>