EVALUATION OF SNEAK PATH CURRENT IN SELF-RECTIFYING MEMRISTOR CROSSBAR

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DEDICATION

This project is dedicated to my father, who has always been the pillar of strength of my family. His determination positively influenced me and inspired me for never give up easily. This work is also dedicated to my mother, who is always by my side through all the ups and downs. She always showered me with endless care and encouragement.

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ABSTRACT

Memristor is a non-volatile memory nanodevice which requires lower energy to operate. Besides, memristor is fast yet stable, thus making it attractive in the computing field and competitive as alternative candidate for the integration of high-density memory. While acting as a memory cell in a crossbar array circuit, there is limitation related to undesired sneak path current. Utilizing a self-rectifying memristor is reported to minimize the effect of the sneak path issue. Since there is lack of resources on research of implementing self-rectifying memristor in crossbar array structure, it is the focus of this project. The objective of this project is to model and simulate self-rectifying memristor with different rectification ratio and non-linearity. Their effect on the performance of memristor in crossbar array structure is then analyzed. Several types of self-rectifying memristor are reviewed and their compact SPICE models are generated. The memristor SPICE model is used to build a crossbar array circuit and run simulation through LTSPICE software. Moreover, comparison between Knowm memristor and self-rectifying memristor is done by observing their current-voltage relationship. The reduction of sneak path current by using different value of saturation current in self-rectifying memristor is evaluated and the effect of rectification ratio and non-linearity is being studied. Based on the simulation result, low saturation current helps to ensure large rectification ratio and non-linearity to lower sneak path current in the circuit. In short, self-rectifying memristor is able to effectively suppress sneak path current in crossbar array.

ABSTRAK

Memristor ialah peranti nano memori bukan meruap yang beroperasi dengan penggunaan tenaga yang rendah. Selain itu, memristor adalah pantas lagi stabil, oleh itu memristor semakin menjadi tarikan dalam bidang pengkomputeran dan berkeupayaan menjadi calon alternatif bagi penyepaduan memori yang berketumpatan tinggi. Di samping digunakan sebagai sel memori dalam litar tatasusunan bar bersilang, batasan litar tersebut ialah laluan susup yang tidak diingini. Penggunaan memristor pengayaan diri dikatakan dapat meminimumkan kesan yang disebabkan oleh laluan susup. Oleh sebab kekurangan sumber penyelidikan yang berkaitan dengan memristor pengayaan diri dalam struktur tatasusunan bar bersilang, ia dijadikan sebagai tumpuan projek ini. Objektif projek ini adalah untuk mengilustrasikan dan mensimulasikan memristor pengayaan diri dengan nisbah rektifikasi dan nilai bukan linear yang berlainan. Kesan-kesan terhadap prestasi memristor dalam struktur tatasusunan palang kemudian dianalisis. Beberapa jenis memristor pengayaan diri telah dikaji dan model SPICE turut dihasilkan. Model SPICE memristor digunakan untuk membina litar tatasusunan bar bersilang jenis dan menjalankan simulasi dengan perisian LTSPICE. Tambahan pula, perbandingan antara memristor Knowm dan memristor pengayaan diri dijalankan dengan meneliti hubungan arus dengan voltan. Pengurangan arus laluan susup bagi memristor pengayaan diri yang berlainan arus teru juga dinilai di samping kesan nisbah rektifikasi dan nilai bukan linear turut diteliti. Berdasarkan keputusuan simulasi, arus teru yang rendah dapat memastikan nisbah rektifikasi dan nilai bukan linear yang tinggi serta mengurangkan laluan susup dalam litar. Pendek kata, memristor pengayaan diri dapat menyelesaikan masalah laluan susup dalam litar tatasusunan bar bersilang secara efektif.

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LIST OF ABBREVIATIONS

NVM	-	Non-volatile Memory
ROM	-	Read-only Memory
EPROM	-	Erasable programmable ROM
EEPROM	-	Electrically erasable programmable ROM
LRS	-	Low Resistance State
HRS	-	High Resistance State
1D1M	-	One-Diode-One Memristor
1T1M	-	One-Transistor-One Memristor
1S1M	-	One-Selector-One Memristor
SRM		Self-Rectifying Memristor
VMM	-	Vector Matrix Multiplication
FAST	-	Field Assisted Superlinear Threshold
OTS	-	Ovonic Threshold Switching
VBS	-	Varistor-type Bidirectional Switch
MIIM	-	Metal-Insulator-Insulator-Metal
MIM	-	Metal-Insulator-Metal

CHAPTER 1

INTRODUCTION

1.1 Background Study

In 1965, Gordon Moore came out with a prediction where the number of transistors on integrated circuit chip would double up every two years, which is known as Moore's law [1]. This trend is realized by focusing in three aspect which is 20% of chip area increment per year, 10% feature size decrement per year, device and circuit design enhancement [2]. However, the community believed that Moore's law would not last forever as there is limitation in device scaling and it has always been the main concern. Aside of the dimension of the device, the semiconductor industry needs to balance in between the device reliability and manufacturing cost in order to fulfil the market needs while making sure they are sustainable. Rapid growth in computing field increases the demand of fast and promising alternative memory device to take over current solid state storage technologies.

Solid state storage or non-volatile memory (NVM) is memory that is capable for information storing without power supply for long term storage purpose which includes Read-only Memory (ROM) for example EPROM and EEPROM, flash memory and magnetic computer storage device. Figure 1.1 shows the device structure of NVM where floating gate is the polysilicon layer for data storage. Data is able to retain during power off because the bilayer structure is consisted of conductive metal oxide and insulating oxide where the tunnel oxide acts as an insulator that prevents the leakage of negative charge [3]. NVM is widely used in multiple applications including cell phones, tablets and laptops where these electronic appliances are part of our daily essential items in this era. As we are approaching the limitation in device capacity, a substitution device is desired.

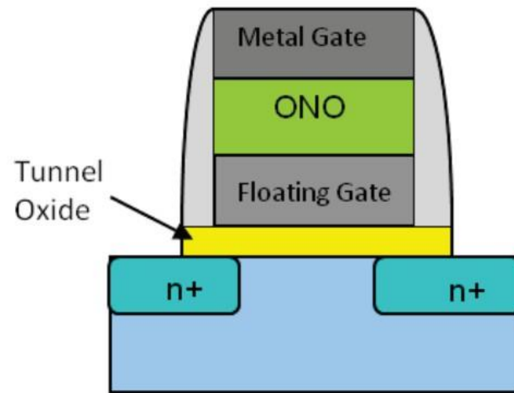

Figure 1.1 Cross section of NVM device [3]

1.1.1 Memristor

Memristor which is also known as memory resistor was first discovered by Leon Chua in 1971 as the fourth basic two-terminal circuit element, other than resistor, capacitor and inductor [4]. This device works on memristor technology that links up magnetic flux and movement of charge while their relationship in between is named as memristance, which is the resistance that varies according to flux and current with unit Ohm (Ω). Figure 1.2 represents the structure of a memristor device where resistive element such as titanium oxide is sandwiched in between two metal electrodes. This layer in between is split into two regions: TiOx is high conductive doped region with length of W while TiO is high resistive undoped region [5]. The overall length of the device is represented by parameter D. The dual layer structure of the device possesses benefit in current control.

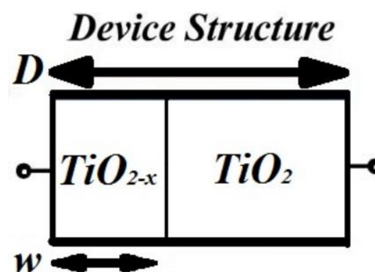

Figure 1.2 Memristor device structure [5]

For the ease of understanding, memristor is always described as a water pipe that changes its diameter according to the direction of water flow. Water represents the electric charge where when it flows in a single direction, the memristor is less resistive while if the charge flows in an opposite direction, the device becomes more resistive [6]. When we apply voltage across the device, an electric field is formed and subsequently causes the vacant positive charged oxygen ion in the doped region to repel towards the undoped region [7]. This act turns the device to be more conductive. On the other hand, when a negative voltage is applied, the positive charged ions are attracted away of TiO_2. Thus, the device turns out more resistive. Figure 1.3 shows the distribution of positive ions during different conditions of voltage supply.

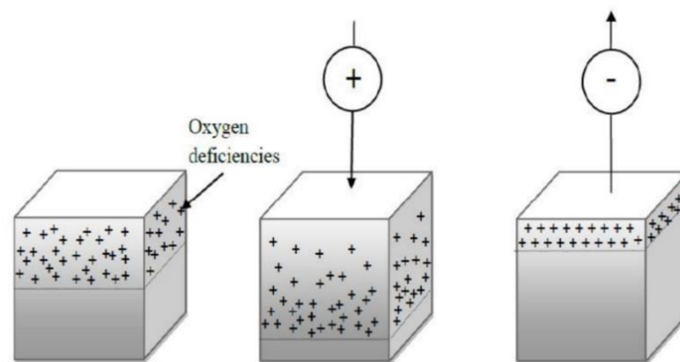

Figure 1.3 Memristor behaviour during each operation: (from left) no voltage supply, positive voltage and negative voltage [8]

In short, the voltage supplied varies the length of the doped region and changes the total resistivity of the device. The dynamic resistance value represents different memory states where low resistance state (LRS) is logical 1 while high resistance state (HRS) is logical 0. Memristor exhibits the characteristic of 'pinched hysteresis loop' which each current value corresponds to two voltage value as shown in Figure 1.4 [6]. This loop perfectly explains what Leon Chua said, "If it's pinched it's a memristor" and the pinched point is the only current value that does not correspond to two voltages. Other than that, memristor has the ability to retain information even when the power is off because oxygen ions are able to stay at the same location and being freeze in the boundary between the layers no matter the polarity of voltage being switched is positive or negative [6].

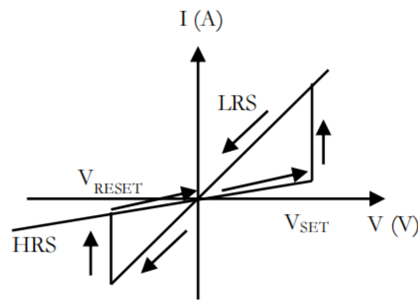

Figure 1.4 IV characteristic of memristor [9]

Memristor caught the community's attention as an alternative candidate for non-volatile memory nanodevice due to its unique characteristics. The physical structure of memristor is simple yet high density. According to [10], memristor is able to achieve read latencies of as low as 7.2ns. Moreover, memristor is not only fast and stable but also offers a better on/off resistance ratio than STT-RAM with lower power consumption [11]. The non-volatility of memristor makes it attractive to be applied in memory and logic deigns. Besides, memristor behaves like synapse to be utilized in neuromorphic systems due to its flexibility and controllable flux.

1.1.2 Crossbar Array

Crossbar array structure is a two dimensional grid which consists of two different conductive lines, namely word line that indicates the input and bit line that represents the output. By referring to Figure 1.5, the devices are located at each intersection point of the top electrodes and bottom electrodes [12]. Figure 1.6 shows the equivalent circuit as Figure 1.5 and gives a better view in connection where the word lines are in pink, bit lines are in blue while the devices are in green. At each time, only one cell is allowed to be targeted to perform either read or write operation. During the write operation, word line is connected to the voltage supply while bit line is grounded. In order to perform read operation, word line is grounded while bit line is connected to the voltage supply. The device would only turns conducting when the voltage applied exceeds the threshold voltage which is the minimum voltage that allows the current to flow from top electrode to bottom electrode.

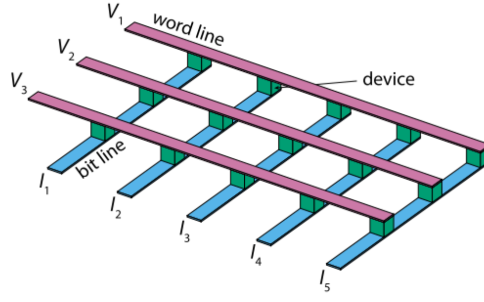

Figure 1.5 Structural diagram of crossbar array [12]

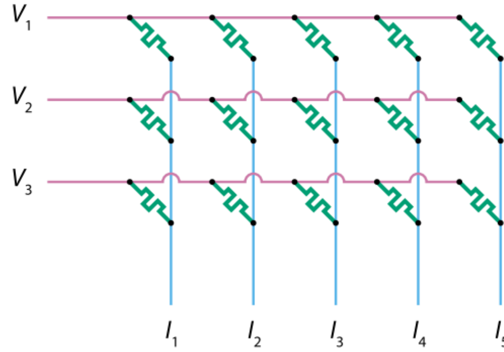

Figure 1.6 Circuit diagram of crossbar array [12]

The device in the crossbar array works based on two laws. The first law that being applied is Kirchhoff's current law where the total current entering the device in each column is equal to the total current leaving the particular column [13]. Secondly, the crossbar array is related to Ohm's law where the current passed through the selected device at (i, j) is represented by equation (1.1) while conductance, G is the inverse of resistance, i represents row in the array and j is column in the array [13]. This equation can also be written in form of charge as equation (1.2) by substituting total charge as it equals to the multiplication of current and its corresponding time.

$$I_j = \sum_i V_i G_{ij} \tag{1.1}$$

$$Q_j = \sum_i V t_i G_{ij} \tag{1.2}$$

Crossbar array structure is desired as it benefits from various perspectives. In terms of scalability, the dimension of wire is able to be scaled down to molecular size

while the number of wires can be casually increased to achieve a large size of circuit for either memory or logic application [14]. Crossbar architecture also offers the ability of stacking so by having layers of cell being vertically stacked together, the cell area can be kept small [15]. It can be described as a multistorey carpark that is being compared between single storey as this structure has a greater capacity. Furthermore, since crossbar array structure is simple, the manufacturing cost is lower while at the same time having nanoscale fabrication achievable. This architecture is rebuildable if any defective elements are found [16].

1.2 Problem Statement

The problem statements of this research are as listed below:

1. Most of the developed SPICE model does not consider non-linear characteristic in self-rectifying memristor as compared to linear behaviour.
2. Most of the research focus on reduction in sneak path current instead of the effect of rectification ratio and non-linearity towards the performance of self-rectifying memristor in crossbar array.

1.3 Research Objective

The principal aim of this research is to figure out in-memory logic circuit that can be implemented in crossbar array while getting the sneak path current issue solved. Thus, the objectives of the research are set to be aligned with the stated problem statements which include:

1. To model and simulate self-rectifying memristor with different rectification ratio and non-linearity.

2. To analyze the effect of different rectification ratio and non-linearity on the performance of self-rectifying memristor in crossbar array structure.

1.4 Research Scope

Scopes that are being covered in this research are as following:

(a) This research models non-linear self-rectifying memristor.

(b) Rectification ratio and non-linearity of memristor is the focused variable.

(c) Self-rectifying memristor with various saturation current are implemented in crossbar array circuit.

(d) LTspice is an open-source tool that is used as simulation tool in this research while MATLAB is tool used for graph replotting.

1.5 Chapter Summary

Chapter 1 presents a general overview on the current memory technology and includes a brief introduction of memristor and crossbar array. Then, the problem statements are listed according to the research gap, followed by research objectives and research scope that aims to get the stated issues resolved.

In Chapter 2, sneak path current along with its impact that occurs in the crossbar array are being investigated. Furthermore, the characteristics and features of various types of memory cell in crossbar array such as 1D1M, 1T1M, 1S1M and self-

rectifying memristor are discussed as they are potential solutions for sneak path current. Some recent works on self-rectifying memristors with different structures and parameters are being tabulated and compared between their performance.

Chapter 3 introduces the methodology that is planned to carry out this project. The main focus of the project is self-rectifying memristor where the device modelling is first done, followed by I-V simulation by using SPICE model. The memristor is later implemented in a crossbar array circuit. The functionality and the performance of the model is being tested and analyzed. This chapter also includes the research timeline throughout two semesters.

Chapter 4 covers the simulated result of different memristors such as their I-V characteristic or crossbar array circuit building by using LTspice. Comments are given based on the outcome analysis. The performance of Knowm memristor and self-rectifying memristor are being compared while the effect of rectification ratio and non-linearity towards the behaviour of memristor is being figured out.

Lastly, Chapter 5 summarize the entire project and came out with conclusion from the research contributions. A few suggestions have been proposed based on the current work and field that yet to be discovered in future work are stated.

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