A 16×2 GEIGER MODE PHOTON COUNTER ARRAY AUTOMATED DATA ACQUISITION SYSTEMS IN 0.18 μm CMOS PROCESS

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DEDICATION

This project report is dedicated to my father, who taught me that the best kind of knowledge to have is that which is learned for its own sake. It is also dedicated to my mother, who taught me that even the largest task can be accomplished if it is done one step at a time.

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ABSTRACT

Photon detection technology involving single photon detection and counting is vital for areas such as biomedical, agriculture, two-dimensional imaging, three-dimensional ranging and fluorescence correlation spectroscopy. These applications require a photon detection system with fast response time and high sensitivity and Single Photon Avalanche Diode (SPAD) is identified to be a suitable candidate as a photon detector. SPAD provides fast photon counting, low biasing voltage, small in size and ability to integrate with Complementary Metal-Oxide Semiconductors (CMOS) compared with other photon detection methods. The motivation of this project is to achieve physical implementation of 2-Dimensional Array of SPAD with intention of improving sensitivity. Previous studies show limitations of SPAD application to detect very low intensity photon signals due to insufficient sensitivity. This project suggests a robust data acquisition system to work with 16 x 2 photon counting array of SPAD detector and its readout controller module. The integrated circuit will be implemented in Verilog Hardware Descriptive Language (HDL), simulated, synthesized, and tested for Application Specific Integrated Circuit (ASIC) implementation using Synopsys Electronic Design Automation (EDA) tool. Besides that, an additional task is in place to realize fabrication ready physical implementation of the proposed integrated circuit using 0.18 µm CMOS technology. The full design consists of 16 x 2 SPAD model, 16 bits 2 to 1 multiplexer, Brent-Kung Adder (BKA) as data acquisition system and a Parallel In Parallel Out (PIPO) shift register. Verifications are done to each element individually and to whole system to ensure functionality correctness. Physical implementation of the whole system is carried out to study area and power performance of the post-layout design. The 16 x 2 BKA system is able to achieve an area reduction of 20.93 % when taking the 16 x 2 KSA system as reference. The maximum main clock frequency and area consumption achieved by the 16 x 2 BKA system are 680.3 MHz and 11688.97 μm^2 respectively.

ABSTRAK

Teknologi pengesanan foton melibatkan pengesanan dan pengiraan foton tunggal mempunyai kepentingan dalam sektor sepert bioperubatan, pertanian, pengimejan dua dimensi, pengukuran kejauhan tiga dimensi dan spektroskopi korelasi pendarfluor. Aplikasi-aplikasi ini memerlukan sistem pengesanan foton dengan masa tindak balas yang cepat dan sensitiviti yang tinggi serta Diod Avalanche Foton Tunggal dikenal pasti sebagai pengesan foton yang sesuai. Diod Avalanche Foton Tunggal mempunyai ciri-ciri seperti pengiraan foton pantas, voltan pincang yang rendah, bersaiz kecil dan keupayaan untuk berintegrasi dengan semikonduktor-oksida logam pelengkap berbanding kaedah pengesanan foton lain. Motivasi projek ini adalah untuk mencapai pelaksanaan fizikal tatasusunan 2 Dimensi Diod Avalanche Foton Tunggal dengan hasrat untuk meningkatkan sensitiviti. Kajian terdahulu menunjukkan had aplikasi Diod Avalanche Foton Tunggal untuk mengesan isyarat foton intensiti sangat rendah kerana kepekaan yang tidak mencukupi. Projek ini mencadangkan sistem pemerolehan data yang teguh untuk berfungsi dengan 16 x 2 foton tatasusunan mengira untuk pengesan SPAD dan modul pengawal bacaannya. Litar bersepadu akan dilaksanakan dalam Verilog HDL, disimulasikan, disintesis dan diuji untuk pelaksanaan ASIC menggunakan alat Automasi Reka Bentuk Elektronik Synopsys. Di samping itu, tugas tambahan dilakukan untuk merealisasikan fabrikasi siap pelaksanaan fizikal litar bersepadu yang dicadangkan menggunakan teknologi CMOS 0.18 µm. Reka bentuk penuh terdiri daripada model 16 x 2 Diod Avalanche Foton Tunggal, 16 bit 2 hingga 1 pemultipleks, Penambah Brent-Kung sebagai sistem pemerolehan data dan daftar anjakan selari keluar. Pengesahan dilakukan kepada setiap elemen secara individu dan keseluruhan sistem untuk memastikan ketepatan fungsi. Pelaksanaan fizikal keseluruhan sistem telah dijalankan untuk mengkaji kawasan dan prestasi kuasa reka bentuk pasca susun atur. Sistem 16 x 2 BKA mampu mencapai pengurangan kawasan sebanyak 20.93 % apabila mengambil sistem 16 x 2 KSA sebagai rujukan. Frekuensi operasi maksimum dan penggunaan kawasan yang dicapai oleh sistem 16 x 2 BKA ialah 680.3 MHz dan 11688.97 μm^2.

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LIST OF ABBREVIATIONS

SNSPD	-	Superconducting Nanowire Single Photon Detector
TES	-	Transition Edge Sensor
SPAD	-	Single Photon Avalanche Diode
ASIC	-	Application Specific Integrated Circuit
PISO	-	Parallel In Serial Out
KSA	-	Kogge Stone Adder
PPA	-	Parallel Prefix Adder
RCA	-	Ripple Carry Adder
CSA	-	Carry Save Adder
BKA	-	Brent-Kung Adder
FPGA	-	Field Programmable Gate Arrays
DRC	-	Design Rule Check
CMOS	-	Complementary Metal-Oxide Semiconductor
RTL	-	Register Transfer Level
DC	-	Design Compiler
ICC	-	IC Compiler
BIST	-	Build-In-Self-Test
STA	-	Static Timing Analysis
EDA	-	Electronic Design Automation
LVS	-	Layout Versus Schematic
HDL	-	Hardware Descriptive Language
CTS	-	Clock Tree Synthesis
MCMM	-	Multi Corner Multi Mode

LIST OF SYMBOLS

K	-	Kelvin
ns	-	Nano Second
%	-	Percent
Hz	-	Hertz
W	-	Watt
k	-	Kilo
G	-	Giga
μm^2	-	Micro Metre Square

CHAPTER 1

INTRODUCTION

1.1 Introduction

The background of the project, problem statement, objectives, scopes of project and significance of the project will be presented and discussed in this chapter.

1.2 Problem Background

Quantum photonic is one of the focused research as this field of study is beneficial to multiple domains such as biomedical, agriculture, 2D imaging, 3D ranging and fluorescence correlation spectroscopy. Generation, manipulation and detection of the photon quantum states are generic stages of process for a typical quantum photonic system [1]. There are types of single photon detectors such as Superconducting Nanowire Single Photon Detector (SNSPD) [2], Transition Edge Sensor (TES) [3] and Single Photon Avalanche Diode (SPAD) [4]. SPAD is the most suitable photon detection methodology for either experimental setup or portable solution due to its' ability to operate under room temperature condition while the other two methods will require extremely low working temperature from 1 K to 4 K [2,3]. SPAD also possesses benefits such as efficient photon detection, low operating voltage and ability to be implemented into array form [5]. For the observability of the photons detected by a SPAD array, a data acquisition system is required.

SPAD is one of the photon detection methodologies in quantum photonic with advantages such as integrability into Application Specific Integrated Circuit (ASIC), small size, low power consumption due to lower operating voltage and ability in detecting low intensity photons [6]. SPAD, also known as Geiger mode avalanche photodiode, is built from a PN junction structure which operates under reverse biased

voltage that exceeds breakdown voltage [7]. When SPAD is operating in reverse voltage higher than breakdown voltage, there is no current flow due to the depletion region missing free carriers. Any photon absorbed in this moment will result in avalanche current from ionisation which indicates the photon is detected and a quenching circuit will reset the avalanche current by lowering the reverse voltage.

The implication of SPAD into a 16x1 array is presented by Suhaila et al in enabling the possibility for imaging purpose [8]. A data acquisition system will be required to make the photons detected by SPAD array countable and observable. A complete parallel photon counting circuit will consist of two main portions which are the front end part, SPAD array that detects asynchronous photon signals and the backend part, a synchronous data acquisition system [9] [10]. A backend data acquisition system with 4 main blocks which are pulse discriminator, clock divider, Parallel In Serial Out (PISO) register and Kogge Stone Adder (KSA) is proposed by Kumar [11].

The adder portion which carries out photon counting operations is the bottleneck of the data acquisition system which determines the operating frequency [12]. KSA which is a kind of Parallel Prefix Adder (PPA) was used as counting element in previous implementation due to PPA is having lowest latency compared with other adder topologies such as Ripple Carry Adder (RCA), Carry Save Adder (CSA) and Carry Select Adder [13]. The drawback of KSA will be contribution to large cell area consumption and Brent-Kung Adder (BKA) is showing possibility to replace KSA with the advantage of simplifying complexity of the circuit and leads to area reduction in post physical implementation layout as it is showing saving of 41 % area saving with 22.26 % longer latency [14]. With the latency of 0.7 ns achieved by KSA data acquisition system [15], the degradation in delay of the counter portion is estimated to be able to achieve the requirement of the SPAD array used which is 200 MHz.

ASIC are integrated circuits designed for a specific purpose or function [16]. By implementing the data acquisition system with ASIC, the design can benefit from power consumption and delay performance compared with Field Programmable Gate

Arrays (FPGA). Implementation with standard cell methodology of ASIC will speed up the design process due to easier convergence of the design's timing and Design Rule Check (DRC) of the technology process used.

1.3 Problem Statement

Large area consumption of data acquisition systems with usage of KSA as a photon counting element is being reported by previous research [17] which requires improvement. Area overhead is an important design constraint which determines the design's cost and functionality that is allowed to be implemented within the design. This project will look for a type of adder that possesses lower area overhead and comparable delay to substitute KSA as a counting element.

The finding from previous research by J.W Tai [18] is showing that the 16 x 1 SPAD array is having limitations in sensitivity for photon counting where 16 x 2 SPAD is proposed to improve the sensitivity but there is an existing flaw in the proposed solution where the sensitivity is not improved successfully. Optimization will be done by this project to complete the solution proposed by the previous project and achieve the target of improving sensitivity.

Besides that, physical implementation of the data acquisition system for the SPAD module is needed due to low implementation cost and low power consumption. ASIC is more cost efficient in large scale fabrication and the power consumption of ASIC can be well optimised and controlled more precisely. Lower power consumption will be translated into longer battery life for portable solutions.

1.4 Objectives

The main purpose of this project is to carry out physical implementation of a data acquisition system with BKA for a 16 x 2 SPAD photon counting array with technology process of 0.18 µm Complementary Metal-Oxide Semiconductor (CMOS).

The applicable performance metrics such as timing convergence, area consumption and power consumption of pre and post layout design will be extracted and evaluated.

Here are the objectives of this project:

- To design 16 x 2 photon counting array front-end circuit with data acquisition system on-chip.
- To integrate the proposed 16 × 2 photon counting array for fabrication ready physical implementation using 0.18 µm CMOS technology.
- To reduce area consumption by using 16-bits BKA.
- To characterise the proposed circuit for timing, power and area performances.

1.5 Scopes of Project

The scopes of the project are:

- Specification of APD in [9] have been used.
- Register Transfer Level (RTL) is designed in Verilog Hardware Descriptive Language (HDL) form.
- Optimization is done on the acquisition system adder portion proposed by J.W Tai.
- Random signal generation module is included to simulate photon signal captured by SPAD module.
- Quartus is used to verify the functionality of the blocks in the data acquisition circuit with Verilog HDL form with testbench.
- Design Compiler (DC) is used to translate Verilog HDL into gate-level netlist.

- IC Compiler (ICC) is used to carry out physical implementation.
- Analyse the floorplan size, timing and power consumption of the ASIC design.
- The physical implementation and performance metrics analysis are implemented on 16 x 1 KSA, 16 x 2 KSA and 16 x 2 BKA based systems.

1.6 Significance of Project

This project is going to contribute to photon detection of the quantum photonic field. Improvement in sensitivity of the SPAD application translates into more photon counts per second and more precise results from photon counting are expected to be contributed by this project. Besides that, the effort of this project in reducing the area consumption for the data acquisition system of the SPAD module will contribute to the possibility of incorporating more features for the system and suitable for portable solutions in applications such as agriculture and biomedical field. Reduction of the area consumption with usage of BKA also gives more area of utilisation for further development such as introducing Build-In-Self-Test (BIST).

1.7 Report Organisation

This project proposal is made up from five chapters. This chapter provides an introduction on the research topic of this project, explanation of the problem background which motivates this research, problem statement, objectives of the research, project scope and the overall organisation of this report. Chapter two elaborates the literature review done on the data acquisition system and the adder comparison in identifying the problem statement. Chapter three displays the methodology of implementing the 16 x 2 data acquisition system with BKA from RTL to physical layout. Chapter four will present the experimental data and discussion on the findings of the 16 x 1 KSA, 16 x 2 KSA and 16 x 2 BKA systems in various performance metrics during synthesis, place and route and Static Timing Analysis

(STA). The project management plan will be explained in this chapter as well. Chapter five will summarise the findings obtained from the project outcome and then explain the limitation and future improvement for this project.

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