STUDY OF TIME-DEPENDENT DIELECTRIC BREAKDOWN (TDDB) IN 15MM JUNCTIONLESS FINFET

CHNG SZE LYN

UNIVERSITI TEKNOLOGI MALAYSIA

DEDICATION

This project report is dedicated to my father, who taught me that the best kind of knowledge to have is that which is learned for its own sake. It is also dedicated to my mother, who taught me that even the largest task can be accomplished if it is done one step at a time.

ACKNOWLEDGEMENT

In preparing this report, I had to take the help and guideline of some respected persons, who deserve our greatest gratitude. The completion of this report gives me much pleasure, and I would like to show my gratitude to Ts. Dr. Nurul Ezaila Binti Alias, my supervisor, Senior Lecturer, School of Electrical Engineering, Faculty of Engineering, Universiti Teknologi Malaysia for giving me a good guideline for this report throughout numerous consultations. I would also like to expand our deepest gratitude to all those who have directly and indirectly guided us in preparing this project report.

Many people, especially our classmates, have made valuable comment suggestion on this project which gave us an inspiration to improve the project. I would like to thank all the people for their help directly and indirectly to complete this report.

ABSTRACT

As MOSFETs already reached the limitation in terms of physical and electrical characteristic which is difficult to continue producing with MOSFET due to the level of difficulty and complexity. Although, FinFETs provide several advantages but there are some drawbacks of FinFETs such as higher fabrication cost, difficult to control dynamic threshold voltage etc. Therefore, JL FinFETs has been proposed to overcome the shortcoming. The main difference of FinFETs and JL FinFETs is the presence of junctions and gradient of doping concentration between source and drain. Therefore, JL FinFETs offers higher scalability with lower cost, higher compatibility and additional design parameters like substrate doping concentration. In recent, reliability of device has become one of the major concerns when scaling to nano regime. There are many works on reliability studies have been done includes Negative Bias Temperature Instability (NBTI), Hot Carrier Injection (HCI), Time Dependent Dielectric Breakdown (TDDB) that occurs in MOSFETs. However, the information regarding reliability issue for JL FinFETs is very limited. Therefore, the reliability issue of JL FinFETs become a primary concern and should be investigated. This project mainly discussed about TDDB including type of physical model, typical behavior, constant stress test. The aims of project are to design and simulate the 15nm JL FinFETs device structure and TDDB test applications. Synopsys Sentaurus TCAD will be used for the simulation purpose. The design parameter for n-channel JL FinFETs using 15nm as the gate length, and 10nm for width and height of the fin. Then, TDDB test with Constant Voltage Stress (CVS) method will be carried out by for approx. 10 years with 3 different stresses applied to analyze the threshold voltage shift of 15nm JL FinFETs before and after the stress applications for long-term reliability of the oxide. The stress voltage was determined as 0.9V, 1.35V and 1.8V. Besides, the test will be carried out with several oxide thickness such as 1nm, 2.5nm, 4nm, 6nm and 10nm with numerous types of oxide material like SiO_2, HfO_2 and Si_3N_4. According to the experimental result, JL FinFETs with the combination of Si_3N_4 provide the greatest time to failure compared to SiO_2 and HfO_2 with the highest range in threshold voltage shift which is 2.17% - 8.43%.

ABSTRAK

Memandangkan MOSFET telah mencapai had dari segi ciri fizikal dan elektrik yang sukar untuk terus dihasilkan kerana tahap kesukaran dan kerumitan. Walaupun, FinFET memberikan beberapa kelebihan tetapi terdapat beberapa kelemahan FinFET seperti kos fabrikasi yang tinggi, sukar untuk mengawal voltan ambang dinamik. Oleh itu, JL FinFET telah dicadangkan untuk mengatasi kekurangan tersebut. Perbezaan utama FinFET dan JL FinFET ialah kehadiran simpang dan kecerunan kepekatan doping antara sumber dan longkang. Oleh itu, JL FinFET menawarkan kebolehskalaan yang tinggi dengan kos yang rendah, keserasian yang lebih tinggi dan parameter reka bentuk seperti kepekatan doping substrat. Kebolehpercayaan peranti telah menjadi salah satu kebimbangan utama apabila menskalakan kepada rejim nano. Terdapat banyak kerja kajian kebolehpercayaan telah dilakukan termasuklah Ketidakstabilan Suhu Bias Negatif (NBTI), Suntikan Pembawa Panas (HCI), Pecahan Dielektrik Bergantung Masa (TDDB) yang berlaku dalam MOSFET. Walau bagaimanapun, maklumat mengenai isu kebolehpercayaan untuk JL FinFET adalah sangat terhad. Oleh itu, isu kebolehpercayaan JL FinFET menjadi kebimbangan utama dan harus disiasat. Projek ini terutamanya membincangkan TDDB termasuk jenis model fizikal, tingkah laku biasa, ujian tekanan berterusan. Matlamat projek adalah untuk mereka bentuk dan mensimulasikan struktur JL FinFETs 15nm dengan TDDB. Synopsys Sentaurus TCAD akan digunakan untuk tujuan simulasi. Parameter reka bentuk untuk JL FinFET saluran-n menggunakan 15nm sebagai panjang pintu, dan 10nm untuk lebar dan ketinggian sirip. Kemudian, TDDB dengan kaedah Tegasan Voltan Malar (CVS) akan dijalankan selama lebih kurang. 10 tahun dengan 3 voltan tekanan berbeza digunakan untuk menganalisis anjakan voltan ambang 15nm JL FinFET sebelum dan selepas aplikasi tegasan untuk kebolehpercayaan jangka panjang oksida. Voltan tekanan ditentukan sebagai 0.9V, 1.35V dan 1.8V. Selain itu, ujian akan dijalankan dengan beberapa ketebalan oksida seperti 1nm, 2.5nm, 4nm, 6nm dan 10nm dengan pelbagai jenis bahan oksida seperti SiO_2, HfO_2 dan Si_3N_4. Mengikut keputusan eksperimen, JL FinFET dengan gabungan Si3N4 memberikan masa yang paling panjang untuk kegagalan berbanding dengan SiO_2 dan HfO_2 dengan julat tertinggi dalam anjakan voltan ambang iaitu 2.17% - 8.43%.

TABLE OF CONTENTS

	TITLE	PAGE
	DECLARATION	**iii**
	DEDICATION	**iv**
	ACKNOWLEDGEMENT	**v**
	ABSTRACT	**vi**
	ABSTRAK	**vii**
	TABLE OF CONTENTS	**viii**
	LIST OF TABLES	**xi**
	LIST OF FIGURES	**xiii**
	LIST OF ABBREVIATIONS	**xvi**
	LIST OF APPENDICES	**xvii**
CHAPTER 1	**INTRODUCTION**	**19**
1.1	Problem Background	19
1.2	Problem Statement	19
1.3	Research Goal	20
	1.3.1 Research Objectives	20
1.4	Scope of Works	20
1.5	Report Structure	21
CHAPTER 2	**LITERATURE REVIEW**	**22**
2.1	Introduction	22
2.2	State-of-the-Arts	22
	2.2.1 FinFETs	22
	2.2.2 Junctionless FinFETs (JL FinFETs)	23
	2.2.3 Transistor Reliability	24
	2.2.4 Time Dependent Dielectric Breakdown (TDDB)	26
	2.2.5 Type of Degradation Model	27

	2.2.6 Typical Behavior	30
	2.2.7 Constant Stress Test	34
	2.2.8 High-K (HK) dielectric	38
2.3	Summary of the Review Papers	39
CHAPTER 3	**RESEARCH METHODOLOGY**	**45**
3.1	Introduction	45
3.2	Project Flow	45
3.3	Application of TDDB stress test on the JL FinFETs Device	47
3.4	Synopsys Sentaurus Technology Computer Aided Design (TCAD) Simulation Tools	48
3.5	Project Management	49
CHAPTER 4	**RESULT AND DISCUSSION**	**51**
4.1	Introduction	51
4.2	Device Structure of 15nm JL FinFETs	51
4.3	Related Equations	52
4.4	Silicon Oxide (SiO_2) with different type of oxide thickness	53
4.5	HfO_2 with different type of oxide thickness	61
4.6	Si_3N_4 with different type of oxide thickness	68
4.7	SiO_2 with different gate stress voltage applied	75
4.8	TDDB for SiO_2	78
4.9	TDDB for HfO_2	82
4.10	TDDB for Si_3N_4	85
4.11	Summary of Simulation Result Analysis for SiO_2	89
4.12	Summary of Simulation Result Analysis for HfO_2	90
4.13	Summary of Simulation Result for Si_3N_4	91
4.14	Summary of TDDB Analysis for SiO_2, HfO_2 and Si_3N_4	92
CHAPTER 5	**CONCLUSION AND RECOMMENDATIONS**	**93**
5.1	Research Outcomes	93
5.2	Future Works and Recommendation	94

REFERENCES **95**

Appendices A – B **98 - 102**

LIST OF TABLES

TABLE NO.	TITLE	PAGE
Table 2.1	On-off current ratio for different combination of semiconductor/oxide structure of JL FinFET [3]	32
Table 2.2	Interfacial trap charges impact on temperature sensitivity [3]	33
Table 2.3	Shift in bias point with increasing density of trap charges for different combination of semiconductor/oxide structure of JL FinFET [3]	33
Table 2.4	Summarize of Review Papers	39
Table 4.1	Device Parameters of 15nm n-channel JL FinFET	52
Table 4.2	The threshold voltage of 1nm oxide thickness with different stress time for SiO_2	54
Table 4.3	The threshold voltage of 2.5nm oxide thickness with different stress time for SiO_2	55
Table 4.4	The threshold voltage of 4nm oxide thickness with different stress time for SiO_2	57
Table 4.5	The threshold voltage of 6nm oxide thickness with different stress time for SiO_2	58
Table 4.6	The threshold voltage of 10nm oxide thickness with different stress time for SiO_2	60
Table 4.7	The threshold voltage of 1nm oxide thickness with different stress time for HfO_2	61
Table 4.8	The threshold voltage of 2.5nm oxide thickness with different stress time for HfO_2	63
Table 4.9	The threshold voltage of 4nm oxide thickness with different stress time for HfO_2	64
Table 4.10	The threshold voltage of 6nm oxide thickness with different stress time for HfO_2	66
Table 4.11	The threshold voltage of 10nm oxide thickness with different stress time for HfO_2	67
Table 4.12	The threshold voltage of 1nm oxide thickness with different stress time for Si_3N_4	69

Table 4.13	The threshold voltage of 2.5nm oxide thickness with different stress time for Si_3N_4	70
Table 4.14	The threshold voltage of 4nm oxide thickness with different stress time for Si_3N_4	72
Table 4.15	The threshold voltage of 6nm oxide thickness with different stress time for Si_3N_4	73
Table 4.16	The threshold voltage of 10nm oxide thickness with different stress time for Si_3N_4	75
Table 4.17	TDDB prediction for SiO_2 with different stress time	81
Table 4.18	TDDB prediction for HfO_2 with different stress time	84
Table 4.19	TDDB prediction for Hf2 with different stress time	88
Table 4.20	The threshold voltage shift in percentage for SiO_2 with different oxide thickness	89
Table 4.21	The threshold voltage shift in percentage for HfO_2 with different oxide thickness	90
Table 4.22	The threshold voltage shift in percentage for Si_3N_4 with different oxide thickness	91
Table 4.23	TDDD prediction for different oxide thickness and material	92

LIST OF FIGURES

FIGURE NO.	TITLE	PAGE
Figure 2.1	Device structure of Planar MOSFET and FinFET [5]	23
Figure 2.2	The difference between junction and Junctionless (JL) transistor [7]	23
Figure 2.3	Electrical properties comparison between two type of transistor which are JL bulk FinFET and SOI JL nanowire transistor (JNT) [6]	24
Figure 2.4	Example of phenomenon occurs due to broken bonds [10]	25
Figure 2.5	Present of oxide before and after the stress application [10]	27
Figure 2.6	Schematic illustration of SiO_2 bonds of E model where a) normal structure b) oxygen vacancy with polarized dipole and c) broken bond (e.g., trap) [11]	28
Figure 2.7	Energy-band diagram that used to illustrate 1/E model [13]	29
Figure 2.8	Typical behavior of TDDB [11]	30
Figure2.9	The process of traps creation to break down of dielectric [9][11]	31
Figure 2.10	Accelerated TDDB experiment by using CVS [9]	34
Figure 2.11	The relationship of gate voltage with operating time [24]	34
Figure 2.12	The relationship between gate voltage applied and stress time in CCS [25]	35
Figure 2.13	The relationship between the gate leakage current and stress time [26]	36
Figure 2.14	The relationship between gate voltage applied and stress time in CCS [24]	37
Figure 2.15	The relationship between breakdown time and gate voltage [11]	37
Figure 3.1	Overall Project Flowchart	46
Figure 3.2	TDDB Test Flow of work for Time Dependent Dielectric Breakdown Stress Test Applications	48
Figure 3.3	Schedule for Project 1	49

Figure 3.4	Schedule for Project 2	50
Figure 4.1	Device Structure of n-channel JL FinFET from Synopsys Sentaurus TCAD Simulation	51
Figure 4.2	1nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for SiO_2	53
Figure 4.3	2.5nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for SiO_2	55
Figure 4.4	4nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for SiO_2	56
Figure 4.5	6nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for SiO_2	58
Figure 4.6	10nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for SiO_2	59
Figure 4.7	1nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for HfO_2	61
Figure 4.8	2.5nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for HfO_2	62
Figure 4.9	4nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for HfO_2	64
Figure 4.10	6nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for HfO_2	65
Figure 4.11	10nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for HfO_2	67
Figure 4.12	1nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for Si_3N_4	68
Figure 4.13	2.5nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for Si_3N_4	70
Figure 4.14	4nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for Si_3N_4	71
Figure 4.15	6nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for Si_3N_4	73
Figure 4.16	10nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for Si_3N_4	74
Figure 4.17	1nm, 2.5nm, 4nm, 6nm and 10nm of oxide thickness with 0.9V stress applied to the gate for SiO_2	76
Figure 4.18	1nm, 2.5nm, 4nm, 6nm and 10nm of oxide thickness with 1.35V stress applied to the gate for SiO_2	77

Figure 4.19 1nm, 2.5nm, 4nm, 6nm and 10nm of oxide thickness with 1.8V stress applied to the gate for SiO_2 77

Figure 4.20 TDDB prediction for 1nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for SiO_2 79

Figure 4.21 TDDB prediction for 2.5nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for SiO_2 79

Figure 4.22 TDDB prediction for 4nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for SiO_2 80

Figure 4.23 TDDB prediction for 6nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for SiO_2 80

Figure 4.24 TDDB prediction for 10nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for SiO_2 81

Figure 4.25 TDDB prediction for 1nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for HfO_2 82

Figure 4.26 TDDB prediction for 2.5nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for HfO_2 83

Figure 4.27 TDDB prediction for 4nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for HfO_2 83

Figure 4.28 TDDB prediction for 6nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for HfO_2 84

Figure 4.29 TDDB prediction for 10nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for HfO_2 84

Figure 4.30 TDDB prediction for 1nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for Si_3N_4 86

Figure 4.31 TDDB prediction for 2.5nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for Si_3N_4 86

Figure 4.32 TDDB prediction for 4nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for Si_3N_4 87

Figure 4.33 TDDB prediction for 6nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for Si_3N_4 87

Figure 4.34 TDDB prediction for 10nm of oxide thickness with 0.9V, 1.35V and 1.8V stress applied to the gate for Si_3N_4 88

LIST OF ABBREVIATIONS

DIBL	-	Drain Induced Barrier Lowering
SCE	-	Short Channel Effect
EM	-	Electromigration
NBTI	-	Negative Bias Temperature Instability
HCI	-	Hot Carrier Injection
TDDB	-	Time Dependent Dielectric Breakdown
MOS	-	Metal Oxide Semiconductor
CVS	-	Constant Voltage Stress
JL	-	Junctionless
TCAD	-	Technology Computer Aided Design
ESD	-	Electrostatic Discharge
RBD	-	Radiation Induced Gate Rupture
IC	-	Integrated Circuit
F-N	-	Fowler-Nordheim
SILC	-	Stress Induced Leakage Current
SBD	-	Soft Breakdown
HBD	-	Hard Breakdown
CCS	-	Constant Current Stress
JNT	-	JL Nanowire Transistor
MOL	-	Middle-of-Line
SWB	-	Sentaurus Workbench Setup
SDE	-	Sentaurus Structure Editor
SNMESH	-	Sentaurus Mesh
SDevice	-	Sentaurus Device
SS	-	Subthreshold Swing
SiO_2	-	Silicon Oxide
HfO_2	-	Hafnium Oxide
Si_3N_4	-	Silicon Nitride

LIST OF APPENDICES

APPENDIX	TITLE	PAGE
Appendix A	SDE: Command for 15nm n-channel FinFET	98
Appendix B	SDevice: Command for $I_D - V_G$ Graph Simulation	102

CHAPTER 1

INTRODUCTION

1.1 Problem Background

FinFETs also known as Tri-Gate transistor and multi-gate transistor. It has designed to overcome the bottleneck in terms of increasing the number or transistor density and performance of planar MOSFET. Although, FinFETs provide several advantages like superior performance in terms of lower power consumption, lower leakage current, better Drain Induced Barrier Lowering (DIBL), suppressed short-channel effect (SCE) and others. There are some drawbacks of FinFETs such as higher fabrication cost, difficult to control dynamic threshold voltage, higher capacitance, corner effect etc. Therefore, JL FinFETs has been proposed to overcome the shortcoming such as fabrication cost, higher scalability, higher compatibility, lower degradation of mobility with gate voltage and more.

1.2 Problem Statement

In recent, reliability of device has become one of the major concerns when scaling to nano regime. Therefore, there are many research papers regarding reliability issue such as electromigration (EM), Negative Bias Temperature Instability (NBTI), Hot Carrier Injection (HCI), Time-dependent Dielectric Breakdown (TDDB) that occurs in MOS structure device can be easily found from internet source [1]. However, the researcher paper and information regarding reliability issue for JL FinFETs is very limited. This happens due to JL FinFETs can be considered as type of new technology at this moment. Also, a thinner gate dielectric which is lesser than 10nm with aggressive scaling down of the device geometries will affect the long-term reliability and integrity of the oxide layer. Therefore, the reliability issue of JL FinFETs become a primary concern and should be investigated.

1.3 Research Goal

This project aims to design and simulate a 15nm n-channel JL FinFETs device structure with TDDB test applications. TDDB test will be carried out with Constant Voltage Stress (CVS) varies with stress time and understand the degradation of the electrical characteristic of the proposed device before and after VS applications to the gate. will be designed and simulated by using Synopsys Sentaurus TCAD.

1.3.1 Research Objectives

The objectives of the research are:

(1) To design a device structure for 15nm n-channel JL FinFETs

(2) To study TBDD reliability issues of 15nm n-channel JL FinFETs including the typical behaviour, type of stress etc.

(3) To analyze the threshold voltage shift after stress application of 15nm n-channel JL FinFETs for different oxide thickness and different oxide material.

1.4 Scope of Works

The scope of the research are:

(1) The best optimized design structure for n-channel JL FinFETs using 15nm as the gate length, and 10nm for width and height of the fin.

(2) TDDB test will be applied to the designed JL FinFETs by using CVS for approx. 10 years in order to predict the functionality of device.

(3) TDDB will be carried out by applying CVS method to the designed 15nm n-channel JL FinFETs for 1nm, 2.5nm, 4nm, 6nm and 10nm with several type of material such as SiO_2, HfO_2 and Si_3N_4.

(4) Characterize the performance of electrical properties for 15nm n-channel JL FinFETs before vs after the stress application

(5) Synopsys Sentaurus TCAD Simulation will be used to simulate the reliability test and the performance will be investigated based on the I-V characteristic, leakage current with stress time etc.

1.5 Report Structure

The structure of the report will be organized into several chapters which are Chapter 2: Literature Review discuss about the device structure of FinFETs, JL FinFETs, common reliability issue including the fundamental knowledge about TDDB. Besides, Chapter 3: Research Methodology describe the design, model, parameters, and project flow by using Synopsys Sentaurus TCAD Tools Simulation. Also, Chapter 4: Result and discussion which demonstrate concept for the entire project. Lastly, Chapter 5 will be the conclusion of the project including the future work and recommendation where the reference list and appendixes will be attached at the end of project.

REFERENCES

[1] S. Shaheen, G. Golan, M. Azoulay, and J. Bernstein, “A comparative study of reliability for finfet,” Facta Univ. - Ser. Electron. Energ., vol. 31, no. 3, pp. 343–366, 2018, doi: 10.2298/fuee1803343s.

[2] D. Bhattacharya and N. K. Jha, “FinFETs: From devices to architectures,” Digit. Analog Analog. Digit. IC Des., vol. 2014, pp. 21–55, 2015, doi: 10.1017/CBO9781316156148.003.

[3] N. Garg, Y. Pratap, M. Gupta, and S. Kabra, “Reliability Assessment of GaAs/AlO Junctionless FinFET in the Presence of Interfacial Layer Defects and Radiations,” IEEE Trans. Device Mater. Reliab., vol. 20, no. 2, pp. 452–458, 2020, doi: 10.1109/TDMR.2020.2991662.

[4] C. Cheng, “Lecture 1: Introduction to Digital Logic Design CSE 140: Components and Design Techniques for Digital Systems Winter 2016.” [Online]. Available: https://cseweb.ucsd.edu/classes/wi16/cse140-a/slides/lec1.pdf.

[5] “FinFET Physics,” www.mksinst.com. https://www.mksinst.com/n/finfet-physics.

[6] M. H. Han, C. Y. Chang, H. Bin Chen, J. J. Wu, Y. C. Cheng, and Y. C. Wu, “Performance comparison between bulk and SOI junctionless transistors,” IEEE Electron Device Lett., vol. 34, no. 2, pp. 169–171, 2013, doi: 10.1109/LED.2012.2231395.

[7] Y. Yin, “Simulation Study of Vertical Pillar Transistor and Ge Gate-All-Around FET 2015” [Online]. Available: oral defense_07212012 (slideshare.net)

[8] C. C. Chen, T. Liu, S. Cha, and L. Milor, “Processor-level reliability simulator for time-dependent gate dielectric breakdown,” Microprocess. Microsyst., vol. 39, no. 8, pp. 950–960, 2015, doi: 10.1016/j.micpro.2015.10.002.

[9] S. M. Warnock, “Dielectric reliability in high-voltage GaN metal-insulator-semiconductor high electron mobility transistors,” dspace.mit.edu, 2017. https://dspace.mit.edu/handle/1721.1/112032 (accessed Feb. 03, 2022).

[10] M. A. Alam and W. Lafayette, “A Broad Overview of Reliability of Semiconductor MOSFET Warranty, product recall and other facts of life.”

[11] A. Ghetti, “Gate Oxide Reliability: Physical and Computational Models,” pp. 201–258, 2004, doi: 10.1007/978-3-662-09432-7_6.

[12] D. Faure, D. Bru, C. Ali, C. Giret, and K. Christensen, "Gate oxide breakdown characterization on 0.13μm CMOS technology," Microelectron. Reliab., vol. 43, no. 9–11, pp. 1519–1523, 2003, doi: 10.1016/S0026-2714(03)00269-5.

[13] T. K. S. Wong, "Time Dependent Dielectric Breakdown in Copper Low-k Interconnects: Mechanisms and Reliability Models," Materials, vol. 5, no. 9, pp. 1602–1625, Sep. 2012, doi: 10.3390/ma5091602.

[14] J. W. McPherson, "Time dependent dielectric breakdown physics - Models revisited," Microelectron. Reliab., vol. 52, no. 9–10, pp. 1753–1760, 2012, doi: 10.1016/j.microrel.2012.06.007.

[15] J. H. Lim et al., "Correct Extrapolation Model for TDDB of STT-MRAM MgO Magnetic Tunnel Junctions," IEEE Int. Reliab. Phys. Symp. Proc., vol. 2019-March, pp. 3–9, 2019, doi: 10.1109/IRPS.2019.8720611.

[16] J. McPherson, V. Reddy, K. Banerjee, and H. Le, "Comparison of E and 1/E TDDB models for SiO2 under long-term/low-field test conditions," Tech. Dig. - Int. Electron Devices Meet., pp. 171–174, 1998, doi: 10.1109/iedm.1998.746310.

[17] A. Toriumi and H. Satake, "A study of dielectric breakdown mechanism through the statistical analysis of post-breakdown resistance of thin SiO2 films," Sci. Technol. Adv. Mater., vol. 1, no. 3, pp. 181–186, 2000, doi: 10.1016/S1468-6996(00)00015-2.

[18] I. Hirano *et al.*, "Time-dependent dielectric breakdown (TDDB) distribution in n-MOSFET with HfSiON gate dielectrics under DC and AC stressing," *Microelectron. Reliab.*, vol. 53, no. 12, pp. 1868–1874, 2013, doi: 10.1016/j.microrel.2013.05.010.

[19] A. Kerber, E. Cartier, B. P. Linder, S. A. Krishnan, and T. Nigam, "TDDB failure distribution of metal gate / high-k CMOS devices on SOI substrates," IEEE Int. Reliab. Phys. Symp. Proc., pp. 505–509, 2009, doi: 10.1109/IRPS.2009.5173304.

[20] M. Jo, C. Y. Kang, K. W. Ang, J. Huang, P. Kirsch, and R. Jammy, "Understanding and improving SILC behavior under TDDB stress in full gate-last high-k/metal gate nMOSFETs," Int. Symp. VLSI Technol. Syst. Appl. Proc., vol. 12, pp. 11–12, 2012, doi: 10.1109/VLSI-TSA.2012.6210154.

[21] S. Sahhaf, R. Degraeve, P. J. Roussel, T. Kauerauf, B. Kaczer, and G. Groeseneken, "TDDB reliability prediction based on the statistical analysis of hard breakdown including multiple soft breakdown and wear-out," Tech. Dig. - Int. Electron Devices Meet. IEDM, no. l, pp. 501–504, 2007, doi: 10.1109/IEDM.2007.4418984.

[22] K. Park, K. Park, S. Im, S. Hong, K. Son, and J. Jeon, "Development of an advanced TDDB analysis model for temperature dependency," Electron., vol. 8, no. 9, 2019, doi: 10.3390/electronics8090942.

[23] "TDDB / soft breakdown (SBD), progressive breakdown (PBD) and hard breakdown (HBD)," 네이버 블로그 | 에프램 EFRAM. https://m.blog.naver.com/framkang/220718595715.

[24] T. Dependent and D. Breakdown, "21. Lecture 21: Introduction to Dielectric Breakdown 21.1," pp. 98–112.

[25] J. Shen et al., "The TDDB Characteristics of Ultra-Thin Gate Oxide MOS Capacitors under Constant Voltage Stress and Substrate Hot-Carrier Injection," Advances in Condensed Matter Physics, vol. 2018, p. e5483756, May 2018, doi: 10.1155/2018/5483756.

[26] H. Kim et al., "A systematic study of gate dielectric TDDB in FinFET technology," IEEE Int. Reliab. Phys. Symp. Proc., vol. 2018-March, pp. 4A.41-4A.44, 2018, doi: 10.1109/IRPS.2018.8353577.

[27] J. Dabrowski and E. R. Weber, Predictive simulation of semiconductor processing: status and challenges. Berlin; London: Springer, 2011.

[28] F. Tao et al., "TDDB characteristic and breakdown mechanism of ultra-thin SiO 2/HfO2 bilayer gate dielectrics," J. Semicond., vol. 35, no. 6, pp. 2–7, 2014, doi: 10.1088/1674-4926/35/6/064003.

[29] Nirmal, V. Kumar, P. C. Samuel, Shruthi, D. M. Thomas and M. Kumar,"Analysis of dual Gate Mosfets using high k dielectrics," 2011 3rd International Conference on Electronics Computer Technology, 2011, pp. 22-25, doi: 10.1109/ICECTECH.2011.5941552.

[30] T. E. Kopley, M. Ring, C. Choi, and J. Colbath, "Combined Vramp and TDDB analysis for gate oxide reliability assessment and screening," IEEE Int. Integr. Reliab. Work. Final Rep., vol. 2016-March, no. October, pp. 138–142, 2016, doi: 10.1109/IIRW.2015.7437087.