WIRELENGTH ESTIMATION IN VLSI CELL PLACEMENT USING MACHINE LEARNING TECHNIQUES

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DEDICATION

To my parents, siblings, friends, and supervisor

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ABSTRACT

In recent years, artificial intelligence (AI) plays an important role in Very Large-Scale Integration (VLSI) circuit design for wirelength prediction of cell placement. As compared to conventional wirelength estimation techniques such as Half-Perimeter Wirelength (HPWL) and Rectilinear Steiner Minimal Tree (RSMT), wirelength prediction using AI does provide the results with higher accuracy within a shorter runtime. Therefore, this paper aims to implement and investigate the performance of several machine learning-based wirelength estimation models on the International Symposium on Physical Design (ISPD) 2011 circuit benchmark. Machine learning models such as Artificial Neural Network (ANN), Support Vector Machine (SVM) and Random Forest (RF), are introduced in this paper. Besides, this paper also targets to integrate the machine learning model with the best accuracy and runtime, into actual placement. The results indicate that RF is the best choice for replacement of conventional method as RF achieved an accuracy of more than 90% for wirelength estimation, and the runtime taken by RF is approximately 10000s much faster than RSMT.

ABSTRAK

Pada era globalisasi ini, kecerdasan buatan (AI) memainkan peranan penting dalam reka bentuk litar penyepaduan skala sangat besar (VLSI) untuk kegunaan penganggaran panjang wayar dalam prosedur penempatan sel. Berbanding dengan teknik penganggaran panjang wayar konvensional seperti Half-Perimeter Wirelength (HPWL) dan Rectilinear Steiner Minimal Tree (RSMT), penganggaran panjang wayar melalui AI boleh menghasilkan keputusan dengan ketepatan yang lebih tinggi dalam masa yang singkat. Oleh itu, kajian ini bertujuan untuk melaksana dan menyiasat prestasi beberapa model anggaran panjang wayar berasaskan pembelajaran mesin pada penanda aras litar International Symposium on Physical Design (ISPD) 2011. Model pembelajaran mesin seperti Rangkaian Neural Buatan (ANN), Mesin Vektor Sokongan (SVM) dan Random Forest (RF), diperkenalkan dalam kajian ini. Selain itu, kajian ini juga bertujuan untuk menyepadu model pembelajaran mesin dengan ketepatan terbaik dalam masa yang singkat ke dalam penempatan sel. Keputusan kajian ini menunjukkan bahawa RF adalah pilihan terbaik sebagai penggantian kaedah konvensional kerana RF telah mencapai ketepatan yang lebih daripada 90% bagi penganggaran panjang wayar, dan masa operasi diguna oleh RF adalah agak 10000 saat lebih pantas daripada RSMT.

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LIST OF ABBREVIATIONS

AI	-	Artificial Intelligence
ANN	-	Artificial Neural Network
CSV	-	Comma Separated Value
EDA	-	Electronic Design Automation
HPWL	-	Half-Perimeter Wirelength
IC	-	Integrated Circuit
ISPD	-	International Symposium on Physical Design
MLP	-	Multilayer Perceptron
MSE	-	Mean Squared Error
NP	-	Non-Deterministic Polynomial
RF	-	Random Forest
RMST	-	Rectilinear Minimum Spanning Tree
RSMT	-	Rectilinear Steiner Minimal Tree
SA	-	Simulated Annealing
SVM	-	Support Vector Machine
SVR	-	Regression Based Support Vector Machine
VLSI	-	Very-Large Scale Integration

LIST OF SYMBOLS

ε	-	Tolerance Margin
e	-	Net
i	-	Pin
p	-	Number of Terminal
L_{ϵ}	-	Loss Function
R^2	-	Coefficient of Determination
T	-	Temperature

CHAPTER 1

INTRODUCTION

1.1 Research Background

The design and optimization of integrated circuits (IC) are essential to the manufacturing of semiconductor chips. Recent advances in semiconductor technologies does make the modern Very-Large Scale Integration (VLSI) design becomes more complex and sophisticated. VLSI physical design continues as one of the appealing and arduous areas in the field of Electronic Design Automation (EDA) [1]. The main processes included in VLSI physical design are netlist synthesis, partitioning, floorplanning, placement, routing, and timing closure. In this paper, VLSI cell placement will be mainly discussed.

VLSI cell placement is a crucial stage in determining the positions and orientations of each cell in a layout while also addressing optimization objectives [2]. Placement is a stage in VLSI design flow where cell locations are identified which affects the timing, routability, power consumption and performance of an IC [3]. The conventional VLSI standard cell placement are divided into three main stages, which are global placement, legalization, and detailed placement. In general, global placement generates an initial placement with minimum total Half-Perimeter Wirelength (HPWL) and tries to hit some optimization targets such as routability, timing and so on. Few cells overlap as a result, and the cells are not aligned with the rows. Next, legalization starts to remove unwanted cell overlaps, to put all cell instances on the rows in the core area, and to reduce the displacements of cell instances between initial and legalized placements. Lastly, detailed placement is applied in order to enhance the quality of the results of legalized placement [3].

The main objective of placement optimization is to estimate the coordinates of all cells of a given netlist so that the total wirelength of the netlist can be minimised

[4]. Reduction of total wirelength of a circuit is a must in VLSI design flow, because the total wirelength does affect the maximum clock frequency, power consumption, routability, and the cost of manufacturing for a given design [5]. With the less wirelength and routing demand, routability can be improved in a design. Plus, the performance of the circuits can be better with shorter wirelength since shorter wirelength has less delays of interconnects, and a shorter wirelength also introduces less capacitive loads [6].

As the rapid evolution of the industrial technologies, some requirements on improving the techniques for VLSI cell placement are needed in order to reduce the computational power and runtime. In recent years, Artificial Intelligence (AI) is seen as the alternative replacement for parts of conventional VLSI physical design flow. AI is the processing of human intelligence by computers, particularly computer systems. This includes learning, reasoning, and self-correction. [7]. There are abundant of AI models or algorithms used in the industry nowadays, which can be classified into three main classes, which are deep learning, machine learning and neural network.

As a subset of AI, machine learning is a class of algorithm that automatically extract information from datasets or prior knowledge. As a data-driven strategy, machine learning is a supplement to analytical models that are widely used in EDA tools for VLSI physical design [8]. In this paper, several machine learning algorithms will be mainly discussed as the replacement of the conventional method in VLSI standard cell placement.

1.2 Problem Statement

Finding non-overlapping row and site aligned positions for cells while minimising the design's total wirelength is the challenge of standard cell placement [5]. In recent years, there are several wirelength estimation techniques been adopted in the semiconductor industries as the cell placement algorithm used in VLSI physical design of an IC. Popular algorithms used in the industries are HPWL model, Rectilinear Minimum Spanning Tree (RMST) model, Rectilinear Steiner Minimum

Tree (RSMT) model and so on. Some pros and cons are observed when these algorithms are used in standard cell placement.

HPWL model is the most popular choice as the wirelength reduction algorithm in standard cell placement nowadays in the industry. HPWL is computationally easy and thus a shorter runtime is required when estimating the total wirelength of the design. However, HPWL does make accurate and precise wirelength estimation for smaller netlists. When the size of the netlists grows larger, the accuracy of the wirelength estimation drops drastically when HPWL is used, although simple computation and less runtime are taken [5].

In contrast, RSMT does provide a much accurate wirelength estimation than HPWL model. RSMT is a Non-Deterministic polynomial (NP) model, which is computationally complex and requires a high runtime complexity [6], [9]. As the size of the design increases, more runtime is needed for the NP-complete RSMT model, in order to obtain the accurate estimation. In practice, RMST is preferred to be used instead of RSMT, but the estimated wirelength of RMST is much longer than that of RSMT since Steiner node is not allowed in RMST model [6]. Besides, the quality of floorplan is mainly dependent on the total wirelength in cell placement design. Thus, if the total wirelength is predicted inaccurately, the quality of the floorplan will be affected too.

As the rapid growth of the technology, AI has been introduced as one of the main solutions in replacing the conventional wirelength estimation techniques in standard cell placement, in order to overcome the issues faced when conventional techniques are used. In this paper, several machine learning algorithms such as Artificial Neural Network (ANN), Support Vector Machine (SVM) and Random Forest (RF) regression, are introduced as the replacements of the conventional techniques in VLSI standard cell placement.

1.3 Research Objectives

The objectives of this paper are:

(a) To develop machine learning algorithms for wirelength estimation.

(b) To evaluate, analyse and compare different wirelength estimation techniques which include both conventional and machine learning methods.

(c) To integrate machine learning wirelength estimation into actual placement algorithm.

1.4 Research Scope

The scope of this paper includes the development, evaluation, and comparison between conventional cell placement algorithms, which are HPWL, RMST and RSMT models, and machine learning-based wirelength estimation algorithms.

Besides, the results from the machine learning-based model with the best optimum accuracy and runtime are tested with actual placement, with Simulated Annealing (SA) algorithm is applied to investigate the quality of the placed floorplan. Python programming language is preferred to be used for implementing the algorithms in this paper. The International Symposium on Physical Design (ISPD) 2011 Routability-Driven Placement Contest and Benchmark Suite is imported as the placement circuits used in this paper.

1.5 Thesis Outline

Introduction, Literature Review, Methodology, Result and Discussion and Conclusion are the five main chapters that make up this paper. Introduction is the first chapter of this paper which describes about the research background, problem statement, research objectives, scope of research and the thesis outline.

The following chapter discusses about the literature review of previous works that related to this research. Some of the theoretical background of the research and the techniques of using both conventional and machine learning techniques are mainly discussed.

Chapter 3 shares the methodology of the research. The workflow of the research will be discussed step by step in detail. Flowcharts and the functions of algorithm used are highlighted in this chapter.

The next chapter discusses about the results obtained after the completion of the workflow of the research. Graphs are presented in this chapter to discuss about the performances of both conventional and machine learning approaches after estimations are done.

The last chapter summaries the overall research. Suggestions for further improvements in the future are discussed in this chapter too.

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