PERFORMANCE EVALUATION OF GRAPHENE NANORIBBON-BASED DIFFERENTIAL AMPLIFIER

CHAN JIA ZHEN

UNIVERSITI TEKNOLOGI MALAYSIA

PERFORMANCE EVALUATION OF GRAPHENE NANORIBBON-BASED DIFFERENTIAL AMPLIFIER

CHAN JIA ZHEN

A project report submitted in partial fulfilment of the
requirements for the award of the degree of
Master of Engineering (Computer and Microelectronic Systems)

School of Electrical Engineering
Faculty of Engineering
Universiti Teknologi Malaysia

JULY 2022

DEDICATION

To my mother, sister, supervisor, and my friends.

ACKNOWLEDGEMENT

First and foremost, I would like to express my gratitude to my project supervisor, Ts. Dr. Zaharah Binti Johari throughout this project. I am appreciated the suggestion given by my supervisor while I am facing the problem in this project. I would like to thank her for sharing her experience and knowledge in completing this project.

Besides, I would like to thank my course mates who are taking same UTM master course with me. With their technical and spiritual supports, I can complete my project. I would like to thank them for giving suggestion when I am facing issue in my project.

Lastly, I would like to thank my family members who are giving spiritual support during my project. With their support, I can complete my project even I am facing a lot of problem.

ABSTRACT

The evolution of transistor for many device applications have been following the Moore's Law prediction. The downsizing of transistor to meet design specification may lead to numerous issues related to short channel effect such as leakage current, tunnel effect and increase in power dissipation. To mitigate these issues, nanomaterial is proposed to replace silicon as one of the potential solution. Graphene is an alternative material with its high mobility and high thermal conductivity. Nanoribbon is etched in graphene to convert its metal properties to semiconductor. In this research, differential amplifier is constructed based on graphene device. The performance of graphene based differential amplifier is then compared with silicon-based material for L=32nm. This study used HSPICE for circuit construction and simulation with established graphene nanoribbon SPICE model. Current mirror concept is applied at load of differential amplifier. The number of ribbons is set as 6 and graphene dimer line, N is varied to evaluate performance in term of differential mode gain, common mode gain and CMRR. From simulation result, the highest differential mode gain is 2.59 at N=19 and the lowest common mode gain is 0.12 at N=9. GNRFET based differential amplifier has the best performance with highest CMRR of 18.05 at N=19. While comparing with Si-MOSFET based differential amplifier, GNRFET based differential amplifier is 11.16% higher in differential mode gain, 39.13% lower in common mode gain and 82.14% higher in CMRR. Hence, GNRFET based differential amplifier is 82.14% better performance than Si-MOSFET based differential amplifier. The outcome of this study can be guideline for future study on circuit implementation using graphene material.

ABSTRAK

Evolusi transistor untuk banyak aplikasi peranti telah mengikuti ramalan Undang-undang Moore. Pengurangan saiz transistor untuk memenuhi spesifikasi reka bentuk boleh menyebabkan banyak masalah yang berkaitan dengan kesan saluran pendek seperti arus kebocoran, kesan terowong dan peningkatan pelesapan kuasa. Untuk mengurangkan masalah ini, nanomaterial dicadangkan untuk menggantikan silikon sebagai salah satu penyelesaian yang berpotensi. Graphene adalah bahan alternatif dengan mobiliti yang tinggi dan kekonduksian terma yang tinggi. Nanoribbon terukir di graphene untuk menukar sifat logam menjadi semikonduktor. Dalam penyelidikan ini, penguat pembezaan dibina berdasarkan peranti graphene. Prestasi penguat pembezaan berasaskan graphene kemudian dibandingkan dengan bahan berasaskan silikon dalam L = 32nm. Kajian ini menggunakan HSPICE untuk pembinaan litar dan simulasi dengan graphene nanoribbon SPICE model. Konsep cermin semasa digunakan pada beban penguat pembezaan. Bilangan pita ditetapkan sebagai 6 and garis dimer, N diubah untuk menilai prestasi dari segi keuntungan mod pembezaan, keuntungan mod biasa dan CMRR. Dari hasil simulasi, keuntungan mod pembezaan tertinggi adalah 2.59 pada N = 19 dan keuntungan mod biasa terendah adalah 0.12 pada N = 9. Penguat pembezaan berasaskan GNRFET mempunyai prestasi terbaik dengan CMRR tertinggi adalah 18.05 pada N = 19. Semasa membandingkan dengan penguat pembezaan berasaskan Si-MOSFET, penguat pembezaan berasaskan GNRFET adalah 11.16% lebih tinggi dalam keuntungan mod pembezaan, 39.13% lebih rendah dalam keuntungan mod biasa dan 82.14% lebih tinggi dalam CMRR. Oleh itu, penguat pembezaan berasaskan GNRFET mempunyai prestasi yang 82.14% lebih baik daripada penguat pembezaan berasaskan Si-MOSFET. Hasil kajian ini dapat menjadi panduan untuk kajian masa depan mengenai pelaksanaan litar menggunakan bahan graphene.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

ADC	-	Analog-Digital Convertor
ALU	-	Arithmetic Logic Unit
CMOS	-	Complementary Metal Oxide Semiconductor
CMRR	-	Common Mode Rejection Ratio
CNFET	-	Carbon Nanotube Field Effect Transistor
EDP	-	Energy Delay Product
FOM	-	Field Of Merit
GNR	-	Graphene Nanoribbon
GNRFET	-	Graphene Nanoribbon Field Effect Transistor
IC	-	Integrated Circuit
ICMR	-	Input Common Mode Ratio
IRDS	-	International Roadmap of Device and System
MOSFET	-	Metal Oxide Silicon Field Effect Transistor
PD	-	Propagation Delay
PDP	-	Power Delay Product
PTM	-	Predictive Technology Model
SNM	-	Static Noise Margin
SRAM	-	Static Random Access Memory

LIST OF SYMBOLS

A_{cm}	-	Common mode gain
A_{dm}	-	Differential mode gain
dop	-	Source and Drain reservoirs doping fraction
Ge	-	Graphene
L_{ch}	-	Channel length
N	-	Dimer line
n_{ribbon}	-	Number of Ribbon
p	-	Edge roughness percentage of the device
T_{ox}	-	Thickness of oxide
V_{dd}	-	Total input voltage
V_{p-p}	-	Peak to peak voltage
W_{ch}	-	Channel width
W_{gate}	-	Gate width
W_{sp}	-	Ribbon spacing

CHAPTER 1

INTRODUCTION

1.1 Research Background

Moore's Law was introduced by Gordon Moore in 1965 from his observation on the development of semiconductor industry. Moore's Law states that the number of transistors in an integrated circuit (IC) was doubled for every two years. Moore's Law is further amended to show the actual growth of transistor density in an IC. The period for doubling number of transistors in an IC has been reduced from two years to eighteen months [1]. Moore's Law has accelerated the development of semiconductor industry. To match Moore's Law, the size of transistors had been decreased to increase the numbers of transistors which can be placed in an IC and further increased the number of ICs which can fabricate in a silicon wafer. However, complexity in scaling down the size of transistor slows down Moore's Law and hinders semiconductor industry's technology development. Figure 1.1 shows Moore's Law diagram for the increasing in transistor number of Intel processors before 2010 [2].

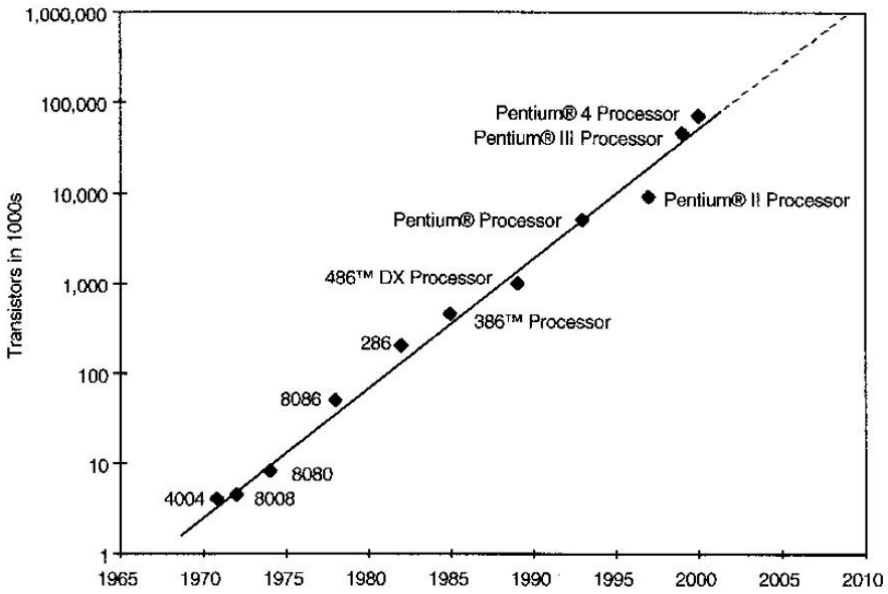

Figure 1.1 Moore's Law diagram [2].

Big data technology is the future trend in semiconductor industry. The Moore's scaling technology brings disadvantages in power and interconnect bandwidth which can be big challenge for big data and instant data technology field. Instant data requires ultra-low power devices with "always on" and high-performance devices to generate the data instantly. Abundant computing, communication bandwidth and memory resources are the requirement for big data field to generate the service and information for clients [3]. In International Roadmap Device and System (IRDS), CMOS scaling technology with reducing in power and cost at the same time is a challenge in More Moore roadmap.

Besides, CMOS scaling technology will reach its fundamental limit. Hence, new information processing devices and microarchitectures will explore and further improve the IC scaling technology. In IRDS Beyond CMOS roadmap, five difficult challenges are listed and one of them are extending CMOS scaling. The solution provided to face this challenge is by developing new materials to replace silicon such as Ge and carbon group as alternative channel which can increase saturation velocity and further reduce voltage supply, Vdd and power dissipation in MOSFET and hence reduce current leakage [3]. Figure 1.2 shows the relationship of More Moore, Beyond CMOS and Novel Computing Paradigms and Application [3].

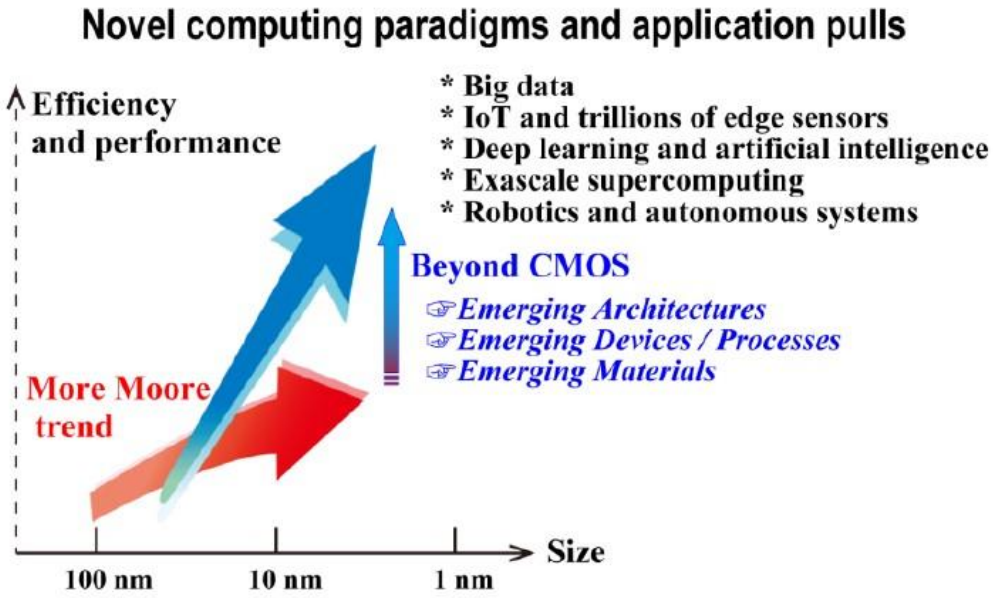

Figure 1.2 Relationship of More Moore, Beyond CMOS and Novel Computing Paradigms and Application [3].

1.2 Problem Statement

From Moore's Law, the number of transistors in an IC is doubled over two years. The size of transistors must be as small as possible to match Moore's Law over year. However, CMOS scaling technology has reached its limitation which brings many issues. The downsizing of transistor's channel length to match Moore's Law brings side effect to the performance of MOSFET such as tunnel effects, increasing in leakage current, increasing in power dissipation and reducing in carrier saturation velocity. To overcome these issues, nanomaterials such as graphene is an alternative material. Graphene has been studied for several applications such as full adder, half adder, logic gate, encoder, and ADC.

There is much research have been done on differential amplifier [19] to [25]. Researchers concluded that CMRR must be high to reject environment noise signal and hence improve the performance of differential amplifier. However, little study has attempted to used graphene for differential amplifier application. Therefore, graphene-based transistor is proposed to construct differential amplifier in this study. It is important to achieve high CMRR since it makes sure the common mode signal or noise is rejected and output voltage is amplified by the differential pair input voltage. The outcome can be compared with carbon nanotube (CNT) to fully exploited graphene potential.

1.3 Research Objective

This study aimed to analyze the performance of new material which is GNR for differential amplifier in term of CMRR and gains. In short, the research embarked on the following objectives:

1. To study the performance of GNR based differential amplifier in terms of Common Mode Rejection Ratio (CMRR) and voltage.

2. To investigate the effect of varying GNR dimer line with CMRR and voltage gain.

3. To compare the CMRR of GNR based differential amplifier with Silicon based at 32nm technology nodes.

1.4 Research Scope

Based on the research objectives, the scope of this thesis work is listed below:

- The design and simulation are using HSPICE tool.
- The GNR SPICE model is adopted from Ying Yu Chen, et al. [4].
- The performance of the differential amplifier is focused on CMRR and voltage gains.
- The netlist file for Si MOSFET transistor at 32nm technology node is adopted from PTM model [5].
- The dimer line of the GNR is from 8 to 20.

1.5 Dissertation Outline

This dissertation is divided into five parts which are Introduction, Literature Review, Methodology, Result and Discussion and Conclusion. The first chapter is Introduction which discusses about research background, problem statement, research objectives, research scopes and dissertation outline.

Second chapter is Literature Review which discusses about the previous work that related to the research. In this chapter, the review on differential amplifier, GNRFET application and related work are discussed.

Next chapter discusses the methodology of research. The workflow is discussed and the step to carry out in the research is described. Parameters of GNRFET used to build differential amplifier are tabulated in table.

Chapter 4 is results and discussions which shares the simulation result of differential amplifier. The performance analysis of GNRFET based differential amplifier is carried out in term of CMRR and voltage gains with varying parameters of GNRFET which is dimer line. The performance of differential amplifier is compared between GNRFET based and Si-MOSFET based in this chapter too.

The last chapter summarize the overall research that have been done. This include some suggestions on further improvement that can be made.

REFERENCES

[1] M. Gianfagna, “What is Moore’s Law?,” *Synopsys*. https://www.synopsys.com/glossary/what-is-moores-law.html# (accessed Dec. 01, 2021).

[2] J. Vanston, “BETTERFORECASTS, BETTERPLANS, BETTERRESULTS Enhance the validity and credibility of your forecasts by structuring them in accordance with the five different ways people view the future,” Jul. 2022.

[3] “THE INTERNATIONAL ROADMAP FOR DEVICES INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS 2017 EDITION EXECUTIVE SUMMARY THE IRDS IS DEVISED AND INTENDED FOR TECHNOLOGY ASSESSMENT ONLY AND IS WITHOUT REGARD TO ANY THE INTERNATIONAL ROADMAP FOR DEVICES,” 2018.

[4] C. Ying-Yu, G. Morteza, R. Artem, S. Amit, and C. Deming, “SPICE Model of Graphene Nanoribbon FETs (GNRFET).” Jul. 2013. [Online]. Available: https://nanohub.org/resources/17074

[5] Predictive Technology Model, “CMOS Model.” http://ptm.asu.edu/ (accessed Dec. 07, 2021).

[6] C. Stampfer *et al.*, “Transport in graphene nanostructures,” *Frontiers of Physics*, vol. 6, no. 3, pp. 271–293, 2011, doi: 10.1007/s11467-011-0182-3.

[7] A. A. Balandin, “Thermal properties of graphene and nanostructured carbon materials,” *Nature Materials*, vol. 10, no. 8, pp. 569–581, 2011, doi: 10.1038/nmat3064.

[8] Y. Y. Chen, A. Sangai, M. Gholipour, and D. Chen, “Graphene nano-ribbon field-effect transistors as future low-power devices,” in *Proceedings of the International Symposium on Low Power Electronics and Design*, 2013, pp. 151–156. doi: 10.1109/ISLPED.2013.6629286.

[9] E. McCann, “Asymmetry gap in the electronic band structure of bilayer graphene,” *Physical Review B*, vol. 74, Aug. 2006, doi: 10.1103/PhysRevB.74.161403.

[10] X. Jia, J. Campos-Delgado, M. Terrones, V. Meunier, and M. S. Dresselhaus, "Graphene edges: a review of their fabrication and characterization," *Nanoscale*, vol. 3, no. 1, pp. 86–95, 2011, doi: 10.1039/C0NR00600A.

[11] S. Almusallam and A. Ashkanani, "Differential Amplifier using CMOS Technology," *Saud Almusallam. IntJournal of Engineering Research and Applicationwww.ijera.com*, vol. 9, pp. 31–37, 2019, doi: 10.9790/9622-0902013137.

[12] S. Shilpa and J. Srilatha, "Design and Analysis of High Gain Differential Amplifier Using Various Topologies," *International Research Journal of Engineering and Technology*, 2017, [Online]. Available: www.irjet.net

[13] P. A. G. Sankar and K. U. kumar, "Design and analysis of two stage operational amplifier based on emerging sub-32nm technology," in *International Conference on Advanced Nanomaterials & Emerging Engineering Technologies*, 2013, pp. 587–591. doi: 10.1109/ICANMEET.2013.6609382.

[14] M. Wolf, "Chapter 4 - Amplifiers," in *Embedded System Interfacing*, M. Wolf, Ed. Morgan Kaufmann, 2019, pp. 65–91. doi: https://doi.org/10.1016/B978-0-12-817402-9.00004-2.

[15] R. C. Jaeger • and T. N. Blalock, "FIFTH EDITION MICROELECTRONIC."

[16] T. Hossain, M. S. Rahman, M. M. Rahman, and A. R. A. Dibbo, "Performance Analysis of Graphene Nanoribbon Field Effect Transistor (GNRFET) based 6T and 7T SRAMs," in *2020 23rd International Conference on Computer and Information Technology (ICCIT)*, 2020, pp. 1–5. doi: 10.1109/ICCIT51783.2020.9392713.

[17] F. Rabieefar and D. Dideban, "Utilizing graphene nano-ribbon transistor in data converters: a comparative study," *ECS Journal of Solid State Science and Technology*, vol. 8, no. 3, p. M30, 2019.

[18] M. U. Mohammed, A. Nizam, L. Ali, and M. H. Chowdhury, "A Low Leakage SRAM Bitcell Design Based on MOS-Type Graphene Nano-Ribbon FET," in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2019, pp. 1–4. doi: 10.1109/ISCAS.2019.8702461.

[19] M. O. Faruque, T. Hasan, and S. al Imam, “Performance comparison between Graphene Nano-Ribbon FET & conventional CMOS based on Arithmetic Logic Unit (ALU),” in *2019 1st International Conference on Advances in Science, Engineering and Robotics Technology (ICASERT)*, 2019, pp. 1–3. doi: 10.1109/ICASERT.2019.8934488.

[20] A. Yadav, M. Patnala, and M. Rizkalla, “High Performance Gnrfet Based Serializer,” in *2019 IEEE National Aerospace and Electronics Conference (NAECON)*, 2019, pp. 458–464. doi: 10.1109/NAECON46414.2019.9057943.

[21] M. Mishra, R. Singh, and A. Imran, “Performance optimization of GNRFET Inverter at 32nm technology node,” *Materials Today: Proceedings*, vol. 4, pp. 10607–10611, Jan. 2017, doi: 10.1016/j.matpr.2017.06.428.

[22] A. Imran, R. S. Singh, and M. Mishra, “Simulation study of logic circuits using optimized graphene nanoribbon FETs,” in *2016 2nd International Conference on Next Generation Computing Technologies (NGCT)*, 2016, pp. 173–177. doi: 10.1109/NGCT.2016.7877410.

[23] G. Saha, A. K. Saha, and A. B. M. H. Rashid, “Low power dissipation logic inverter design using atomic-level width controlled GNR-FETs,” in *8th International Conference on Electrical and Computer Engineering*, 2014, pp. 160–163. doi: 10.1109/ICECE.2014.7026931.

[24] P. Sharma and G. Sapra, “Performance analysis of graphene based operational amplifier with conventional amplifier for future communications,” *Materials Today: Proceedings*, vol. 45, pp. 4084–4086, 2021, doi: https://doi.org/10.1016/j.matpr.2021.03.118.

[25] S. R. Madabhushanam, L. Malladi, and S. R. Gudepu, “Design High gain dual stage operational amplifier using CMOS 45nm Technology,” in *2020 Fourth International Conference on I-SMAC (IoT in Social, Mobile, Analytics and Cloud) (I-SMAC)*, 2020, pp. 1184–1188. doi: 10.1109/I-SMAC49090.2020.9243590.

[26] S. Waykole and V. S. Bendre, “Performance Analysis of Classical Two Stage Opamp Using CMOS and CNFET at 32nm Technology,” in *2018 Fourth International Conference on Computing Communication Control and Automation (ICCUBEA)*, 2018, pp. 1–6. doi: 10.1109/ICCUBEA.2018.8697461.

[27] A. Safrai, M. Dousti, and M. Tavakoli, “Monolayer Graphene Field Effect Transistor Based Operational Amplifier,” *Journal of Circuits, Systems and Computers*, vol. 28, May 2018, doi: 10.1142/S021812661950052X.

[28] P. Jain and A. M. Joshi, “Low leakage and high CMRR CMOS differential amplifier for biomedical application,” *Analog Integrated Circuits and Signal Processing*, vol. 93, no. 1, pp. 71–85, 2017, doi: 10.1007/s10470-017-1027-y.

[29] A. Vikhe and S. Turkane, “Comparative performance analysis of single stage differential amplifier at 32 nanometer regime,” in *2015 International Conference on Energy Systems and Applications*, 2015, pp. 406–410. doi: 10.1109/ICESA.2015.7503380.

[30] R. Tiwari, G. Mishra, and M. Misra, “A New High Performance CMOS Differential Amplifier,” Jan. 2009.