Implementation of Optimized Low Pass Filter for ECG filtering using Verilog

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Abstract. Electrocardiogram is a standard method used for the diagnosis of heart related disease. QRS complex plays an important role in Electrocardiogram signal processing since it is the prominent feature of Electrocardiogram signal. One of the important modules in the QRS detection algorithm is filtering. Electrocardiogram signal is processed to filter out unwanted signal through digital filtering. The main objective of this paper is to compare the resource utilization of hardware realization consumed between Direct Form I structure and Direct Form II structure. In this work, Infinite Impulse Response low pass filter to remove high frequency noise is designed with a passband frequency and stopband frequency of 5 and 25 Hz respectively. The designed filter is verified using Matlab Filter Design Analysis tool and realized in hardware using Verilog. Both the results show that the unwanted signals in the raw ECG signal are attenuated through the designed filter. The resource utilization result shows improvement with optimized Direct Form II implementation. The amount of look up tables, flip flop and digital signal processing used with Direct Form II structure shows a reduction to 0.26%, 0.12% and 2.50% respectively compared to 1.17%, 0.20%, 2.92% of utilization with Direct Form I structure.

***Keywords*:** Electrocardiogram, Digital filter, Infinite Impulse Response filter.

1. Introduction

Electrocardiogram (ECG) signals can be decomposed into three components: QRS complex, P and T waves, and muscle noise. High frequency noise is one of the types of disruption in ECG signal. Common high frequency noise is Electromyogram (EMG) noise which comes from muscular electrical activity or muscle noise which causes difficulties in data processing and analysis. P and T waves normally lies below 5 Hz while EMG noise are masking the QRS complex.

On the other hand, frequency of an ECG signal is ranging between 0.05-100 Hz [1]. This result is found in similar agreement as reported by Gaikwad and Chavan [2] where the frequency of ECG signal is ranging at 0.05-120 Hz. On top of that, 90% of the ECG signal spectrum energy is reported to be concentrated in the range 0.25-35 Hz [3]. In fact, it corresponds with earlier findings reported by Kohler et al. [4] where the QRS complex typically lies in the range of 10 Hz to 25 Hz. Besides, most of the QRS complex energy is located in the 5-15 Hz range [5]. In most records in the MIT-BIH Arrhythmia database, there are two ECG traces of the two main derivations (leads), where the upper signal is modified limb lead II (MLII) and modified lead V1 (V1). Normal QRS complexes are often

prominent in the upper signal. Hence, in this study, an MLII ECG record is selected as the input .mat file contains the matrix of raw signal values.

Appropriate sampling frequency for filter design is needed to ensure the sampling is sufficient to sample the ECG data without eliminating the frequency of the QRS complex. The sampling frequency should be at least 50 Hz as minimum sampling frequency depends on the maximum frequency of the measured data. To sample ECG data, 50 Hz is sufficient as sampling frequency [6]. Based on Nyquist theorem, the sampling frequency for a periodic signal to be digitized must be sampled at least twice the highest frequency component of the signal. In [7], the researchers discussed the appropriate sampling frequency content to preserve the desired frequency for ECG diagnosis and arrhythmia detection.

Filter is an electronic circuit which performs signal processing functions, specifically intended to remove unwanted signal components, and enhance wanted ones. Filter is classified into two types which are analog filter and digital filter. The flexibility and reconfigurability of digital filter are the reasons digital filter are preferred over analog filter. Digital filter is further classified into Finite Impulse Response (FIR) and Infinite Impulse Response (IIR). IIR filter consume less parameters and memory compared to FIR filter [2]. To design a filter commonly begin with the number of orders of the filter. This number of orders is directly proportional to the stopband attenuation of the filter. The filter attenuates the unwanted signals better with the increment on the number of orders. However, it has drawbacks on the hardware complexity [8] and hardware cost overhead since increased number of order means increased number of resources and this will lead to area increment. Hence, the filter design with a minimum number of orders is sufficient to fulfil the specifications to preserve the resources needed.

Optimum output is executed with Butterworth filter compared to Chebyshev type I and Chebyshev type II as a trade-off to hardware resources. Previous research [9] attempted to overcome trade-off between speed and area. Fully parallel architecture offers exponentially increment in speed. However, it increases the area requirement simultaneously. They counter the drawback with Direct Form I and Direct Form II structure implementation. The filter specifications which are the cut off frequency and sampling frequency are determined based on the ECG application with 100 Hz and 1 kHz respectively. With Butterworth filter order five, their filter design has three sections that are cascaded which consists of ten adders, ten delay elements and 13 multiplier units for their Direct Form I structure. Their research shows that Direct Form II structure consume less area, number of nets and number of connections. In fact, Direct Form II structure shows 20% faster than Direct Form I structure where the amount of delay resources used is reduced by sharing delay between feed-forward coefficient and feedback coefficient. However, the cut-off frequency of the filter proposed is not within the range of raw ECG signal for MIT-BIH Arrhythmia database used in this paper.

On the other hand, Lai et al. [10] have presented a pipelined digital filter module. An IIR filter is designed intended for filtering the low frequency components. However, the filter is designed with Direct Form I structure which known to double up the amount of required delay elements.

In this paper, IIR filter for ECG filtering is designed with Direct Form I and Direct Form II structure. These two structures will be compared in terms of the resource utilization for the hardware implementation using Verilog. The filter specifications-passband frequency and stopband frequency are 5 Hz and 25 Hz respectively. Section 2 of this paper presents the design of IIR filter implementation in Matlab and Verilog. Meanwhile section 3 demonstrates the simulation results. Finally, the analysis of the obtained result is summarized in section 4.

2. Design of Filter

Figure 1 shows the block diagram of IIR filter. A recursive filter like IIR filter has feedback. The recursive part depends on the previous value of the input, x[n] and previous values of y[n] where y [n]

is the filter output at a discrete time instance. These values will be multiplied by coefficients and added together afterwards and produced output which is the filtered signal.

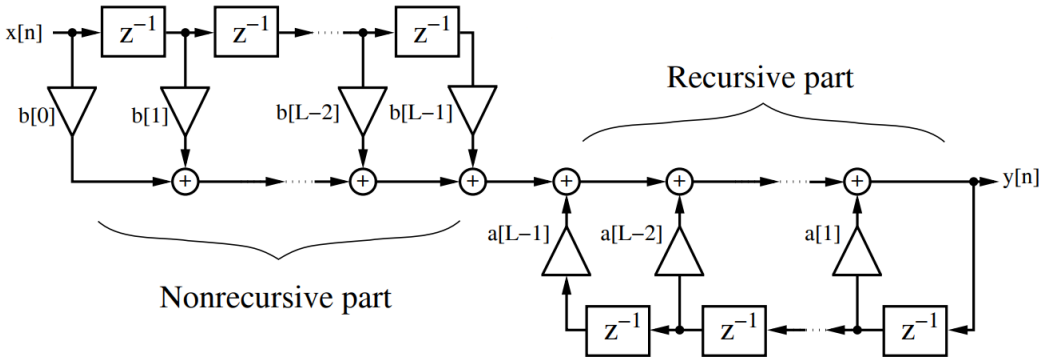


Figure 1. Block diagram of IIR filter [11]

The obtained coefficient of the designed filter is modelled in Matlab to verify its functionality before proceeding to hardware implementation in Verilog. However, converting Register Transfer Level (RTL) from any Matlab code will not give correct functionality at hardware level since Hardware Description Language (HDL) code generation has limitations on the supported number of blocks. In fact, most Digital Signal Processing algorithms are executed sequentially, hence, simply extracting the algorithm into hardware design will result in poor output. This sequential processing reduces the area and power utilization. In fact, the elements in filter design are multipliers, adder, and registers (delay elements). These elements will increase the area consumed. To accelerate the hardware performance, optimization is needed. The purpose of optimization is to achieve the best design that seeks to maximize or minimize one or more performance indices.

2.1. Filter implementation in Matlab

To remove the high frequency noise within the ECG signal, Butterworth IIR low pass filter is designed using Filter Design and Analysis (FDA) tool in Matlab which offers accuracy and time wise in designing digital filter blocks [12]. Matlab simulation was performed to verify the magnitude response and performance of the designed filter.

Figure 2 shows the flowchart of designing filter using Matlab. Initial step to design a filter is defining the filter specifications. Filter specifications which are passband frequency, stopband frequency and sampling frequency are set according to the design requirements. The minimum order as well as the filter coefficients are then obtained and finally the filter is verified with ECG signal as input. Once verified, it proceeds to be implemented in hardware using Verilog.

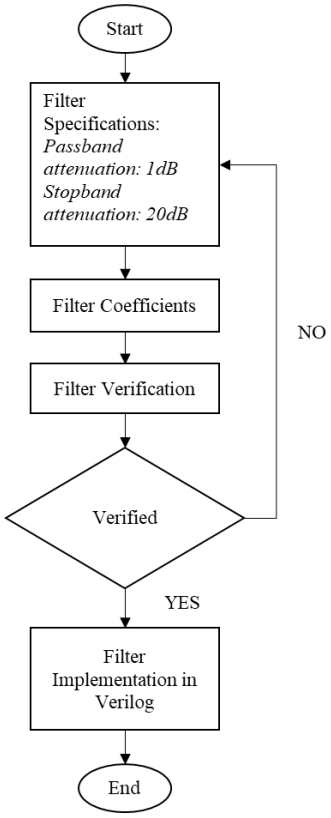


Figure 2. Flowchart of filter design in Matlab

The passband frequency and stopband frequency are 5 Hz and 25 Hz respectively since the QRS complex typically lies in that frequency range. Sampling frequency is set according to the input sample which is 360 Hz as it is the sampling frequency for the ECG signal acquired from MIT-BIH Arrhythmia database [13]. In fact, it complies with the Nyquist theorem mentioned earlier where the sampling frequency must be at least twice of the highest frequency component of the signal that needs to be sampled. With the specifications defined, the number of orders two is selected by the tools. Figure 3 shows the magnitude response of the designed filter.

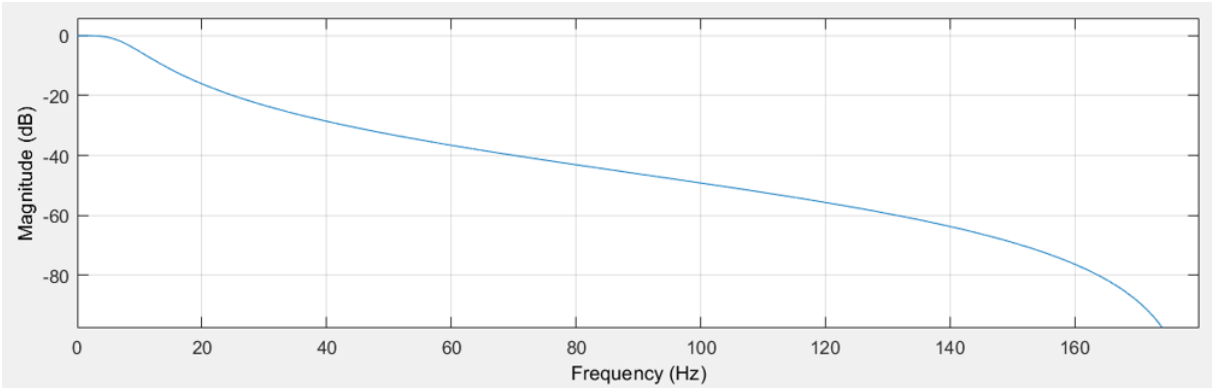


Figure 3. Magnitude response of the design filter

The transfer function of the designed filter has numerator polynomial coefficients of 1, 2 and 1 while the denominator polynomial coefficients are 1, -1.802 and 0.820. Equation (1) shows the difference equation of the second order IIR low pass filter.

$$y(n) = 1.802y(n-1) - 0.820y(n-2) + x(n) + 2x(n-1) + x(n-2) \quad (1)$$

where:

x(n): input signal (raw ECG signal)
y(n): filtered output

The raw ECG signal from the MIT-BIH Arrhythmia database is used as the input samples, x(n) to verify the filter's functionality. MLII ECG record for data 100 with 10 s duration time is selected as the input. Once verified, the filter is proceeded to be implemented in hardware using Verilog.

2.2. Filter implementation in Verilog

The hardware module is then designed using Verilog and has the performance of the designed filter analysed. Both the input and coefficient values are signed values; hence the most significant bit (MSB) is used as the sign bit and the remaining bits are the value that must fit into. For this IIR filter, the input sample and coefficient registers are set to be 32 bits wide and the output sample to be 64 bits wide. The obtained filter coefficients from Matlab are floating points numbers. To address the coefficient values in Verilog, the decimal point is converted to fixed point values. The purpose of fixed-point representation is to quantify and minimise the word length effects.

Equation (2) shows the calculation to convert the floating point to fixed point. Since both the input and coefficient values are signed values, the two's complement of x is calculated if the coefficient is negative.

$$fixed\ point, x = round\ off\ (floating\ point\ X\ 2^{fractional\ bits}) \quad (2)$$

Figure 4 shows the Direct Form I structure of IIR filter. It consists of four adders, five multipliers and four delay elements. The feed-forward coefficients (b) and feedback coefficients (a) are multiplied with the separate delay elements. This will increase the number of resources, especially flip flop when realized using Verilog.

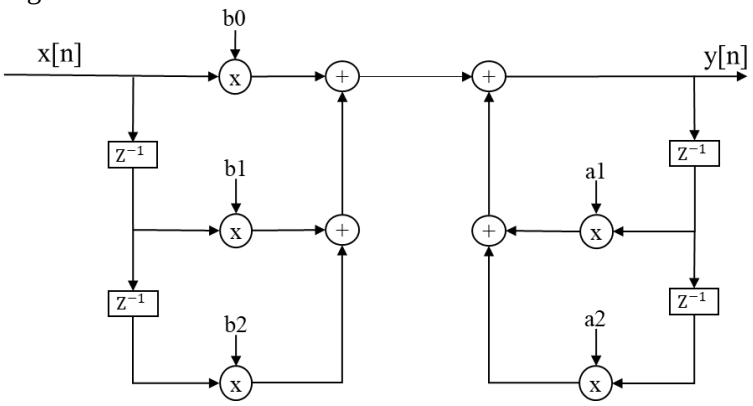


Figure 4. Direct Form I structure

Figure 5 shows the block diagram Direct Form 1 structure of IIR filter. D-type flip flop module is used for one clock delay module. This structure needs five flip flops to realize the digital filter in Direct Form I structure. Input, x will be stored in D flip flop labelled as z1_b and concurrently multiplied with coefficient b0. The output of z1_b becomes the delay by one and is then multiplied with coefficient b1. Next, the output of z2_b which holds the output value of z1_b becomes delayed by two and multiplied with coefficient b2. These values are then sum together. The feedback value with delay one and two are multiplied with coefficient a1 and a2 respectively. These values are then added up with the previous summation value before storing the value in flip flop and produced output, y.

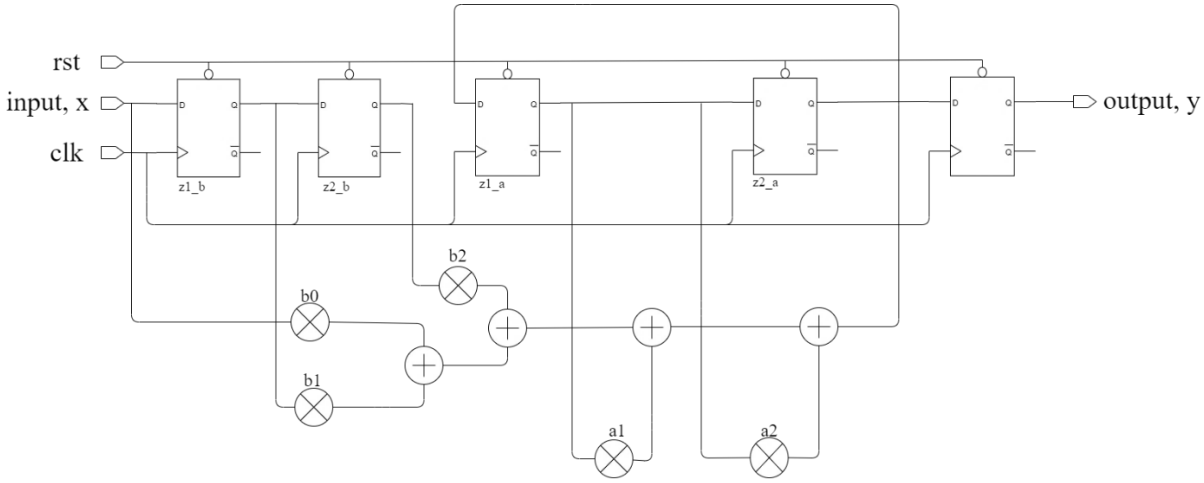


Figure 5. Block diagram with Direct Form I structure

To optimize the hardware resources, the filter is designed with Direct Form II structure. Digital filter with Direct Form II structure is shown in Figure 6. It consists of four adders, five multipliers and two delay elements.

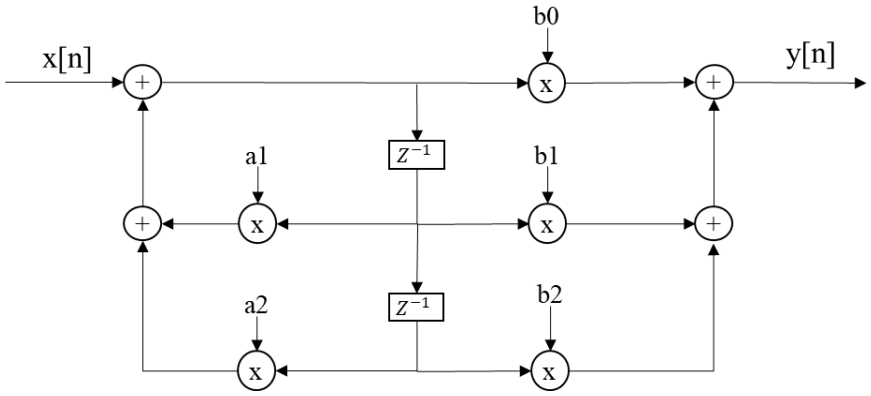


Figure 6. Direct Form II structure

The block diagram of a digital filter with Direct Form II structure is shown in Figure 7. The delay elements are shared between the feed-forward coefficient and feedback coefficient. Hence, they only need three flip flops to perform the operation. The amount of flip flop needed is reduced from five flip flops in Direct Form I structure to three flip flops in Direct Form II structure.

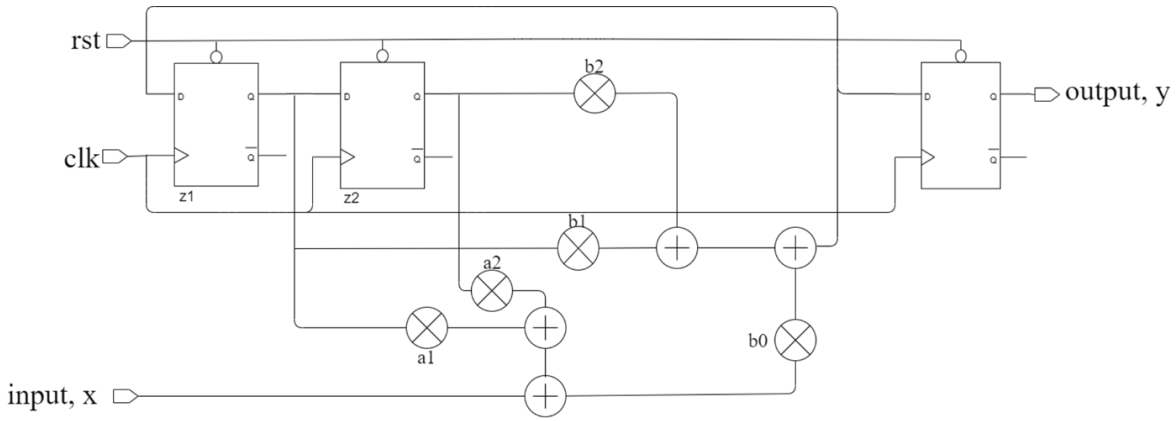


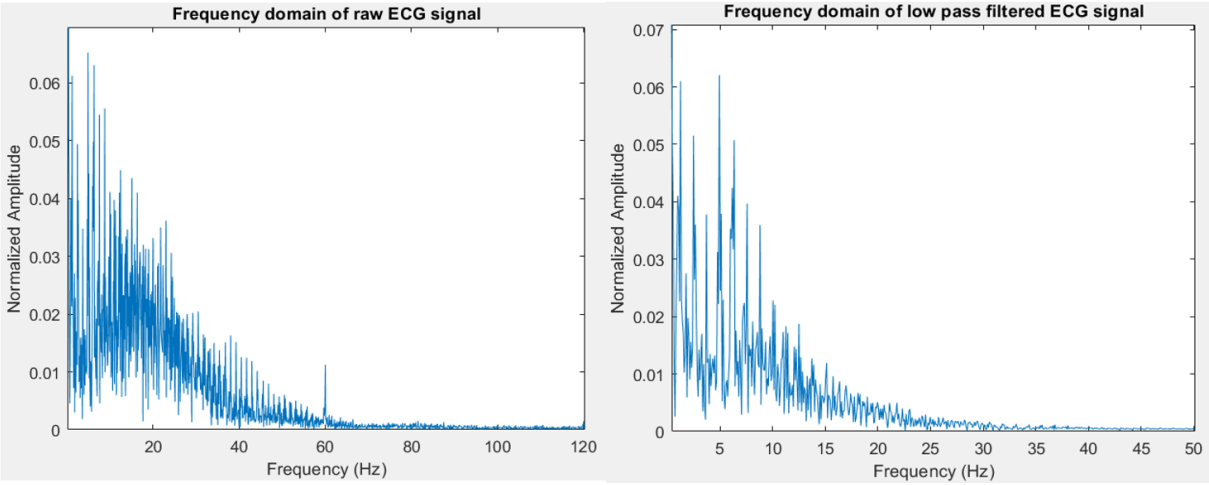
Figure 7. Block diagram with Direct Form II structure

3. Experimental Results

3.1. Filter implementation in Matlab

Figure 8 shows the comparison of frequency of raw ECG signal and the frequency of ECG signal after filtering. This result in Figure 8 (a) is found in similar agreement as reported by Gaikwad and Chavan [2] where the frequency of ECG signal is ranging at 0.05-120 Hz. It also reflected the resemblance made by Wu et al. [3] where 90% of the ECG signal spectrum energy is concentrated in range 0.25-35 Hz. The sampling frequency set earlier which is 360 Hz complied with the highest frequency of this raw ECG signal which is 120 Hz. The sampling frequency is more than twice of Nyquist theorem requirement. The low pass filter is designed to remove the high frequency signal and enhance the low frequency signal.

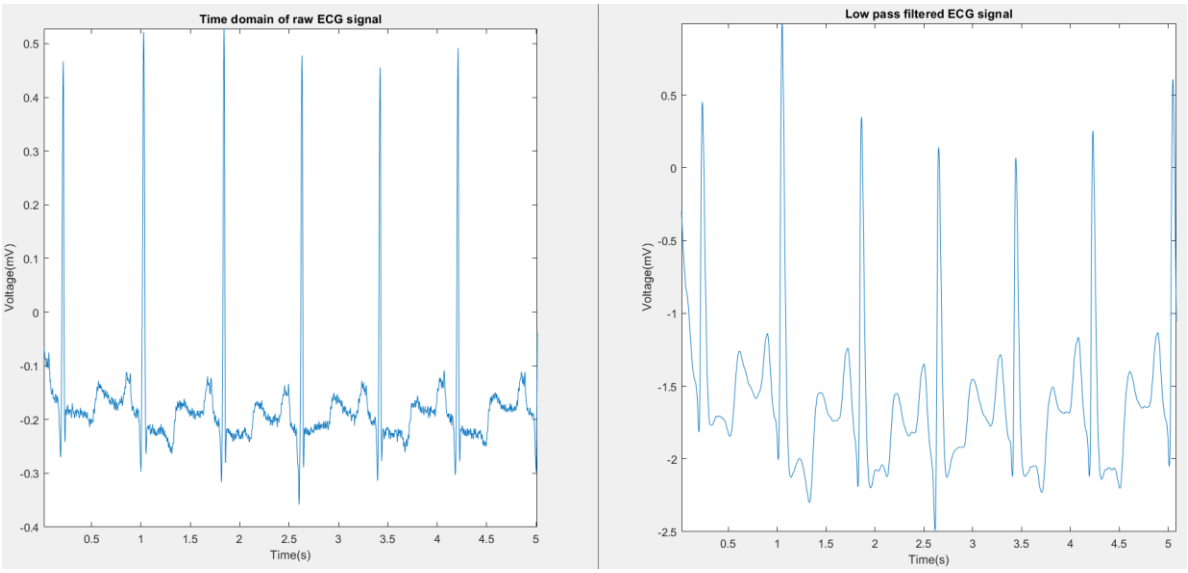
The frequency of the QRS complex typically lies in the range of 10 Hz to 25 Hz [4]. On the other hand, most of the QRS complex energy is in the 5-15 Hz range [5]. Considering these statements, the designed filter is set to attenuate the signal with frequency greater than 25 Hz and enhance the signal with frequency within 5-25 Hz as shown in Figure 8 (b). This is to ensure that the unwanted signal frequency is eliminated while enhancing the wanted ones.



(a) (b)

Figure 8. Comparison of frequency domain of (a) raw ECG signal and (b) low pass filtered ECG signal

Figure 9 (a) and (b) show the time domain of the ECG signal of pre and post filtering respectively. The obtained results show that the filter successfully eliminates the unwanted signal that exist within the input signal and the filtered signal is smoothen and high frequency-noise free. The data with high frequency is eliminated after the filtering.

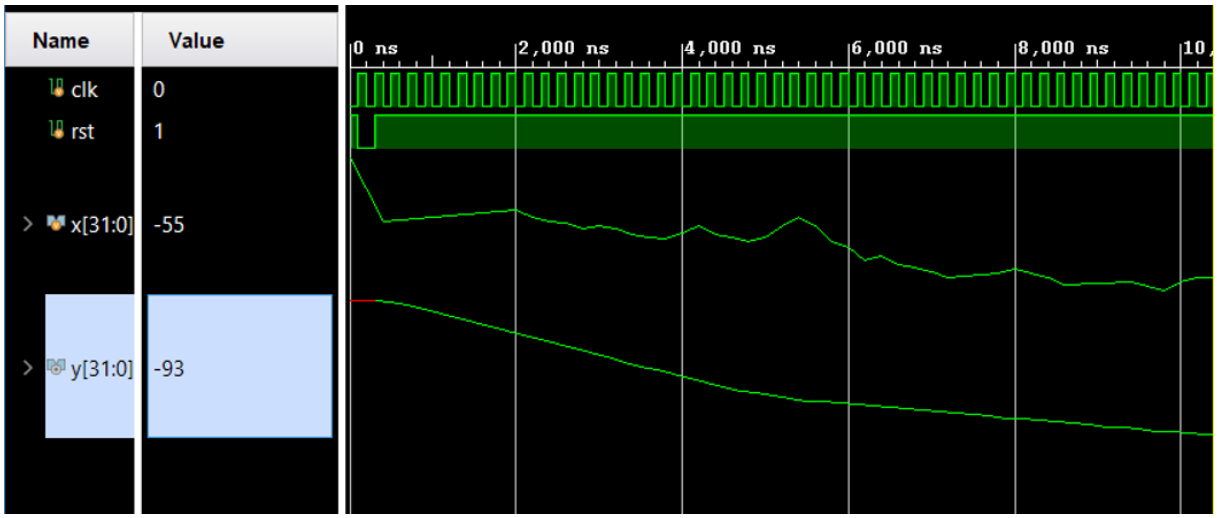


(a) (b)

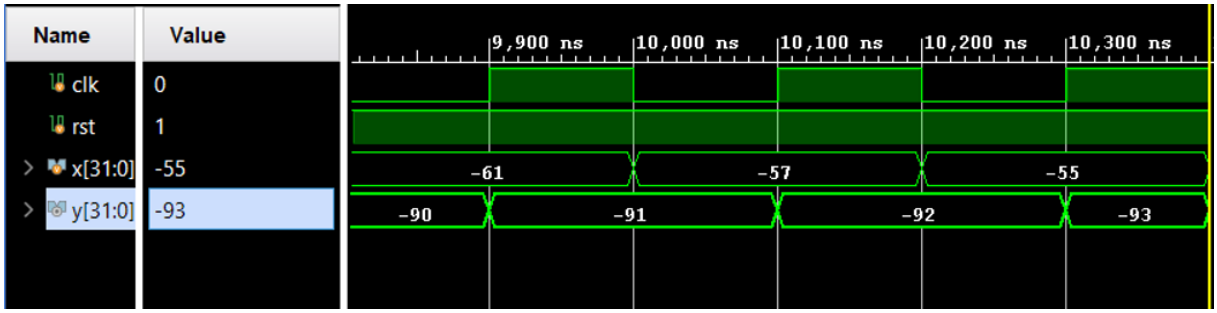
Figure 9. Comparison of time domain of (a) raw ECG signal (b) low pass filtered ECG signal

3.2. Filter implementation in Verilog

The length of the raw ECG signal is 3600. However, only 50 samples are extracted to be as the input, x in the testbench for verification. Raw ECG signal is used as the input, x. and output, y is the result of the filtered signal after implementation of the designed low pass filter which consists of only expected frequency. The result of the filtered ECG signal is shown in Figure 10. Functional simulation is used to verify the logical correctness of the filter design. From the result shown in Figure 10 (a), the filtered signal, y is smoothened where it consists of only signal with expected frequency that has been filtered by the designed filter. Figure 10 (b) is the reflected digital version of the analog waveform in Figure 10 (a). At every positive edge clock cycle, a new output is produced. No output is produced till the next positive edge clock cycle.



(a)



(b)

Figure 10. Result of filtered ECG signal (a) in analog waveform (b) in digital waveform

With Direct Form I structure, the number of flip flops to perform the filtering operation is five flip flops. To filter data like an ECG signal which has lots of data points will consume the resources. To minimize the resource utilization used, the digital filter is then optimized by applying Direct II form structure. Table 1 shows the resource utilization of the digital circuit of IIR low pass filter with Direct Form I and Direct Form II structure.

Table 1. Resource Utilization of Direct Form I and Direct Form II structure

Resource Utilization	Max	Design			
		Direct Form I		Direct Form II	
		Used	Utilization %	Used	Utilization %
Look Up Tables	41000	478	1.17	108	0.26
Flip Flop	82000	160	0.20	96	0.12
Digital Signal Processing	240	7	2.92	6	2.50

Utilization percentage is obtained from the used resources out of the maximum resources available in the board. Implementation of different structure reflected the resource utilization has shown that the amount of Look Up Tables, Flip Flop and Digital Signal Processing used shows a reduction to 0.26%, 0.12% and 2.50% respectively compared to 1.17%, 0.20%, 2.92% of utilization previously.

4. Conclusion

IIR low pass filter is designed to filter the raw ECG signal from MIT-BIH Arrhythmia Database. Matlab is used as the verification for the designed filter while Verilog is used for the hardware implementation of the digital filter. From the result, it shows that the unwanted signal in the raw ECG signal is attenuated through the designed filter. By sharing the delay elements between input coefficients and feedback coefficients through optimization with Direct Form II structure, the resource utilization is improved. It is possible to enhance and analyse the performance of the designed filter by implementing it in Application Specific Integrated Circuit (ASIC). In future work, the designed filter will be instantiated as filtering module of the QRS detectors of ECG signal. Besides, the number of gate count possibly to be reduced through the multiplier optimization since multiplier is also one of the main area consuming blocks in filtering module apart from delay element.

5. References

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