A Pspice-based Design of DC-DC Converter Systems

Nik Din Muhamad, Abdul Halim Mohd Yatim, *Senior Member, IEEE*, and Abd Jaafar Shafie

***Abstract*—A new approach to using Pspice in designing dc-dc converter systems is introduced in this paper. In this new approach, the power stage and control loop design equations are programmed in Pspice. For this purpose, an option available in Pspice called Analog Behavioral Modeling (ABM) is used. By doing so, the parameter of power stage and the component values of the error amplifier can be easily obtained by means of Pspice DC analysis. The methodology of development is presented in some detail. A design example is included to demonstrate the effectiveness of the proposed approach in designing dc-dc converter systems.**

***Index Terms*—Computer-aided design, Pspice, Control loop design, DC-DC Converter, Small-signal model.**

I. Introduction

In designing dc-dc converter systems, there are two requirements to be satisfied: steady-state and dynamic. The steady-state requirements can be satisfied by properly choosing the parameters of the power stage. The dynamic requirements can be met by using an appropriate controller. There are a number of well-documented techniques and guidelines available for designing dc-dc converter systems [1-5]. Today, most dc-dc converter system design is carried out with the aid of a computer-aided circuit analysis program such as Pspice. However, the use of Pspice is limited to validation of circuit designs. A dc-dc converter design usually needs some theoretical analysis and calculation. This makes another calculation software, such as Mathcad, used along with Pspice in the process of design. The use of another software besides Pspice causes the process of design to be somewhat inconvenient and inefficient.

In this paper we demonstrate that Pspice alone can be used to design dc-dc converter systems. The design equations can be programmed in compact form in Pspice. For this purpose, an option available in Pspice called Analog Behavioral Modeling (ABM) is used. Both steady-state and dynamic design equations are programmed. A set of design equations can be made as a subcircuit model and stored in Pspice's library. In this manner, the design equations can be treated as a library component, making it easy to use. The presence of design equations programmed in Pspice make a new approach to using Pspice simulator in process of design. This approach includes both design as well as simulation tools thus making extensive use of Pspice in dc-dc converter design cycle. Moreover, both the flexibility and capability of Pspice as a stand-alone program can be enhanced. This approach will facilitate the design of dc-dc converter systems in Pspice and it will make the design more convenient and efficient.

Throughout this paper, a buck converter with voltage mode control is used as an example to develop and to verify the design procedure. The general procedure, however, can still be readily extended to include other converters with different control schemes provided that their transfer functions and design equations are available.

This paper is actually an extension to our previous paper [6]. The power stage design equations, which were excluded in the previous paper, are included in this paper.

II. Design Process

The buck converter with voltage mode control is shown in Fig. 1. This converter is used to illustrate the design process and demonstrate its feasibility for power supply design. The converter system comprises the power stage, the compensator and the PWM modulator. The converter is operating in continuous conduction mode.

A. Power Stage, PWM modulator and Controller

Using the averaging and linearization techniques, the control-to-output transfer function of the buck converter including PWM modulator, can be obtained as

$$\frac{\hat{v}_o}{\hat{v}_c} = g_{co}\frac{\left(1+\frac{s}{\omega_{zESR}}\right)}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}} \tag{1}$$

where

$$g_{co}=\frac{V_g}{V_p},\ \omega_o=\frac{1}{\sqrt{LC}},\ \omega_{zESR}=\frac{1}{R_{esr}C},\ \text{and}\ Q=\frac{R}{\omega_o L}.$$

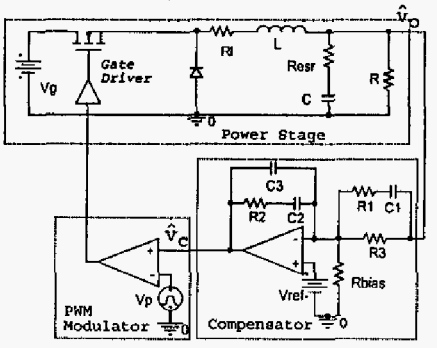

Fig. 1. Buck converter with voltage mode control. The compensator used is type-3 error amplifier.

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Nik Din Muhamad, Abdul Halim Mohd Yatim and Abd Jaafar Shafie are with the Department of Energy Conversion, Faculty of Electrical Engineering, Universiti Teknologi Malaysia, 81310 UTM Skudai, Johor.

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For the circuit in Fig. 1 the power stage has the following parameters: V_g = 12 V, V_o = 5V, R = 1.25 Ω, R_l = 50 mΩ. The power stage design parameters are inductance L_f, capacitance, C_f and ESR of capacitor, R_{ESR}. The peak value of sawtooth voltage, V_p, for the PWM modulator is assumed to be 3 V. The compensator network consists of R1, R2, R3, R_{bias}, C1, C2, C3 and V_{ref}. We assume that the value of V_{ref} is 2. 5V, R_{bias} is 10 kΩ and the rest are design parameters.

B. Power Stage Design Equations

The values of L_f , C_f, and R_{ESR} determine CCM of operation and a prespecified peak-to-peak output voltage ripple. For a given switching frequency, power stage components L_f, C_f, and R_{ESR} may be selected to meet the following criteria:

1) The value of inductance is chosen to assure CCM. To maintain CCM down to one-fifth output current I_o, the minimum value for L_f is

$$L_{min} = \frac{2.5(V_g - V_o)D}{f_s \frac{V_o}{R}} \tag{2}$$

where V_o, f_s, R, and D are the output voltage, switching frequency, load resistance and steady state duty ratio respectively.

2) Capacitance C_f is determined from maximum allowable peak-to-peak output ripple voltage V_{pp} = Δv_c considerations:

$$\Delta v_c \le \Delta v_{c,c} + \Delta v_{c,ESR}$$

where $\Delta v_{c,c}$ is the AC component of the voltage across the ESR and $\Delta v_{c,ESR}$ is the AC component voltage across the filter capacitance. However, it is known that the peak-to-peak ripple voltage is independent of the voltage across the filter capacitor and is determined only by the ripple voltage of the ESR if [7]

$$C_f \ge C_{min} = \max\left(\frac{1-D_{min}}{2r_c f_s}, \frac{D_{max}}{2r_c f_s}\right) \tag{3}$$

3) The peak-to-peak voltage ripple, Δv_c, is usually given as a percentage of the output voltage, typically equal or less than 1%. If the condition described by (3) is satisfied, the ESR of capacitor for the prespecified peak-to-peak voltage ripple is

$$R_{ESR} \le \frac{\Delta v_c f_s L}{V_o(1-D_{min})} \tag{4}$$

C. Compensator Design Equations

The loop shaping approach is simple and effective for dealing with the plants having complex dynamic behavior. Among popular loop shaping method in power electronic applications is K-factor approach, introduced in [4]. The main features of K-factor approach are that the pole-zero placement and resultant circuit component values can be obtained without trial-and-error. This is one of the reasons why the K-factor approach is widely accepted by many researchers [9-12]. Since the analysis of the control loop design equations using K-factor approach in Pspice has been published earlier [6] we repeat here, for the sake of brevity, only the essential.

The type-3 error amplifier is commonly used for compensation of buck, boost and buck-boost circuits due to its ability to provide the phase boost, $\emptyset_{boost}$:

$$0 \le \phi_{boost} \le 180° \tag{5}$$

The transfer function of the type-3 error amplifier is given by

$$G_c(s) = \frac{\frac{\omega_{co}}{A_{co}K}\left(\frac{\sqrt{K}}{\omega_{co}}s+1\right)^2}{s\left(\frac{s}{\sqrt{K}\omega_{co}}+1\right)^2} \tag{6}$$

where ω_{co} is the desired crossover frequency, K is the pole frequency and zero frequency control factor. The value of K can be adjusted depending on the phase boost ($\emptyset_{boost}$) required to make the phase compensation. To use the K-factor approach, the crossover frequency, f_{co}, must be chosen, and then the gain, A_{co} and the phase, $\emptyset_{co}$, of power stage at f_{co} must be found. In short, the computation procedures of K-factor approach are as follows:

1. Calculate the gain, A_{co} and the phase, $\emptyset_{co}$, of power stage at f_{co}:

$$A_{co} = \left|\frac{v_o}{v_c}\right| = \frac{G_{co}\sqrt{1+\left(\frac{\omega_{co}}{\omega_{zesr}}\right)^2}}{\sqrt{\left(1-\left(\frac{\omega_{co}}{\omega_o}\right)^2\right)+\left(\frac{\omega_{co}}{Q\omega_o}\right)^2}} \tag{7}$$

$$\phi_{co} = \tan^{-1}\frac{\omega_{co}}{\omega_{zesr}} - \tan^{-1}\frac{\frac{\omega_{co}}{Q\omega_o}}{1-\left(\frac{\omega_{co}}{\omega_o}\right)^2} \tag{8}$$

2. By knowing A_{co}, and $\emptyset_{co}$, and specifying the phase margin, PM, the phase boost required can be calculated as

$$\phi_{boost} = PM - 90° - \phi_{co} \tag{9}$$

3. Then, K-factor is calculated as

$$K = \tan^2\left(\frac{\phi_{boost}}{4} + 45^\circ\right) \quad (10)$$

4. The two poles of the compensator are located at

$$\omega_{p12} = \frac{\omega_{co}}{\sqrt{K}} \quad (11)$$

5. The two zeros of the compensator are located at

$$\omega_{z12} = \sqrt{K}\omega_{co} \quad (12)$$

6. The integrator gain of the compensator is

$$\omega_i = \frac{\omega_{co}}{A_{co}K} \quad (13)$$

It is important to point out that this design procedure is general in the sense that it can be used to any suitable application. For specific application, this design procedure must be suited to the requirements of those applications. In the case of buck converter, an important constraint is that the crossover frequency must be less than one-fourth of the switching frequency. This constraint is required to avoid the large signal instability [1]. The design of compensator follows the design of power stage because power stage parameters, such as filter inductance, capacitance, and ESR of capacitance, are needed. The next step is to convert the obtained values of poles and zeros to the component values of compensator. This is a straightforward process. Basically, the conversions occur as follows:

$$C_3 = \frac{f_{z12}}{(\omega_i R_3 f_{p12})} \quad (14)$$

$$C_2 = C_3\left(\frac{f_{p12}}{f_{z12}} - 1\right) \quad (15)$$

$$R_2 = \frac{1}{2\pi f_{z12} C_2} \quad (16)$$

$$R_1 = \frac{R_3}{\left(\frac{f_{p12}}{f_{z12}} - 1\right)} \quad (17)$$

$$C_1 = \frac{1}{2\pi f_{p12} R_1} \quad (18)$$

$$R_{bias} = \frac{V_{ref}}{V_o - V_{ref}} R_3 \quad (19)$$

III. PSPICE IMPLEMENTATION

The Pspice simulator is provided with an extension called Analog Behavioral Modeling (ABM). With ABM the simulator can be used like a programming language and to solve general mathematical problems by translating them to an electrical circuit. ABM in Pspice is able to evaluate expressions that are functions of circuit variables (voltages, currents, and simulation time) using the controlled current and voltage sources (G and E devices). ABM can also be used to solve system of linear and nonlinear algebraic equations as well as systems of complex, transcendent and ordinary, differential equations in their implicit or explicit form. In each case, the equations are converted into electrical circuits and solved by Pspice with a DC analysis for only algebraic equations or a transient analysis for systems of algebraic and differential equations. Editing the input file of Pspice is relatively more comfortable than programming in MATLAB, C or other program languages.

To implement the equations in Pspice, all variables are coded into voltages. The relevant equations are represented by dependent sources that are function of the coded variables and constants. There are two parts of design equations to be programmed in Pspice: power stage and control loop. The power stage design equations to be programmed are equations (2)-(4), while the control loop design equations are equations (7)-(19). All the equations are implemented in Pspice by using the .PARAM statement. By using the .PARAM statement we can create parameters and assign algebraic mathematical expressions to it. To enable the related parameters available in schematic, ABM parts are used. The complete Pspice listing of design equations is given in Appendix.

V. DESIGN EXAMPLE

A design example is used to demonstrate the effectiveness of the proposed approach in designing dc-dc converters. The example is a buck converter operated in continuous conduction mode with the switching frequency, f_s =100kHz. The only known parameters are: input voltage V_g = 12V, output voltage, V_o = 5V, sawtooth peak voltage of PWM modulator, V_p = 3V, reference voltage, V_{ref} = 2.5V. The value of R_{bias} is chosen arbitrarily as 10 kΩ. For the control loop design, the crossover frequency, f_{co} is chosen as $f_s/6$ and the phase margin is chosen as 60°. This is a typical specification to design the compensator of a buck converter.

All the given parameters above serve as inputs to the programmed design equations. It outputs the following parameters: L_f, C_f, R_{ESR}, C1, C2, C3, R1, R2, and R3. Since Pspice simulator always performs bias point analysis before performing other analysis, these values can be passed to other circuit models in order to perform the other analysis such as transient and frequency response. By doing so, the design phase and the verification phase seem to be simultaneously performed by Pspice. Obviously, this is one of the advantages to program the design equations in Pspice.

In this design example, the design parameters were passed to the averaged circuit models to perform frequency response and transient analysis. The design parameters were also passed to the switching detailed model to perform transient analysis (cycle-by-cycle simulation). The result of design parameters obtained by bias point analysis of Pspice is shown in Fig. 2. It can be seen from the result that all the obtained parameters were given in volt due to all the variables were already coded into voltages.

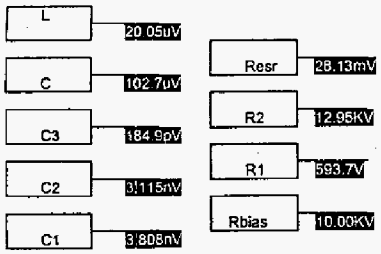

Fig.2. The result of bias point analysis of Pspice gives design parameters.

Using averaged circuit model, frequency response of loop-gain based on the averaged circuit model was simulated by Pspice AC analysis. The result is shown in Fig. 3. From the bode plot, we can see that the crossover phase is −119.6°, indicating stable operation with PM of 60.4°. The crossover frequency is at 16.623 kHz. The differences between the desired values (PM = 60.0° and f_{co} = 16.667kHz) and the results of Pspice are fairly small.

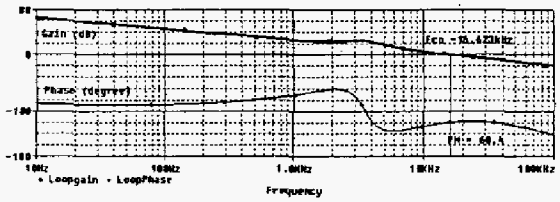

Fig. 3. Bode plot of loop-gain (gain in dB and phase in degree)

Transient analysis of the output voltage and the inductor current based on the averaged circuit and switching detailed models are shown in Fig. 4 and 5, respectively. Both the results of the averaged and switching detailed model (actual) are superimposed in the same graphs for comparison. It can be seen that, both the waveforms agree very well. To evaluate the performance of the system, load steps were performed. The load steps were programmed to step down at 9.0 ms (from 4A to 1A) and to step up at 9.5 ms (from 1A to 4A). It can be seen that the step responses of the inductor current and the output voltage reflect the behavior of a system with phase margin of about 60°, verifying our design.

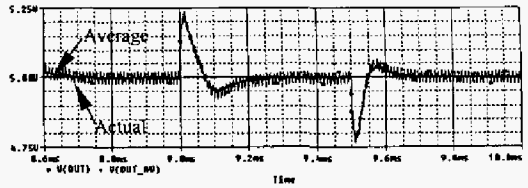

Fig. 4. Load step responses of the output voltage

In order to make the design equations easy to use, it was made as a subcircuit model and stored in Pspice's library. In this manner, the design equations are treated as a library component.

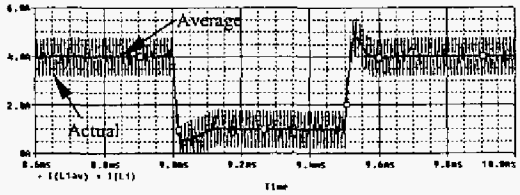

Fig. 5. Load step responses of the inductor current

V. Conclusion

A new approach to using Pspice in designing dc-dc converter system has been introduced. In this new approach, the power stage and control loop design equations are programmed in Pspice. The design parameters have been easily obtained by means of Pspice DC analysis. The extension of this approach to other converters and control schemes like peak current mode (PCM), Average current control (ACC) and power factor correction (PFC) is straightforward provided that there exist small-signal models and design procedures.

VI. Acknowledgment

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VII. APPENDIX

Pspice Listing for Power Stage and Control Loop Design Equations

Power Stage and Control Loop Design Equations

PARAMETERS:
pi = 3.14159265

PARAMETERS:
L = {1.1*Lmin}
Resr = {IF(0.9*Rc>40m,40m,0.9*Rc)}
C = {1.1*Cmin}
R3 = 10k
Vp = 3
Vref = 2.5V
f = {fco}
fs = 100k
fco = 16.666k

PARAMETERS:
wi = {w/(Aco*k)}
wp12 = {w*sqrt(k)}
wz12 = {w/sqrt(k)}

PARAMETERS:
w = {2*pi*f}
Mag_Buck_ZESR = {SQRT((1+(w*w)/(wzesr*wzesr)))}
wzesr = {1/(Resr*C)}
Ph_Buck_Zesr = {atan(w/wzesr)*180/pi}
wco = {2*pi*fco}

PARAMETERS:
Mag_Buck_LC = {(Vg/Vp)/SQRT(((w/(Q*wo))*(w/(Q*wo)))+(1-(w*w/(wo*wo)))*(1-(w*w/(wo*wo))))}
Ph_Buck_LC_raw = {-atan((w/(Q*wo))/(1-(w*w)/(wo*wo)))*180/pi}
Ph_Buck_LC = {IF((1-((w*w)/(wo*wo)))<0,Ph_Buck_LC_raw-180,Ph_Buck_LC_raw)}
Q = {R/(wo*L)}
wo = {1/SQRT(L*C)}

PARAMETERS:
PowerStage = {Mag_Buck_LC*Mag_Buck_Zesr}

PARAMETERS:
Ph_PowerStage = {Ph_Buck_Zesr+Ph_Buck_LC}

PARAMETERS:
Vg = 12
Vo = 5
R = 1.25

PARAMETERS:
Mag_Buck_LC_at_fco = {(Vg/Vp)/SQRT(((wco/(Q*wco))*(wco/(Q*wco)))+(1-(wco*wco/(wo*wo)))*(1-(wco*wco/(wo*wo))))}
Mag_Buck_Zesr_at_fco = {SQRT((1+(wco*wco)/(wzesr*wzesr)))}
Mag_Buck_fco = {Mag_Buck_LC_at_fco*Mag_Buck_Zesr_at_fco}

PARAMETERS:
PM = 60
Aco = {PowerStage}
Pco = {Ph_PowerStage}
k = {(Tan(((Pboost/4)+45)*pi/180))*(Tan(((Pboost/4)+45)*pi/180))}
Pboost = {PM-90-Pco}

PARAMETERS:
Lmin = {5*(Vg-Vo)*D/((PIL/10)*fs*Vo/R)}
D = {Vo/Vg}
PIL = 20

PARAMETERS:
Cmin = {max((1-D)/(2*Rc*fs),D/(2*Rc*fs))}
Rc = {fs*Lmin*Vr/(Vo*(1-D))}

PARAMETERS:
Vr = {PVC*Vo/100}
PVC = 1

PIL: Percentage of Inductor Current
PVC: Percentage of Capacitor Voltage

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