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A new pulse-width modulation (PWM) scheme for modular structured multilevel voltage source inverter

J. A. AZIZ†* and Z. SALAM†

This work proposes a new switching scheme for a particular multilevel topology, known as the modular structured multilevel inverter (MSMI). The proposed scheme is based on symmetric regular sampled unipolar PWM, with multiple modulating waveforms and a single carrier. Mathematical equations that define the PWM switching instants are derived. These equations are suitable for digital implementation. An experimental five-level MSMI test-rig is built to implement the proposed algorithm. The derived equations are implemented by a low-cost fixed-point microcontroller. Several tests to quantify the performance of the inverter under the proposed modulation scheme are carried out.

1. Introduction

Multilevel voltage source inverter (MVSI) offers several advantages that make it preferable over the conventional voltage source inverter (VSI). These include the capability to handle higher dc link voltage, improved harmonics performance and reduced power devices stress. As a result, MVSI is very attractive in high voltage and high power applications. The development of MVSI began in the early 1980s when Nabae *et al.* (1980) proposed a neutral-point clamped (NPC) PWM inverter. Since then several multilevel topologies have evolved and applied in adjustable speed drives, electric utility and renewable energy systems.

The general structure of the MVSI is to synthesize a staircase or multilevel output sinusoidal voltage out of several levels of dc voltages (Jih and Fang 1995); it can therefore be described as a voltage synthesizer. In conventional VSI, the maximum voltage output is determined by the blocking capability of each device. By using a multilevel structure, the stress on each switching device can be reduced in proportional to the number of levels, thus the inverter can handle higher voltages (Li *et al.* 2000). Consequently, in some applications it is possible to avoid an expensive and bulky step-up transformer. Another significant advantage of a multilevel output waveform is that several voltage levels lead to a better and more sinusoidal voltage waveform. As a result, a lower total harmonic distortion (THD) is obtained. Theoretically, as the number of voltage levels reach infinity, the output THD approaches zero. In motor application, high $\mathrm{d}V/\mathrm{d}t$ in power supply generates high stress on motor windings and requires additional motor insulation. Furthermore, high $\mathrm{d}V/\mathrm{d}t$ of semiconductor devices increases the electromagnetic interference (EMI), common-mode voltage and possibility of failure of the motor. With several levels in output waveform constructed by multilevel inverter, the switching $\mathrm{d}V/\mathrm{d}t$ stresses are reduced (Li *et al.* 2000).

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There are three main types of multilevel inverter topologies that have been frequently cited in the literature: (i) diode-clamped multilevel inverters (DCMI), (ii) flying capacitor multilevel inverters (FCMI), and (iii) modular structured multilevel inverters (MSMI). The above-mentioned topologies have their specific advantages and disadvantages as detailed elsewhere (Lai and Peng 1995, Ahmad Azli *et al.* 1998). The last topology (MSMI) uses cascaded inverters with separate dc sources, and hence it is naturally well suited for various renewable energy sources such as photovoltaic, fuel cell and biomass.

Another important aspect that determines the inverter performance is the PWM switching scheme. Historically, the development of PWM switching strategy was prompted by the natural sampled sinusoidal PWM technique introduced by Schonung and Stemmler (1964). This analog technique is based on the physical comparison between a carrier signal and a pure sinusoidal modulating signal. Its digital version, i.e. the regular-sampling PWM was introduced by Bowes (1975). It has simplified the PWM generation tremendously and has become the impetus for the proliferation of several important digital PWM techniques until the present day. Several currently popular PWM schemes are the selective harmonic elimination PWM (SHEPWM) (Enjeti *et al.* 1990) optimized PWM (Bowes and Midoun 1988) and more recently the space vector PWM (SVPWM) (Boys and Handley 1990). These modulation techniques were originally applied to the two-level inverter. However, it was discovered that by making some modifications they could also be suitably used for a multilevel inverter. For multilevel sinusoidal PWM in particular, different methods of carrier arrangement such as phase opposition disposition (POD), phase disposition (DP) and alternatively in phase opposition disposition (APOD) (Carrara *et al.* 1990) have been suggested. All of these techniques employ multiple carriers with a single modulating waveform.

In this report, a new PWM switching strategy for multilevel inverter is proposed. Unlike other methods, the proposed scheme is based on a SPWM with a single carrier and multiple modulating signals. It will be shown later that using the proposed modulation scheme, simple trigonometric equations to define the switching instant of inverter switches can be obtained. The derived equations can be suitably programmed using a microprocessor for an online PWM waveform generation. To validate the feasibility of the switching strategy, a five-level MSMI using the proposed scheme will be implemented.

2. Modular structured multilevel inverter (MSMI)

The modular structured multilevel inverter (MSMI) is unique when compared to other types of multilevel topologies such as DCMI or FCMI inverters, in the sense that it consists of several modules that require separate dc sources (Ahmad Azli *et al.*). This topology requires the least number of components among all multilevel converters to achieve the same voltage levels. It also avoids the necessity for complicated clamping diodes or voltage balancing capacitors. Moreover modularized circuit layout and packaging is possible because each voltage level is synthesized using a regular inverter structure.

A single-phase N-level MSMI configuration is shown in figure 1. It consists of several single-phase full-bridge inverter modules with separate dc sources. The ac output voltage of each module is connected in series to form an output voltage, V_{out}. The number of module (M), which is equal to the number of dc sources, depends on

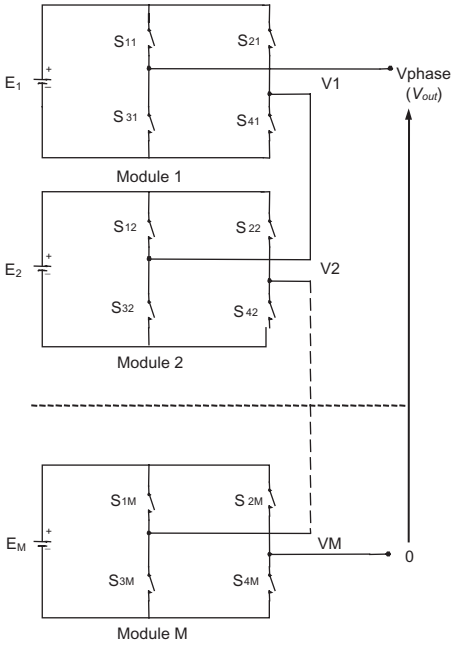


Figure 1. Single-phase structure of a MSMI.

Output Voltage	$+2E$	$+E$	0	0*	$-E$	$-2E$
Switches states						
S_{11}	On	On	On	Off	Off	Off
S_{21}	Off	Off	On	Off	On	On
S_{31}	Off	Off	Off	On	On	On
S_{41}	On	On	Off	On	Off	Off
S_{12}	On	On	On	Off	Off	Off
S_{22}	Off	On	On	Off	Off	On
S_{32}	Off	Off	Off	On	On	On
S_{42}	On	Off	Off	On	On	Off

Table 1. A possible inverter switches state for a five-level MSMI.

the number of levels (N) required. It is usually assumed that N is odd, as this would give an integer-valued M. The number of output voltage levels is defined by

$$M = \frac{N-1}{2} \tag{1}$$

By different combinations of the four switches, S_{1M} through S_{4M}, each module can generate three different voltage outputs, i.e. $+E$, $-E$, and 0. The total output voltage is constructed by the sum of the output voltage from each module. For example, a five-level inverter would have output levels of $+2E$, $+E$, 0, $-$E, and $-2E$. There are many possible ways in which the output voltage of each module can be summed-up. Table 1 presents an example of a possible combination for a five-level MSMI and their corresponding switch states.

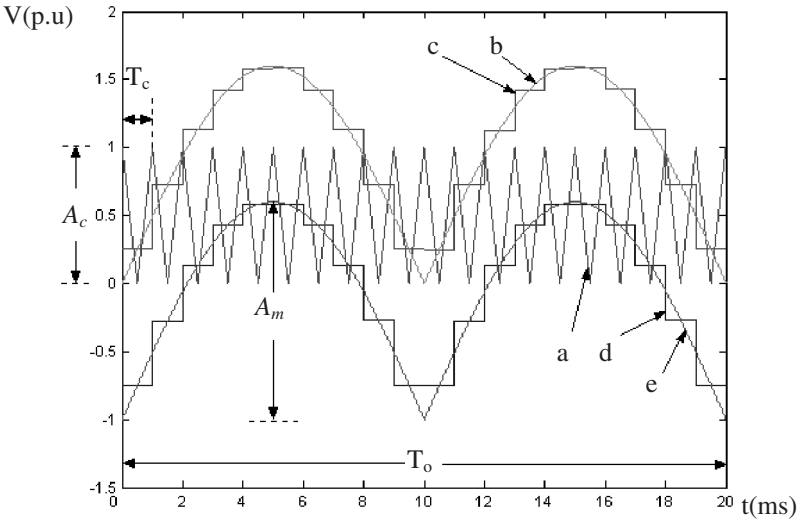


Figure 2. The modified sinusoidal modulation signals and a single carrier signal. (*a*) Carrier signal $c(k)$. (*b*) Absolute sinusoidal modulation signal $m_1(t)$. (*c*) Modified sinusoidal modulation signal $s_1(k)$ of $m_1(t)$. (*d*) Shifted absolute sinusoidal modulation signal $m_2(t)$. (*e*) Modified sinusoidal modulation signal $s_2(k)$ of $m_2(t)$.

3. The proposed modulation scheme

The proposed modulation scheme for the MSMI is based on the classical unipolar, symmetric PWM switching technique. The main idea behind this method is to compare several modified sinusoidal modulation signals $s(k)$ with a single triangular carrier signal $c(k)$ as shown in figure 2. These modified signals are the 'regular sampled' continuous sinusoidal modulating waveforms, $m(t)$. Intersection between the modified modulation signals and the carrier signal defines the switching instant of the PWM pulses. Each of these modified modulation signals have the same frequency (f_o) and amplitude (A_m). Since the modulation is symmetric, the modulation signals are sampled once in every carrier cycle.

The carrier signal is a train of triangular waveform with frequency f_c and amplitude A_c. Equation (2) defines the modulation m_i for N-level inverted with M number of modules

$$m_i = \frac{A_m}{((N-1)/2)/A_c} = \frac{A_m}{MA_c} \tag{2}$$

Therefore, if A_c defined at a fixed p.u. (1 p.u.), then m_i ranges between 0 and 1, while A_m ranges between 0 and M. The definition of the modulation ration m_f for the multilevel inverter is similar to the conventional two-level output inverter, i.e.

$$m_f = \frac{f_c}{f_o} \tag{3}$$

In this equation, f_c and f_o correspond to the frequencies of the carrier and sinusoidal modulation signals, respectively. To illustrate the principal of the proposed scheme, a five-level inverter at $m_i = 0.4$ and $m_i = 0.8$ is shown in figure 3 and figure 4 respectively. For clarity, m_f for bath cases was arbitrarily chosen to be a low value of 20.

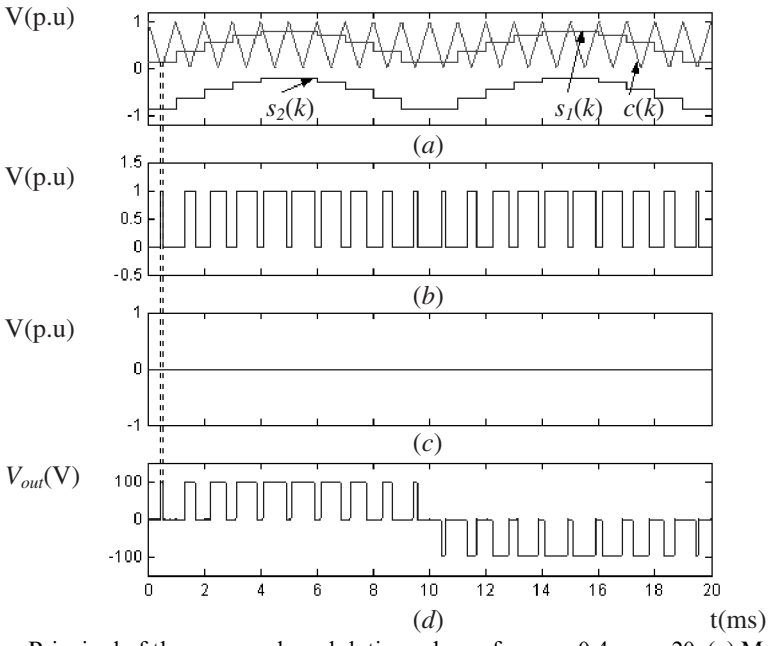


Figure 3. Principal of the proposed modulation scheme for $m_i = 0.4$, $m_f = 20$. (*a*) Modulation signals and carrier signal. (*b*) PWM pulses produced from comparison between $s_1(k)$ and $c(k)$, $V_1(k)$. (*c*) PWM pulses produced from comparison between $s_2(k)$ and $c(k)$, $V_2(k)$. (*d*) PWM output waveform.

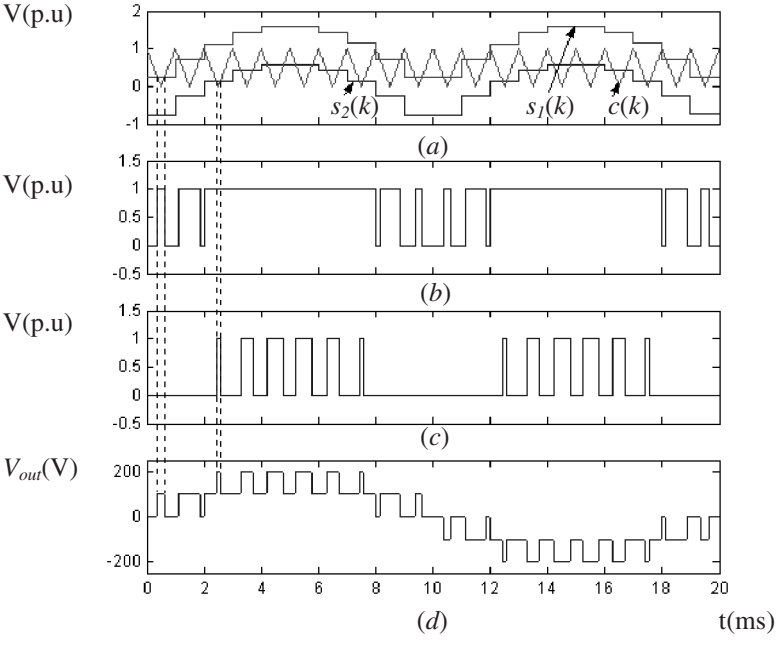


Figure 4. Principal of the proposed modulation scheme for $m_i = 0.8$, $m_f = 20$. (*a*) Modulation signals and carrier signal. (*b*) PWM pulses produced from comparison between $s_1(k)$ and $c(k)$, $V_1(k)$. (*c*) PWM pulses produced from comparison between $s_2(k)$ and $c(k)$, $V_2(k)$. (*d*) PWM output waveform.

For a five-level output, two modulation signals namely $s_1(k)$ and $s_2(k)$ and single triangular carrier $c(k)$ are involved in the modulation process. Signal $s_2(k)$ is actually $s_1(k)$ shifted down by the amplitude of triangular carrier signals A_c.

The PWM pulses $V_1(k)$ is generated from the comparison between s_1(k) and $c(k)$ while $V_2(k)$, is from comparison between $s_2(k)$ and $c(k)$. The comparison is designed such that if $s_1(k)$ is greater than $c(k)$, a pulse-width $V_1(k)$ is generated; if $s_2(k)$ is greater than $c(k)$, $V_2(k)$ is generated. On the other hand if there is no intersection, then $V_1(k)$ and $V_2(k)$ remain at 0. It can be seen in figure 3 that for the case of $m_i \leq 0.5$, only $s_1(k)$ and carrier signal $c(k)$ is involved in the modulation process. There is no intersection for $s_2(k)$. Therefore, the output pulse $V_2(k)$ is zero. The output voltage V_{out} which is the sum of $V_1(k)$ and $V_2(k)$, is then similar to the conventional three-level unipolar PWM case. For $m_i > 0.5$, as depicted in figure 4, both modulating signals, i.e. $s_1(k)$ and $s_2(k)$, intersect the carrier and therefore V_1 and V_2, pulses are generated. As a result, a multilevel output voltage V_{out} is formed.

4. Derivation of the switching angle equations

This section outlines the method used to obtain mathematical expressions that define the switching instants for the inverter switches. The initial derivation is based on a five-level MSMI and, by extending the result, a general equation for N-level MSMI can be accomplished. The derivation is intended to generate PWM signals $V_1(k)$ and $V_2(k)$ as depicted in figure 4. For clarity, it is zoomed as shown in figure 5.

It can be seen that the kth rising edge is defined as the intersection of the negative slope carrier $c^-(k)$ and two set of modulating signals $s_1(k)$ and $s_2(k)$. The variable k represents a position of each modulated width pulses $V_1(k)$ and $V_2(k)$, initiated from $k = 1, 2, 3 \ldots m_f$. Since the waveform is symmetrical, the intersection of the positive slope carrier $c^+(k)$ and the modulating signals is not required. It can be deduced from the rising edge equations, i.e. the intersection between $c^-(k)$ and $s_1(k)$ or $s_2(k)$.

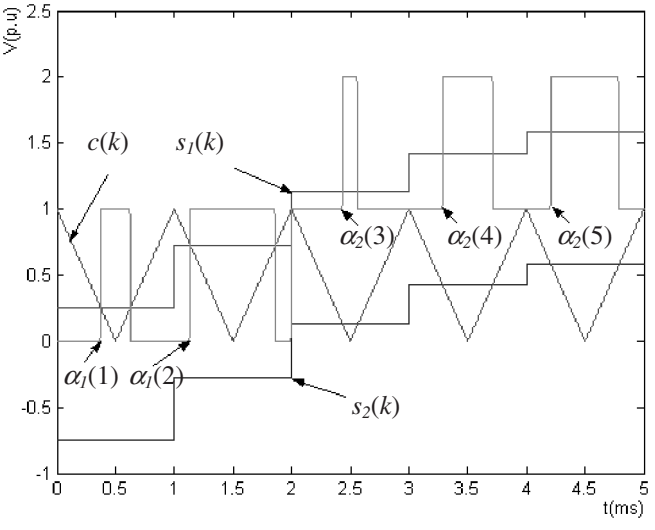


Figure 5. Intersection between single carrier and modulation signals in first quarter wave.

The straight-line equation for the carrier wave is denoted by $c^{-}(k)$ for the negative slope. It can be expressed as

$$c^{-}(k) = \left(\frac{-A_c}{T_c/2}\right)\alpha_k + hA_c, \quad k = 1, 2, 3, \ldots, \quad h = 1, 3, 5, \ldots \tag{4}$$

The relationship between T_c, f_c, f_o and m_f can be written

$$T_c = \frac{1}{f_c} \tag{5}$$

$$f_c = m_f f_o \tag{6}$$

where T_c is a period of carrier signal, f_c is a carrier frequency and f_o is a modulating signal frequency. The symmetric regular sampled modulation signals $s_{1k}(k)$ and $s_{2k}(k)$ can be expressed as

$$s_1(k) = A_m \sin\left[\omega(i) + \frac{\pi}{m_f}\right] \tag{7}$$

$$s_2(k) = A_m \sin\left[\omega(i) + \frac{\pi}{m_f}\right] - A_c \tag{8}$$

$i = 0, 1, 2, 3, \ldots$ when the modulation signal interect with $c^{-}(k)$.

The angular frequency ω in (7) and (8) is represented by

$$\omega = 2\pi f_o \times \frac{T_o}{m_f} = \frac{2\pi}{m_f} \tag{9}$$

From the arithmetic regression equation

$$T_n = a + (n-1)d \tag{10}$$

where $T_n = n$th number, $a = T_1 =$ first number, $d =$ increment/decrement of next number and $n = 1, 2, 3 \ldots$.

Using the arithmetic regression in (10) and realizing that k is equal to n, then the relationship between h and i with k can be rewritten as

$$h = 2k - 1 \tag{11 a}$$

and

$$i = k - 1 \tag{11 b}$$

The kth raising edge ($\alpha_1(k)$) of PWM signal $V_1(k)$ is produced by the intersection between $s_1(k)$ and $c^{-}(k)$, i.e.

$$\left(\frac{-A_c}{(T_c/2)}\right)\alpha_1(k) + hA_c = A_m \sin\left(\omega(i) + \frac{\pi}{m_f}\right)$$

To solve this the rising edge kth transition point $\alpha_1(k)$ is represented by

$$\alpha_1(k) = \frac{T_c}{2}\left[(2k-1) - \frac{A_m}{A_c}\sin\left(\omega(k-1) + \frac{\pi}{m_f}\right)\right] \tag{12}$$

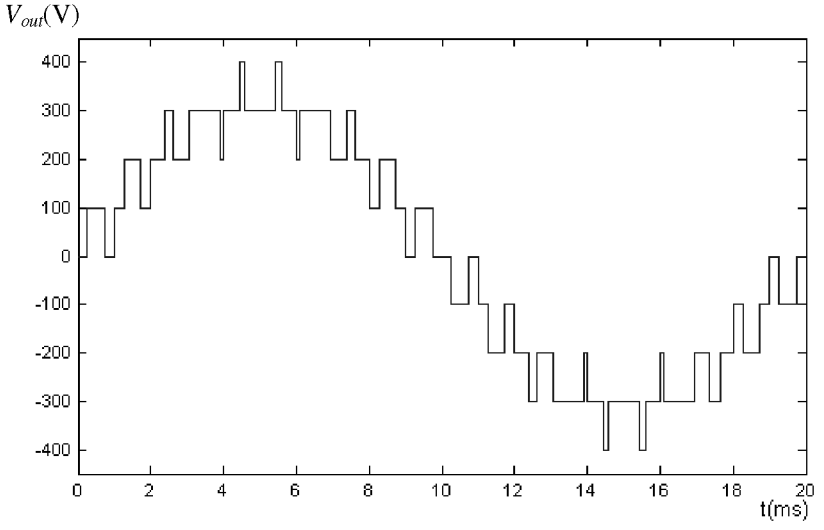


Figure 6. Nine-level inverter output waveform for $m_i = 0.8$ and $m_f = 20$.

Using the same method, i.e. the intersection between $s_2(k)$ with $c^-(k)$, every rising edge $\alpha_2(k)$ of PWM signal $V_2(k)$ can be expressed as

$$\alpha_2(k) = \frac{T_c}{2}\left[2k - \frac{A_m}{A_c}\sin\left(\omega(k-1) + \frac{\pi}{m_f}\right)\right] \tag{13}$$

Equations (12) and (13) can be generalized to produce a general switching angle for an N-level inverter, i.e.

$$\alpha_M(k) = \frac{T_c}{2}\left[(2k + M - 2) - \frac{A_m}{A_c}\sin\left(\omega(k-1) + \frac{\pi}{m_f}\right)\right] \tag{14}$$

where

$$M = \frac{N-1}{2}$$

Equation (14) can be used to generate the kth PWM pulses for any level of M. An example of the application of the equation on a nine-level MSMI are shown in figure 6. It can also be noted that (14) is non-transcendental and its practical implementation using a simple microcontroller is therefore possible.

5. Hardware implementation

A proof-of-concept five-level experimental rig is built to implement the proposed modulation technique. The inverter input voltages are fixed at 100 V dc for each module and the inverter load is purely resistive. The generation of the PWM pulses is implemented using a relatively simple, 16-bit fixed-point microcontroller (SIEMENS SAB-C167CR-LM). A MATLAB-Simulink block simulation is also carried out to confirm the validity of the results.

6. Results

6.1. *Output voltage waveforms*

Figure 7 shows the oscillogram of the output voltage and current of the inverter for $m_i = 0.4$ and $m_f = 20$. As can be observed, the output voltage is similar to a three-level inverter because $m_i < 0.5$. For the case of $m_i = 0.8$ and $m_f = 20$ shown in figure 8, the five-level PWM waveform is obtained. The results are consistent with the theoretical predictions shown by the simulation plots.

For the case of $m_f = 20$ and $m_i = 0.4$, the practical result of output voltage harmonic spectrum are shown in figure 9(*a*). The theoretical spectrum for the similar case is shown in figure 9(*b*). By comparing figures 9(*a*) and (*b*), it can be clearly observed that the harmonics incidences for $m_i \leq 0.5$ agree closely with theoretical predictions. The proposed modulation scheme produces only odd harmonics for even modulation ratio. Furthermore, harmonics at the carrier and the multiples of carrier frequency do not exist at all. For the case of $m_f = 20$ and $m_i = 0.8$, practical and theoretical results of the output voltage harmonic spectrum are illustrated in figure 10(*a*) and (*b*), respectively. Again, it can be seen that as far as the harmonics incidences are concerned, the practical results agree with theory. Note that for five-level inverter, $m_i = 0.4$ is 'equivalent' to $m_i = 0.8$ for a three-level inverter. For an equivalent modulation index, the significant harmonic of a five-level is half compared to a three-level inverter.

5.2. *Other performance indexes*

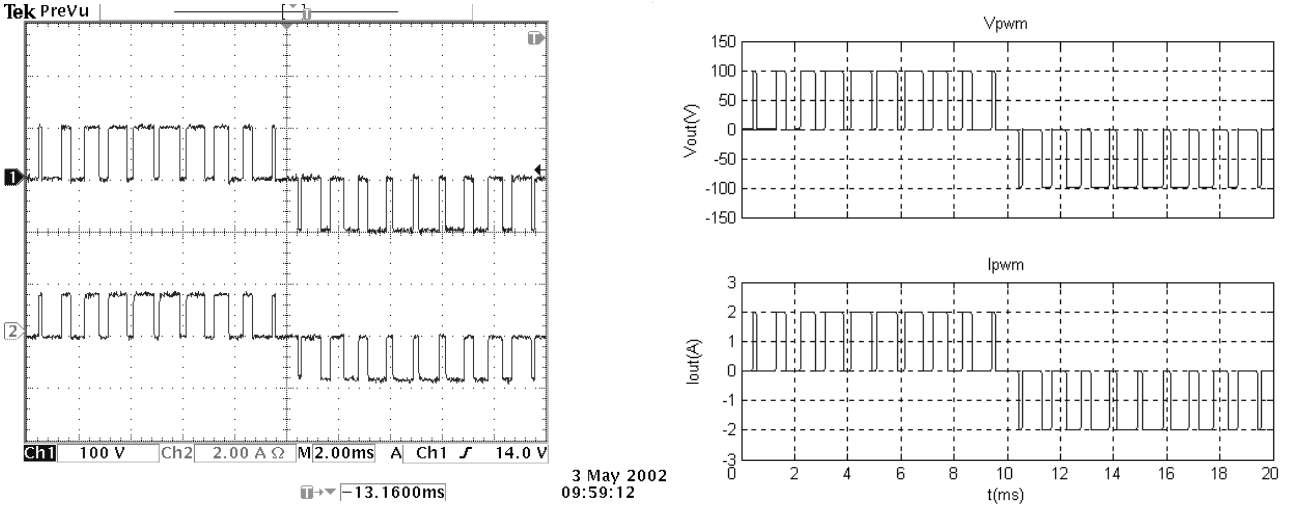
Total harmonic distortion (THD) is the most common power quality index to describe the quality of the power electronic converter (Abbas 2000). For an inverter application, THD represents how close the ac output waveform is to the pure sinusoidal waveform. The THD of the output voltage can be defined as

$$\mathrm{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} V_h^2}}{V_1} \tag{15}$$

where n denotes the harmonic order and 1 is the fundamental quantity. A high-quality inverter system should have low THD.

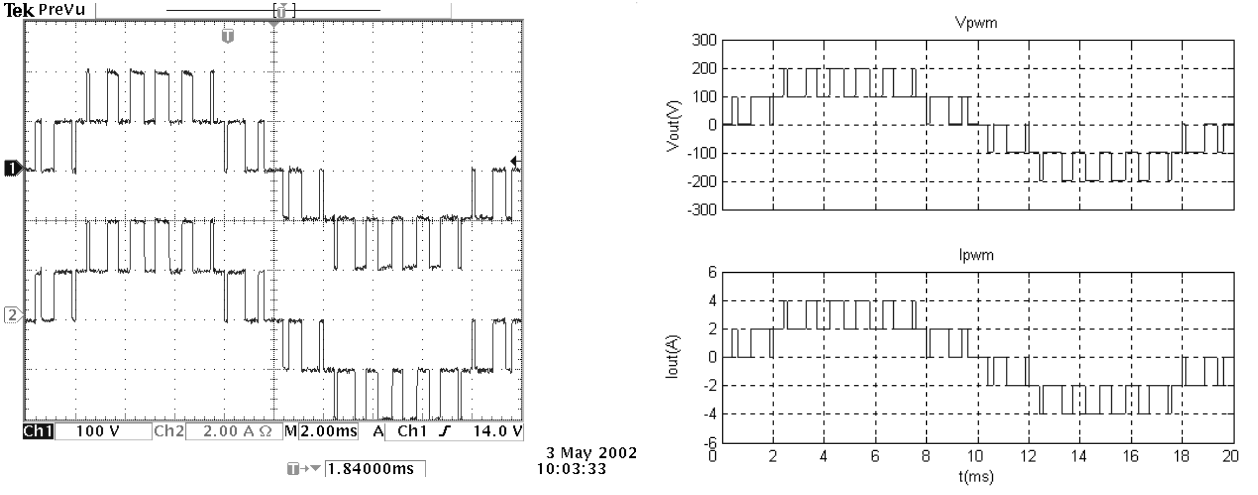
Figure 11 shows the comparison of the THD between a five-level single-phase MSMI and a conventional two-level inverter configuration. The figure shows that for both cases, a poor THD are obtained when the inverter operated at low modulation index. This is to be expected because at $m_i \leq 0.5$, the MSMI essentially behaves like a conventional three-level inverter. A better THD is obtained when the inverter operated at higher modulation index. For example, at modulation index equals 1.0, it was found that THD for a MSMI inverter is three times superior compared to a conventional two-level inverter.

Another important quality index of PWM technique is related to losses in inverter-fed ac drives which is quantified as harmonic loss factor (HLF) (Enjeti *et al.* 1990). The harmonic equivalent circuit of an induction machine can be assumed



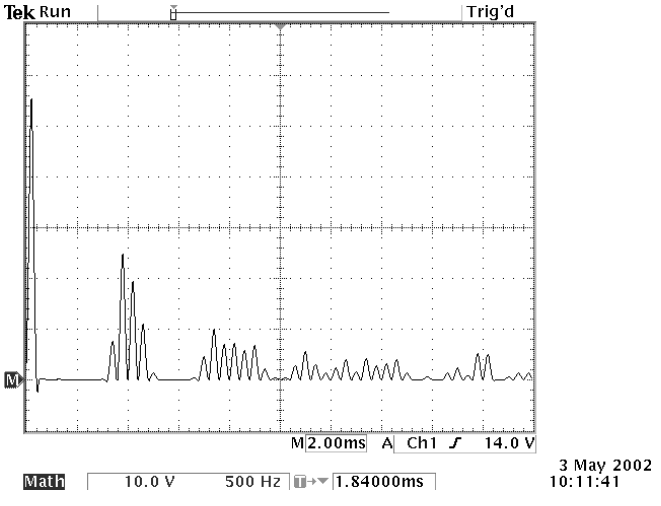
(*a*) (*b*)

Figure 7. (*a*) Practical result for $m_i = 0.4$, $m_f = 20$. (*b*) Simulation. Top trace: output voltage; vertical scale 100 V/div. Bottom trace: output current; Vertical scale 2 A/div. Horizontal scale 2 ms/div.

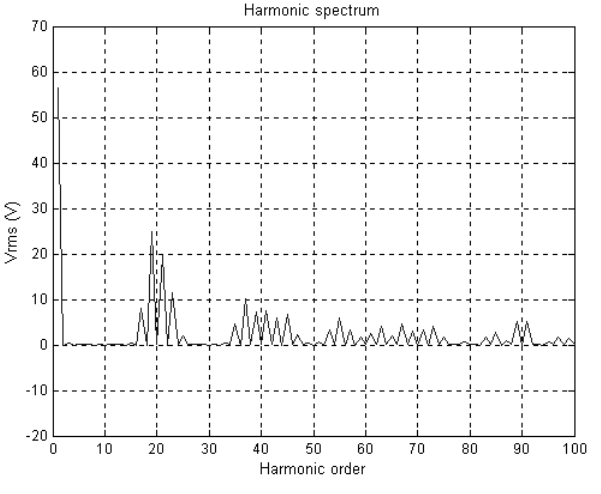


(*a*) (*b*)

Figure 8. (*a*) Practical result for $m_i = 0.8$; $m_f = 20$. (*b*) Simulation. Top trace: output voltage; vertical scale 100 V/div. Bottom trace: output current; Vertical scale 2 A/div. Horizontal scale 2 ms/div.

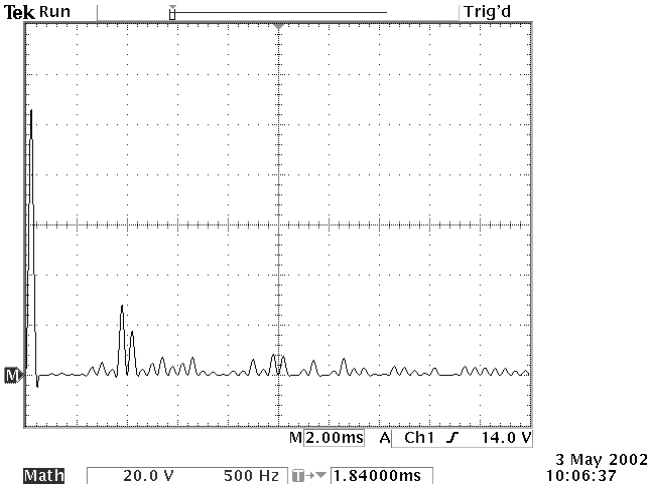


(*a*)

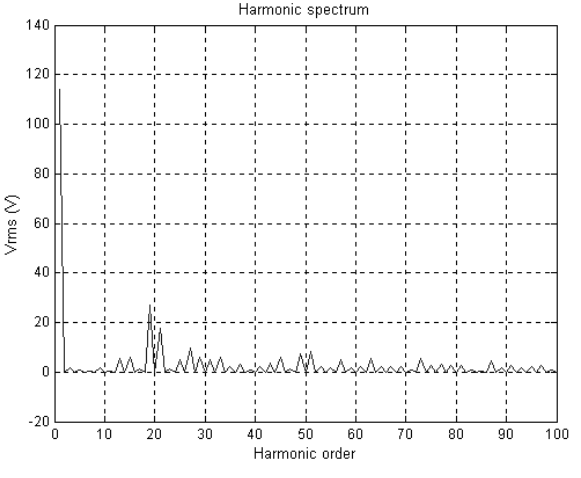


(*b*)

Figure 9. (*a*) Practical harmonic spectrum of output voltage for $m_i = 0.4$; $m_f = 20$. (*b*) Simulation. Vertical scale 10 V/div. Horizontal scale 500 Hz/div.



(*a*)



(*b*)

Figure 10. (*a*) Theoretical harmonic spectrum of output voltage for $m_i = 0.8$; $m_f = 20$. (*b*) Simulation. Vertical scale 10 V/div. Horizontal scale 500 Hz/div.

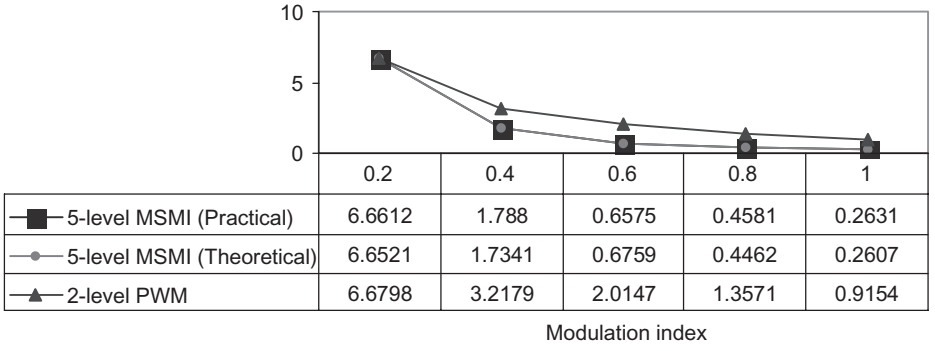


Figure 11. Variation of THD for five-level and two-level SPWM inverter configuration. Note: Data for two-level SPWM is obtained from Mohan *et al.* (1995).

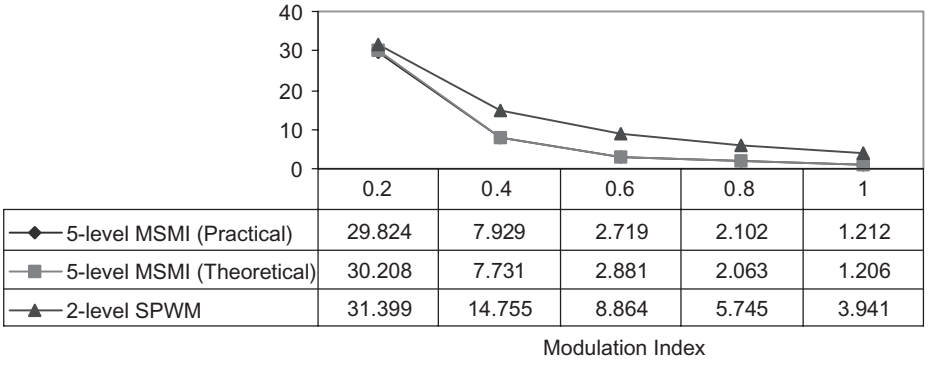


Figure 12. Variation of HLF for five-level and two-level SPWM inverter configuration. Data for two-level SPWM is obtained from Mohan *et al.* (1995).

to be its total leakage reactance at the harmonic frequency. The HLF, which is proportional to total rms harmonic current, can be defined as (Enjeti *et al.* 1990)

$$\mathrm{HLF} = \frac{100}{V_{L1}} \sqrt{\sum_{n=5}^{\infty} \left[\frac{V_n}{n}\right]^2} \tag{16}$$

where V_n is harmonic voltage. A good inverter-fed ac drive system should have a low HLF. Figure 12 shows the variation of HLF for single-phase five-level MSMI and a conventional two-level inverter. The figure shows that for both inverter types, a poor HLF are obtained when the inverter operated at low modulation index. However, at higher modulation index, the HLF improve tremendously. For example, at $m_i = 1.0$, the HLF of the MSMI is reduced to about one third of the two-level inverter. The result is expected because in general, the HLF will follow the trend of THD.

Inverter power supplies such as uninterruptible power supplies (UPS) employ an *L–C* filter between the inverter and the load. The main purpose of this filter is to provide harmonic attenuation, which is proportional to the square of the order (n) of

	0.2	0.4	0.6	0.8	1
5-level MSMI (Practical)	1.475	0.391	0.141	0.109	0.069
5-level MSMI (Theoretical)	1.482	0.386	0.148	0.119	0.072
Two-level SPWM	1.556	0.725	0.431	0.278	0.193

Modulation index

Figure 13. Variation of DF_2 for five-level and two-level SPWM inverter configuration. For two-level SPWM, data obtained from Mohan *et al.* (1995)

the harmonic. A distortion factor that represents total harmonic content at the output of a second-order filter as can be described as (Enjeti *et al.* 1990)

$$DF_2 = \frac{100}{V_{L1}} \sqrt{\sum_{n=5}^{\infty} \left[\frac{V_n}{n^2}\right]^2} \tag{17}$$

For an inverter power supply a PWM scheme that results in minimum DF_2 is desirable.

Figure 13 illustrates the DF_2 variation for a single-phase five-level MSMI and a two-level conventional inverter. The figure demonstrates that the DF_2 for five-level MSMI and two-level inverter is about equal when the modulation index is low. However as the index increases, the DF_2 for the MSMI reduces significantly compared to two-level inverter. At $m_i = 1.0$, it can be observed that DF_2 for MSMI is three times better than the two-level inverter.

From the analyses for THD, HLF and DF_2 above, it can be concluded that the performance of MSMI as far better than the conventional two-level inverter. It should noted that for purpose of simplicity analysis was carried for one particular value of modulation ratio, i.e. $m_f = 40$. However, it was found that for other values of m_f (above 30), the trend does not change very much. This is in conformity with the conclusion described in (Enjeti *et al.* 1990). It also important to note that the number of harmonics considered in all the above calculation is only up to the fourth cluster.

6. Summary

This paper presents a new switching scheme for a modular structured multilevel inverter (MSMI). The proposed scheme is based on symmetric regular sampled unipolar PWM, with multiple modulating waveforms and a single carrier. Mathematical equations that define the PWM switching instants is derived and verified by a hardware test rig. The derived equations are implemented by a low-cost fixed-point microcontroller. Several tests are used to quantify the performance of the inverter under the proposed modulation scheme. From the comparison between the output voltage and current waveform of a five-level MSMI, it was found in general that the practical results are in good agreement with theory. Analyses on the performance of the MSMI with the proposed modulation are

carried out further by calculating the THD, HLF and DF_2 indexes. It can be concluded that the harmonic performance of a modular structured five-level inverter using the proposed modulation scheme is superior compared to a conventional two-level inverter.

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