# A NEW PWM SCHEME FOR CASCADED MULTILEVEL INVERTER USING MULTIPLE TRAPEZOIDAL MODULATION SIGNALS

**Ayob, S.M, Salam, Z.**

Department of Energy Conversion,
Faculty of Electrical Engineering,
Universiti Teknologi Malaysia,
81310 UTM Skudai, Johor Bahru,
Malaysia
Email: shahrin@suria.fke.utm.my

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## Abstract

This work proposes a new PWM scheme for the Cascaded Multilevel Inverter (CMI). The proposed scheme uses multiple trapezoid modulating signals with a single triangular carrier. The scheme offers several advantages compared to Sinusoidal PWM (SPWM) in terms of easy and fast real-time waveform generation with higher fundamental output voltage. This paper details the technique and the parameters that affect its performance. A low power 5-level CMI prototype is constructed to verify the viability of the modulation scheme.

## 1 Introduction

Multilevel voltage source inverter (VSI) has been recognized as an important alternative to the normal two levels VSI, especially in high power application. Using multilevel technique, the output voltage amplitude is increased, switching devices stress is reduced and the overall harmonics profile is improved. Several multilevel topologies are reported [2,3], but the one considered in this paper is known as the Cascaded Multilevel Inverter (CMI) This topology is inherently simple and modular in structure and requires less components count [2]. The N level CMI is shown in Figure 1.

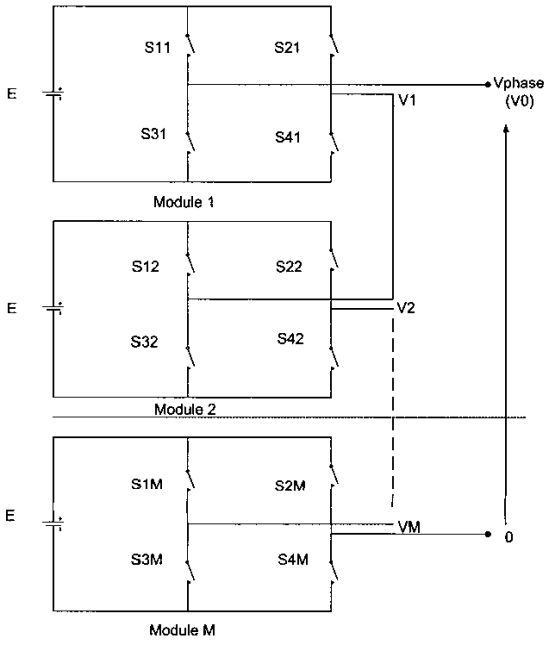



Figure 1: CMI N-level structure

By far, the most popular modulation method for VSI is the Sinusoidal PWM (SPWM) method. Historically, the development of PWM switching strategy was prompted by the natural sampled sinusoidal PWM technique introduced by Schoung and Stemmler in early 1960's. This analog method compares a triangular carrier with a sinusoidal modulation signal, and the intersection between the signals determines the switching instants. In 1975, its digital version, i.e the regular-sampling PWM was introduced by Bowes. It has simplified the PWM generation tremendously and has become the impetus for the proliferation of several important digital based PWM modulation technique. Several currently popular PWM schemes are the selective harmonic elimination PWM (SHEPWM) [4], optimized PWM [7], and more recently the space vector PWM (SVPWM)[1].

Abovementioned PWM modulation techniques were originally applied to the two-level inverter. However, it was discovered that by making some modifications they could be also be used for multilevel inverter. For multilevel sinusoidal PWM in particular, different methods of carrier arrangement namely the phase opposition disposition (POD), alternatively in phase opposition disposition (APOD) and phase disposition (PD) have been suggested [2]. All of these techniques employ multiple carriers with single modulating signal

waveform. The resulting harmonics profiles were quite distinct and are discussed elaborately elsewhere [2].

In this paper, a new PWM switching scheme for the CMI inverter is proposed. Contrary to others techniques proposed by other researchers, this method uses multiple trapezoid modulating signal waveforms with a single triangular carrier. The employment of trapezoidal modulation offers several advantages. It provides simple signal generation with minimal digital circuitry, avoidance of look-up tables that require large data bases. It also provides higher fundamental output voltage compared to SPWM.

## 2 The Proposed Modulation Scheme

### 2.1 Modulation Principle

The proposed modulation scheme is based on the classical unipolar PWM switching technique. It uses a single triangular carrier $c(t)$ and multiple trapezoid $m(t)$ modulating signals, as shown in Figure 2. The intersection between the trapezoid signals and carrier signal defines the switching instant of the PWM pulse. The number of trapezoidal modulating signals depends on the number of modules ($M$) of the CMI inverter. Each of the trapezoid modulating signals has the same frequency $f_m$ and amplitude $A_m$.

Figure 3 characterized the trapezoidal signal by its slope angle, $\alpha$. As can be seen, the shape of the trapezoidal waveform varies with $\alpha$. If $\alpha = 0$, the trapezoidal resemble a square wave; $\alpha = 90^0$, will result in triangular wave. As a result, for different values of $\alpha$, different harmonics profile will be obtained. For a 5-level CMI inverter as shown in Figure 2, two modules are needed, thus the trapezoidal signals are:

$$m_1(t) = m(\alpha, 2\pi f_m t) \quad (1)$$

$$m_2(t) = m(\alpha, 2\pi f_m t) - 1 \quad (2)$$

The carrier signal is a train of triangular waveform with a frequency $f_c$ and amplitude $A_c$. The relationship of modulation index ($m_i$) and modulation ratio ($m_f$) for N-level inverter can be represented as:

$$m_i = \frac{A_m}{\frac{(N-1)}{2} A_c} = \frac{A_m}{MA_c} \quad (3)$$

$$m_f = \frac{f_c}{f_o} \quad (4)$$

As $m_i$ ranges between 0 and 1, $A_m$ ranges between 0 and $M$ while $A_c$ remains fixed at 1 p.u. The intersection between modulation signals and the carrier produces the PWM signals. These signals can then be used to drive the actual gating signals for the power devices in each inverter module.

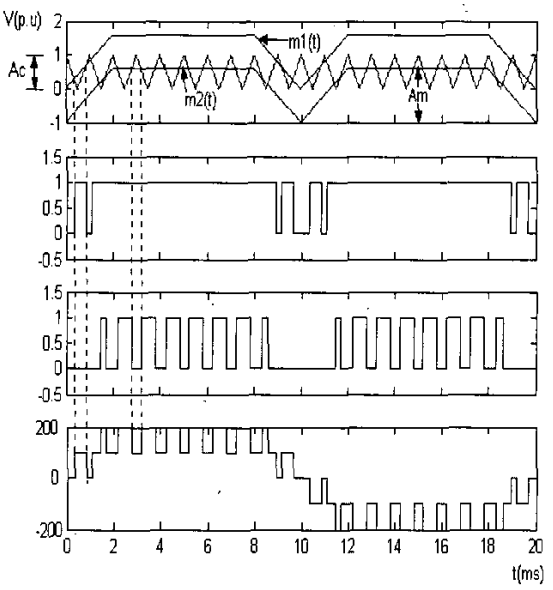



Figure 2: PWM technique for 5-level inverter

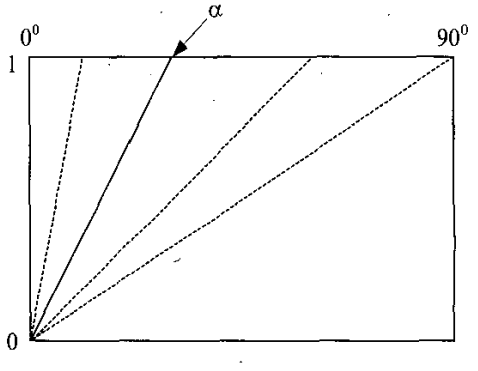



Figure 3: Characterization of the trapezoidal slope angle $\alpha$

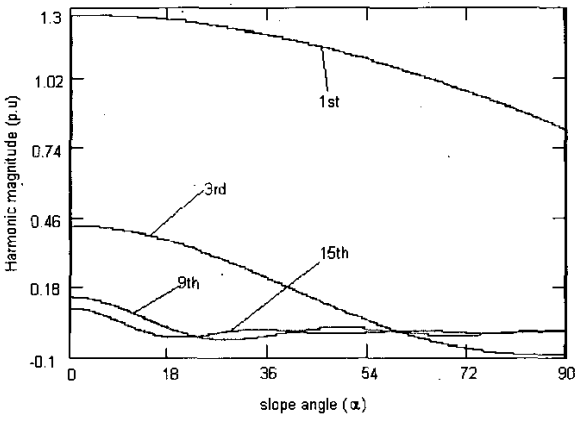
### 2.2 Trapezoidal Reference Signal Harmonic Content

The harmonic content of the trapezoidal reference signal, having an angle $\alpha$ between $0^0$ and $90^0$ as in Figure 3 can be found using a standard Fourier analysis. By assuming quarter-wave symmetry, only odd sine terms are present. Thus, the sine-term Fourier coefficient can be expresses as:

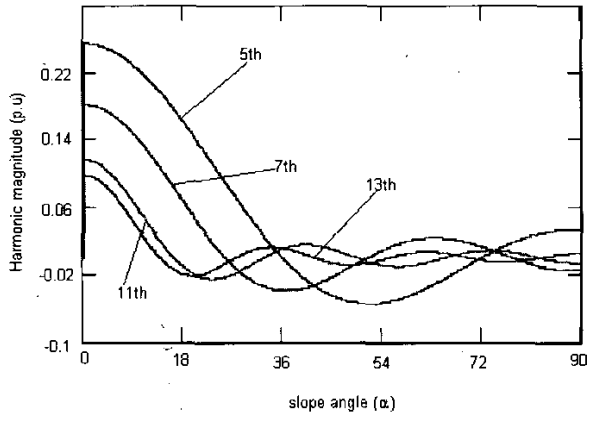
$$A_n = \frac{4}{\pi} \int_{\theta=0}^{\pi/2} F(\theta).\sin(n\theta)d\theta \quad (5)$$

and can be simplified to the general expression:

$$A_n = \frac{4}{n^2\pi} x \frac{\sin(n\alpha)}{\alpha} \quad (6)$$




(a) Harmonics: Fundamental, 3rd, 9th and 15th




(b) Harmonics: 5th, 7th, 11th and 13th

Figure 4 (a) and (b): Harmonics of trapezoidal signal over $\alpha$

The voltage harmonics versus $\alpha$ calculated from equation (6) is as shown in Figure 4 (a) and 4 (b). Figure 4 (a) shows the magnitude of the fundamental component, 3rd, 9th and 15th harmonic, while Figure 4 (b) shows the magnitude of the 5th, 7th, 11th and 13th harmonic. As can be seen from Figure 4(a) and (b), some of the harmonics can be eliminated, if a correct value of $\alpha$ is chosen. In case of $\alpha = 36^0$, for example, the fifth harmonic is eliminated. Thus, by carefully selecting $\alpha$, the low-order harmonic content of trapezoidal signal can be reduced.

### 2.3 PWM Output Waveform Harmonics Performance

PWM output waveform harmonic performance can be improved by eliminating more reference signal low-order harmonic content. If a three-phase system is considered, the triplens are allowed, then it is appropriate to choose $m_f$ equal to odd and multiple of three. In such a case, $\alpha$ is selected to be $36^0$ or $72^0$, so as to eliminate the fifth harmonic. This in turn, improves PWM waveform harmonic performance. Since slope angle of $36^0$ provides higher fundamental compared to $72^0$, the former angle is preferable.

## 3 Inverter Simulation

To obtain an insight on the proposed modulation scheme, a MATLAB simulation was carried out. The 5-level CMI inverter system is simulated using SIMULINK, a simulation interface provided by MATLAB. It is assumed that the dc voltage input for each module is E = 100V, the output voltage fundamental frequency, $f_o$= 50Hz and the carrier frequency, $f_c$ = 20K Hz ($m_f$ = 40) while $m_i$ and $\alpha$ is set to 0.8 and $36^0$, respectively. The block diagram of the control scheme and the inverter is as shown in Figure 5. While Figure 6 (a) and 6 (b) shows the resulting output voltage and its harmonic spectra.

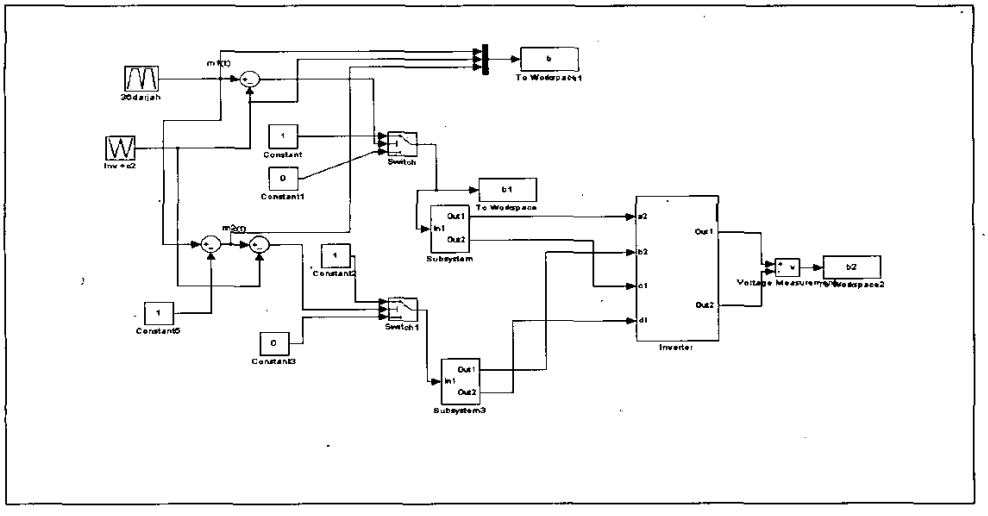



Figure 5: Block diagram of inverter system

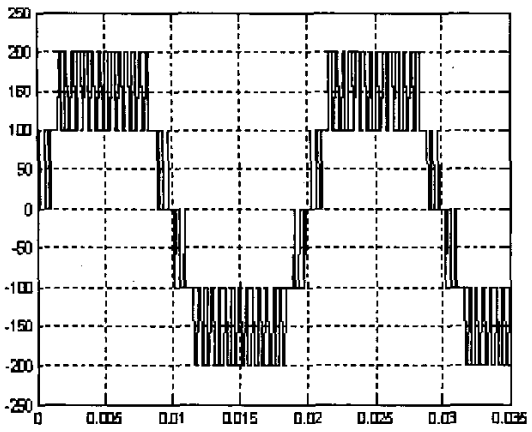



Figure 6 (a): Simulated 5-level output voltage

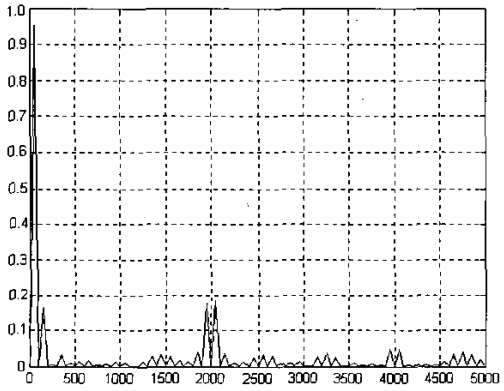



Figure 6(b): Output harmonic spectra

## 4 Hardware Implementation

Trapezoid signal shape can be easily generated digitally in real-time with minimal circuitry. It avoids the usage of sinusoidal reference look-up table together with the associated digital circuitry and large data access time [5]. Compared to sinusoidal reference signal, trapezoid signal can be easily implemented in gate-array based modulator such as Field Programmable Gate Array (FPGA).

A low-voltage 5-level CMI test-rig has been constructed to verify viability of the proposed scheme. Figure 7 shows the flow chart of the low voltage test-rig.

In this work, the development of the proposed scheme is done using MAX-Plus II, which is the Altera development tool. Its converts the design idea into a configuration data files, which then could be loaded to the Altera FPGA device. In this work, EPF10K70RC24, a low cost FPGA device from Altera is used.

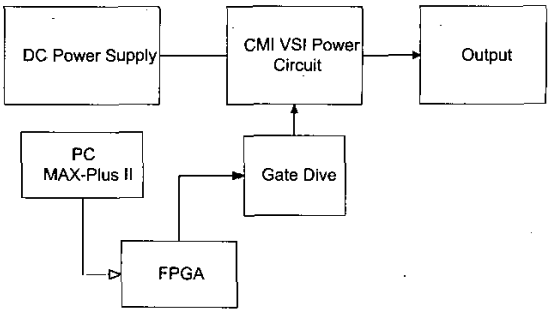



Figure 7: Flowchart of test-rig to implement the CMI VSI

A hierarchal design methodology has been implemented in the development process of the proposed scheme. The top-level design used schematic as an entry level and the lower level used a mixture of graphical and language-based design. The top level of Altera schematic diagram is shown in Figure 8, while Figure 9 shows an example of gate signal from MAX-Plus II.

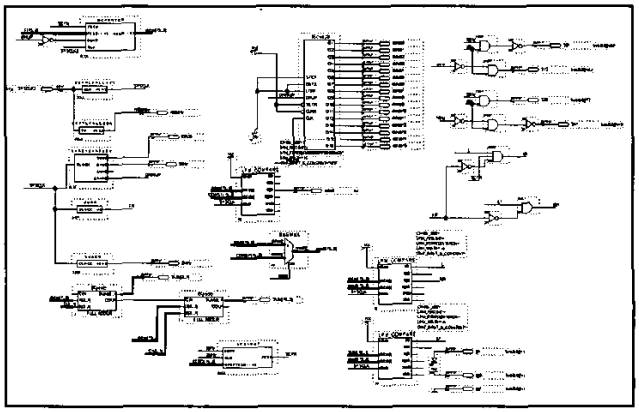


Figure 8: Top level schematic diagram

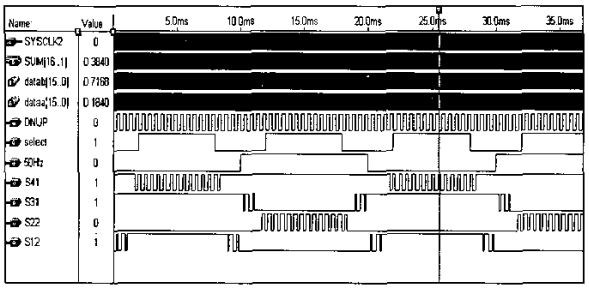



Figure 9: Gate signal from MAX-Plus II

## 5 Hardware Results

Figure 10 (a) and (b) shows the practical output voltage and its harmonic spectra obtained from the test-rig, respectively. The conditions are set as follows: DC voltage source = 100V,

$m_i = 0.8$, $m_f = 40$ and $\alpha = 36^0$. As can be seen, the hardware results are in close agreement with the simulation.

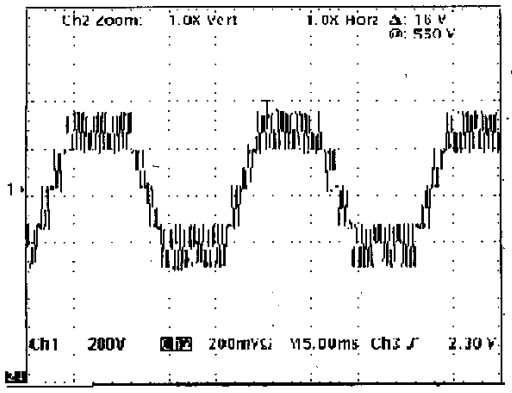



Figure 10 (a): Practical 5-level CMI output voltage

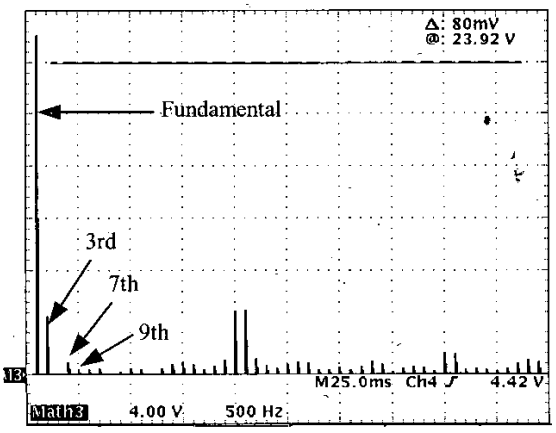



Figure 10 (b): Practical 5-level CMI harmonic spectra output

Note that the third harmonic magnitude is quite high: however, as has been discussed earlier, it can be eliminated in three-phase system if $m_f$ is chosen to be odd and multiple of three. The fifth harmonic is eliminated as $\alpha$ is chosen equal to $36^0$.

From the experiment data, it was found that the output fundamental component is not solely dependent with modulation index, $m_i$. It is also influenced by the trapezoidal slope angle, $\alpha$. A higher fundamental magnitude can be obtained with a smaller value of $\alpha$. However larger $\alpha$ will degrade the output harmonic performance as the amplitude of low-order harmonics grow. For case $m_i = 0.8$, with $\alpha = 36^0$, the fundamental magnitude obtained is 0.952 (normalized value).

Furthermore, it was also found that under the proposed scheme, only odd harmonics exist since the reference modulation signal is quarter-wave symmetry. The incidences of the harmonics depend on the modulation ratio. The harmonics produced are shifted to high frequency when the modulation ratio is increased. The amplitude of each harmonic is influenced by the modulation index and the trapezoidal slope angle, whereby a better harmonic performance can be obtained when the modulation index get closer to 1.0 and slope angle closer to $90^0$.

## 6 Conclusion

This work proposed a new switching strategy for Cascaded Multilevel Inverter, using the multiple trapezoidal modulation waveforms with a single triangular carrier. The scheme offers several advantages compared to Sinusoidal PWM (SPWM) in terms of easy and fast real-time waveform generation and higher fundamental output voltage. However its output harmonic performance is inferior compared to SPWM due to the existence of low-order harmonics, but can be improved by selecting the appropriate trapezoidal slope angle, $\alpha$. A low voltage FPGA-based 5-level CMI was constructed to verify the viability of the modulation strategy. It was found that the practical result agree very closely with simulation.

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