AN ISOLATED BIDIRECTIONAL INVERTER USING HIGH FREQUENCY CENTER-TAPPED TRANSFORMER

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Abstract

This paper proposes a bidirectional high-frequency link inverter using a high-frequency center-tapped transformer. The main feature of the inverter is fewer number of power switches used. On the secondary side of the transformer, the active rectifier employs only two switches, thus reducing the switching losses. Furthermore, a modified sinusoidal Pulse Width Modulation (PWM) has been applied to increase the efficiency of the inverter. A 1 kW prototype has been constructed and experiments were carried out to verify the viability of the proposed inverter.

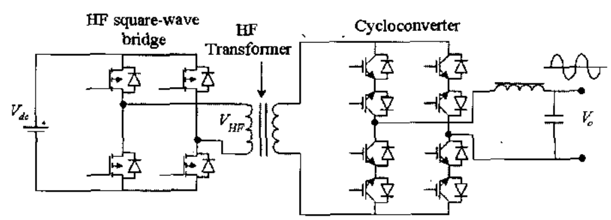
1 Introduction

High frequency (HF) link inverters are widely used in uninterruptible power supply (UPS) and renewable energy sources applications. Compared to the inverter that uses 50Hz isolation transformer, HF link inverter offers significant advantages in terms of compactness, weight and cost. By utilizing high frequency isolation transformer, the converter size and weight can be drastically reduced.

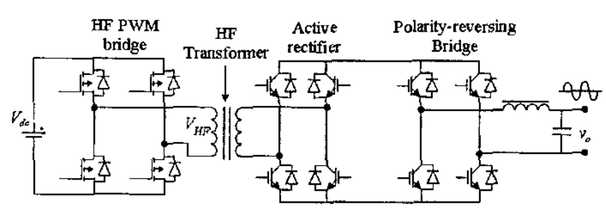
The two well-known HF link inverters are the "cycloconverter" and the "dc-dc converter" types. The cycloconverter HF link inverter, suggested by Matsui [1] is shown in Fig. 1(a). This inverter is capable of bidirectional power flow. The main advantage of this topology is that it requires only two conversion stages, namely the HF square-wave bridge and the cycloconverter circuit. The major disadvantage is that all the (twelve) power switches operate at high frequency, resulting in appreciable switching losses. Furthermore the required switching scheme for the cycloconverter section is quite complex.

The dc-dc converter type consists of three power stages i.e. the HF PWM bridge, active rectifier and polarity-reversing bridge [2]. The circuit configuration is shown in Fig. 1(b). This topology is robust and is also capable of bidirectional power flow. However, it appears that substantial power losses occur due to the forward conduction losses of the active rectifier's diodes. Another drawback of this circuit is that the HF PWM bridge requires PWM modulated signal, which makes the transformer design less efficient.

In this paper, we propose a high efficiency and compact bidirectional HF link inverter using HF center-tapped transformer. With this topology, fewer switches are used, thus switching losses are expected to be lower. In addition we implement a modified modulation technique for the PWM bridge that allows more efficient utilisation of the transformer. It is also discovered that the proposed method results in simpler hardware implementation.



(a) Cycloconverter type HF link inverter.



(b) Dc-dc converter type HF link inverter.

Fig. 1. Bidirectional HF link inverter.

2 Proposed Circuit Description

2.1 Circuit Operation

The proposed topology for a single-phase inverter is shown in Fig. 2. Basically, there are three conversion stages. At the first stage, the HF bridge converts the dc voltage into high frequency ac voltage using PWM scheme. Then, the power is transferred to the second stage via a center-tapped HF transformer. At this stage, the HF PWM waveform will be rectified using a center-tapped active rectifier. The active rectifier enables bidirectional power flow in the case of inductive load. For transfer of power from the source, the diodes are utilised. For reverse power flow, the power switches S3 and $\overline{S3}$ are turned-on. The opening and closure of the switches are accomplished by a control signal, v_s. It must also be noted that every switch of the active rectifier requires a snubber network to reduce the high voltage spike that results from the leakage inductor of the transformer secondary. The snubber circuit is not shown in the block diagram for simplicity.

The PWM waveform is then low-pass filtered to obtain the rectified fundamental component and to remove the high order harmonics. The *LC* filter also helps to reduce the remaining spikes that are not completely clamped by the active rectifier snubbers. Finally, using a polarity-reversing bridge, the second half of the rectified sinusoidal voltage waveform is inverted at zero-crossing, and the sinusoidal output waveform is obtained. Note that the polarity-reversing bridge utilises only supply switching frequency switches.

Using this configuration, the total number of power switches is reduced into ten. From these, only six switches are switched at high frequency.

The timing diagrams for the key waveforms are illustrated in Figs. 3 and 4. The rectified sinusoidal modulating signal is compared with the triangular carrier signal to produce the switching instants of the PWM waveform, v_{pwm}. This process is done digitally using a microcontroller. Using the HF bridge, the HF PWM waveform, v_{HF} is produced at the primary side of the HF transformer. The stepped-up HF PWM voltage at the secondary side is then rectified by the active rectifier. The gate control signal of the active rectifier, v_s, shown in Fig. 4, is used to control the power flow at the active rectifier stage. The produced output voltage waveform, $v_{PWMrect}$ is filtered using a low pass *LC* filter, and the rectified sinusoidal voltage waveform is obtained. Through polarity-reversing bridge, the ac sinusoidal output waveform is obtained. The gate control signal for polarity-reversing bridge is denoted as v_u.

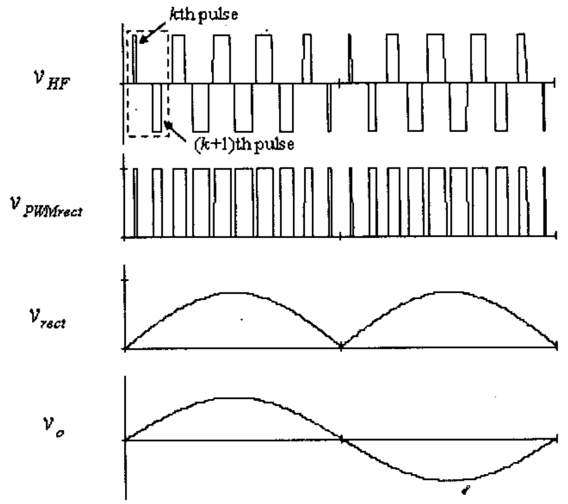


Fig. 3. Principal waveforms at different stages of the dc/ac conversion.

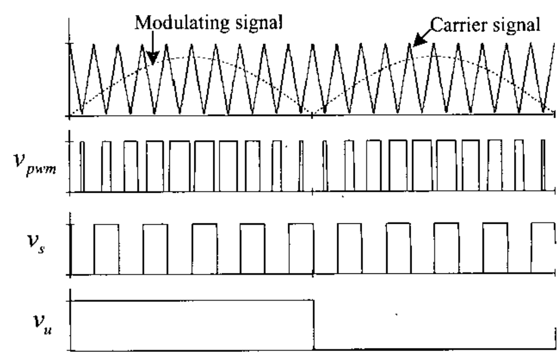


Fig. 4. Modulating technique and signal generated by microcontroller.

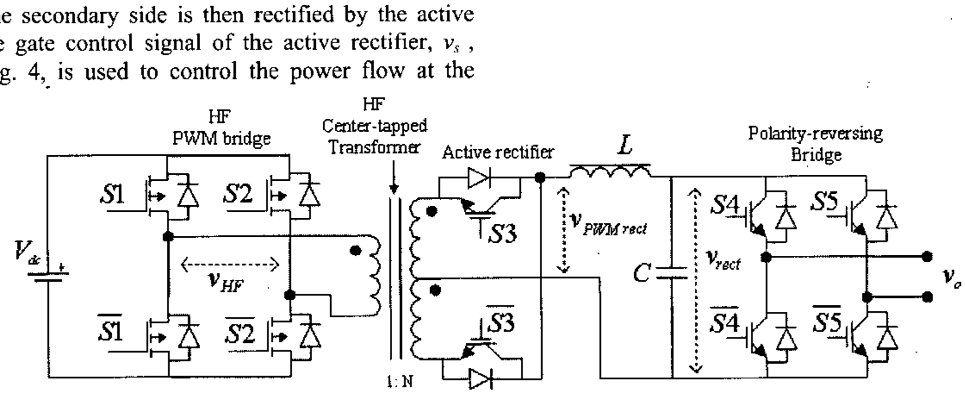


Fig. 2. Block diagram of the proposed inverter.

2.2 Digital Modulation Technique

In this work, the modulation technique of the HF bridge is based on the symmetric regular sampling sinusoidal PWM. The derivation of the switching angles is accomplished using the volt-second equalization method, as illustrated in Fig. 5. The PWM pulse width characterization is also shown in the same figure. Note that the modulating waveform is a rectified sinusoidal signal. The equation used to calculate the pulse width of the kth PWM for a given modulation index, M_I, and modulation ratio, m_f, is given as follows:

$$\delta_k = 4\delta_o M_I \sin\alpha_k \qquad (1)$$

where $k = 1\ldots\left(\frac{m_f}{2}\right)$.

Using Eqn. (1) the rising and falling edges (i.e. the switching instants) of the kth pulse can be written as:

$$\text{Rising edge,}\ \ \alpha_{1k} = \alpha_k - \delta_k \qquad (2)$$

$$\text{Falling edge,}\ \ \alpha_{2k} = \alpha_k + \delta_k \qquad (3)$$

From Fig. 3, it can be noticed that the widths for kth and $(k+1)$th pulses are not equal in v_{HF}. If the difference in the pulse widths are plotted from k=1 through m_f, it can be observed that a low frequency voltage envelope existed along with the high frequency component. This may results in transformer saturation, as the transformer is normally designed for high frequency operation. Alternatively, the transformer can be utilized below its rated capacity to avoid the possible saturation.

To overcome this problem, we propose the kth pulse width to be equalized to the $(k+1)$th. Using this approach, the use of dc blocking capacitance at primary side of transformer, as suggested in [2] can be avoided. Furthermore, the processing speed to calculate the pulse widths can be increased, with only $m_f/8$ pulses to be calculated in each cycle. The following equation is used for this purpose:

$$\delta_k = \delta_{(k+1)} = 4\delta_o M_I \sin(\alpha_k') \qquad (4)$$

where:

$$\alpha'_k = \frac{\alpha_k + \alpha_{k+1}}{2},\ k = 1, 3, 5\ldots\left(\frac{m_f}{2} - 1\right).$$

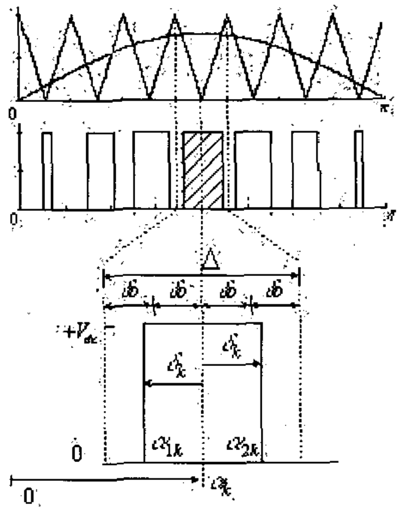


Fig. 5. Volt-second modulation technique

3 Hardware Implementation

A prototype 1 kW HF link inverter is built around the C167 (16 bit fixed-point) microcontroller. Fig. 6 shows the photograph of the finished inverter. The HF bridge is constructed using the IRFP460 power MOSFETs. The center-tapped transformer is hand-wound on the ETD59 ferrite core. The active rectifier is built using the IRG4PH40K IGBTs and 20EFT10 fast recovery diodes, with rated voltage of 1200V. In addition, RC snubber has been placed across each switch to reduce the surge voltage. The polarity-reversing bridge is constructed around the SK25GB065 IGBT module. To generate the PWM signals for the HF bridge, the PWM generator of C167 microcontroller is used. The signals generated are converted into gate drive signals using external logic gates, as shown in Fig. 7.

A dead-time compensation algorithm for the HF bridge is incorporated into the software. The waveform for the compensation is shown in Fig. 8. Note that t_d is the amount of dead-time taken away from the pulse width.

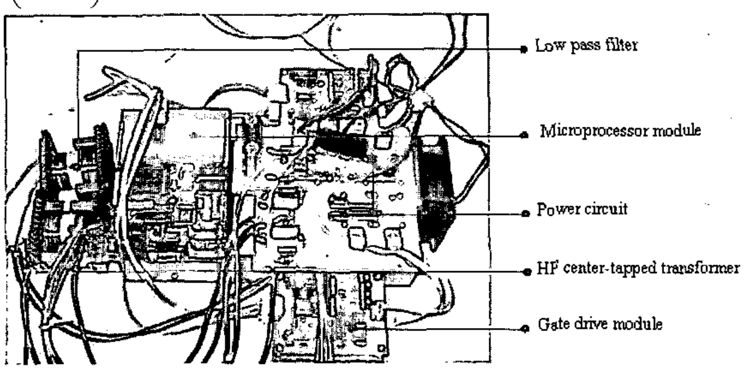


Fig. 6. Photograph of the prototype HF link inverter.

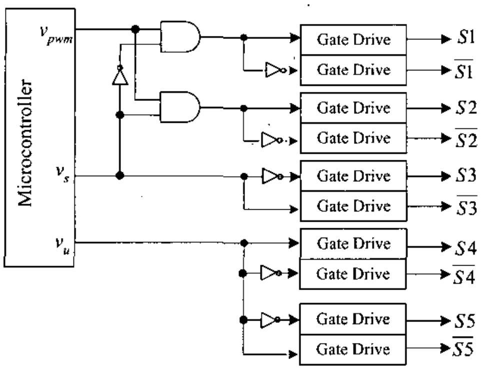


Fig. 7. Interface between the microcontroller with the power switches.

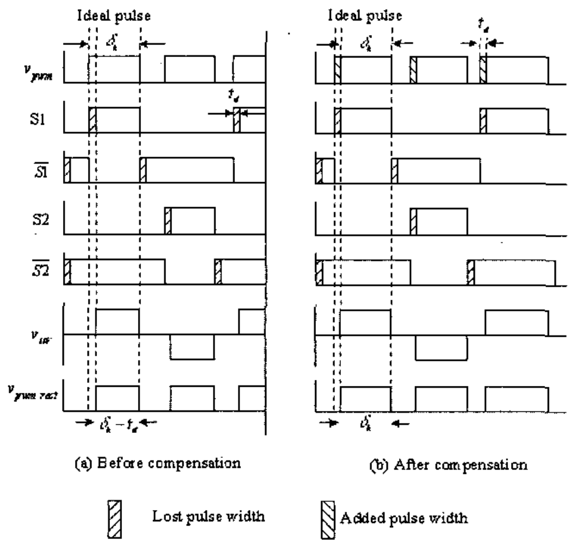


Fig. 8: Dead-time compensation scheme for the HF bridge.

4 Experimental Results and Discussion

Laboratory experiments have been carried out to verify the viability of the proposed inverter. The specifications of the inverter are as follows:

- Input voltage ranged from 130V to 150V.
- Sinusoidal output voltage 220-250 V_{rms}, 50 Hz.
- Maximum output power of 1 kW.

The practical output waveforms for resistive load and inductive load are shown in Fig. 9 and Fig. 10 respectively. From the latter, it can be observed that the inverter is capable of carrying bidirectional power flow. To measure the harmonics of the inverter output, the *LC* filter is disconnected. The frequency spectrum is shown in Fig. 11. The main harmonic components exist at and around the multiples of switching frequency, which are m_f, $2m_f$, $3m_f$ and $4m_f$. This is to be expected because the modulation technique is basically based on sinusoidal PWM.

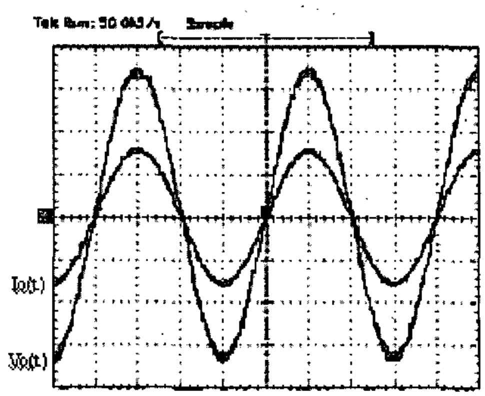


Fig. 9. Output voltage and current with resistive load. Output power = 1050W. Scales: output voltage 100V/div, output current 4A/div, time 5ms/div.

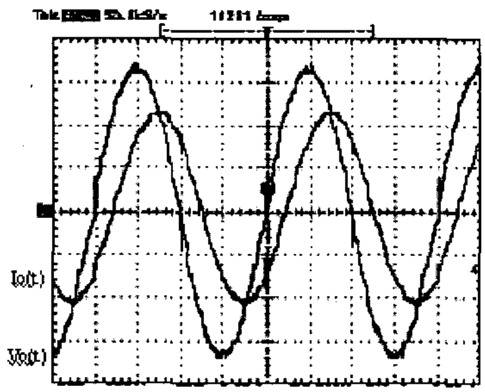


Fig. 10. Output voltage and current with inductive load. Real power = 511.7 W and power factor = 0.7. Scales: output voltage 100V/div, output current 2A/div, time 5ms/div.

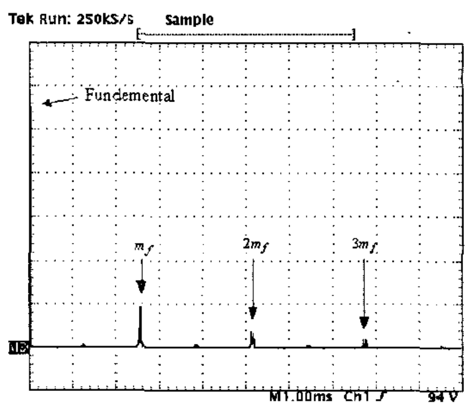
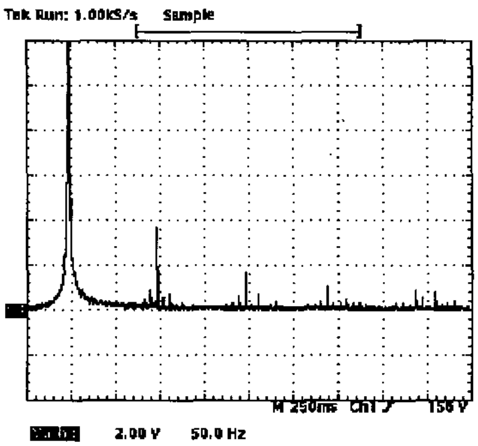
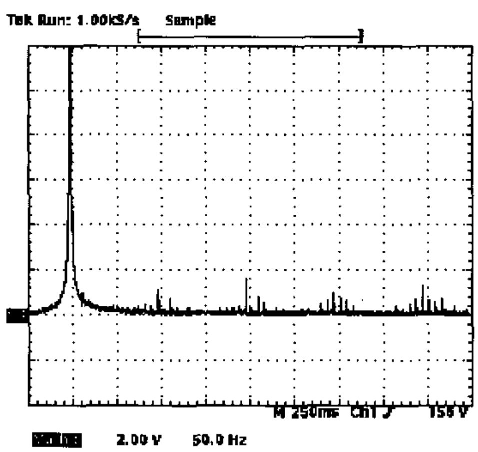


Fig. 11. Frequency spectrum of the output voltage without *LC* filter. Parameters: $M_i = 1.0$, $m_f = 650$. Scales: spectra 40V/div, frequency 12.5kHz/div.

Figs. 12(a) and (b) show the spectra of the filtered output voltage before and after dead-time compensation, respectively. The chosen dead-time to the pulse period ratio (t_d/T_s) is 0.1. As can be seen, most of the low order harmonics (3rd, 5th, etc) that result from the dead time effect is reduced. Fig. 13 indicates the effectiveness of the dead-time compensation technique employed on the inverter. Even as t_d/T_s is increased to a large value, i.e. 0.25, the compensation scheme works quite well.



(a) Output spectra before dead-time compensation.



(b) Output spectra after dead-time compensation.

Fig. 12. Frequency spectrum of the filtered output voltage before and after dead-time compensation. Scales: spectra 2V/div, frequency 50Hz/div.

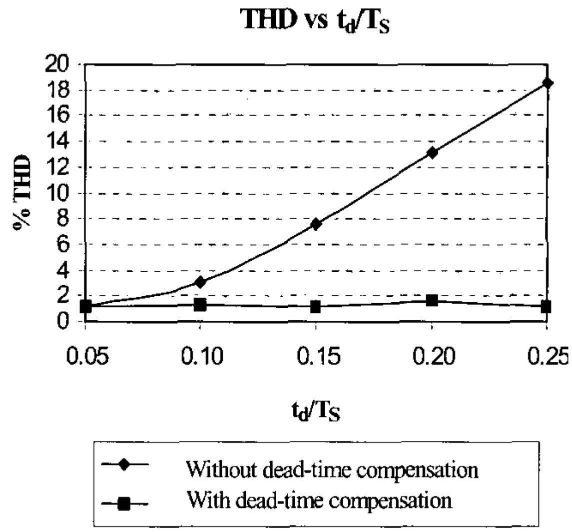


Fig. 13. Effectiveness of the dead-time compensation for various values of t_d/T_s.

The measured output voltage THD for resistive load is shown in Fig. 14. It can be seen that the output voltage THD is less than 1% over the entire output power, with the average value approximately 0.5%. This can be attributed to the effectiveness of the dead-time compensation scheme. The measured values are much less than the 5% level, the industrial standard for UPS systems [3]. The minimum value of THD (0.35%) is obtained when the inverter operates at output power 600 W – 700 W.

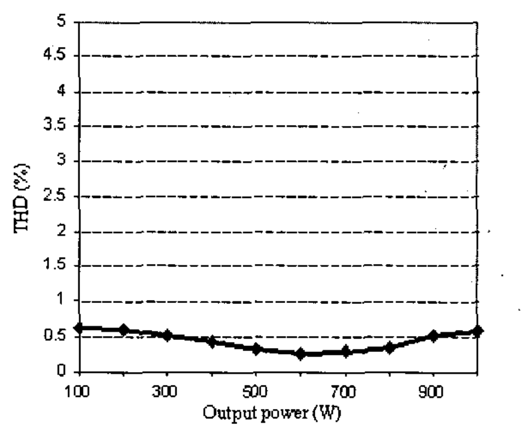


Fig. 14. Output voltage THD versus output power.

Fig. 15 shows the measured efficiency of the inverter at each conversion stages, against the output power. The average efficiency of HF bridge is 95%, while the mean efficiency of the HF transformer is 91%. The average total efficiency of the inverter is around 88%. Note that when the output power increases to 1 kW, the average efficiency decreases to the minimum level of 87%. This can be attributed to the increased losses of power switches and transformer at high current operation.

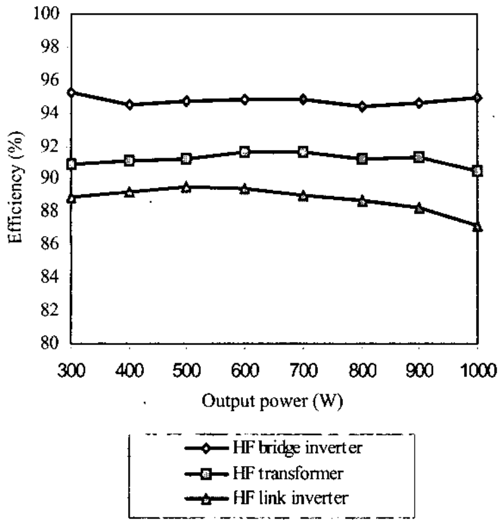


Fig. 15. Efficiency against output power at various stages of the inverter.

5 Conclusion

A compact HF link inverter that enables bidirectional power flow using center-tapped transformer has been described. The use of center-tapped active rectifier requires less power switches, thus increases the overall system efficiency. The modified digital PWM technique allows better utilisation of the transformer capacity. It also increases the switching angle calculation processing speed. A 1kW prototype is constructed to study the viability of the inverter. It was found that the output voltage has a very low THD with an average efficiency of 88%.

Acknowledgements

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References

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