PERFORMANCE EVALUATION OF FINFET SILICIDE BASED CONTACT THROUGH ELECTRICAL SIMULATION

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DEDICATION

This project report is dedicated to my lovely wife who always be there and motivated me. Not to forget to my mother who raised me up to what I am today with love and care. Also, this dissertation is also dedicated to my respected father who taught me the wisdom of life and important of living with knowledge. To my teachers and lecturer, I outcome of this report represents the continuation of your effort towards the road of knowledge contribution.

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ABSTRACT

Continues scaling of device dimension allows the complex integration of increasing number of transistors in a single chip possible. As the semiconductor industry move according to Moore's law, the scaling down of field effect transistor (FET) has reached less than 10 nm. The conventional planar FET structure can no longer withstand the short channel effect that become pronounce at ultra-narrow channel length. Therefore, alternative transistor architecture FinFET had been introduced. However, the focus to obtain minimal device leakage from this structure is still on-going due to the thin width of fin that causing an incease in parasitic resistance. In this study, silicidation will be implemented on 10nm FinFET structure and analysed through electrical simulations. The parameters studied in this research are threshold voltage (Vth), off current (Ioff), saturation current (Isat), subthreshold slope (SS) and resistance out (Rout). The silicidation process will involve using following materials which are Silicide, Cobalt Silicide, Nickel Silicide, TiSilicide and Tungsten Silicide. Results from the simulations founds that device power leakage reduced by almost 24% when implemented with Nickle Silicde layer. Futher optimization and simulations will provide insight for engineer in implementing silicidation in short channel devices.

ABSTRAK

Pengurangan saiz peranti yang berterusan membolehkan komplex integrasi bilangan transistor dalam satu cip meningkat dengan mendadak satu realiti. Dengan industry semikonduktor berkembang mengikut undang-undang Moore, pengecilan skala transistor kesan medan (FET) telah mencapai skala kurang daripada 10 nm. Struktur konvesional planar FET tidak lagi mampu menahan kesan saluran pendek yang semakin memberi impak kepada saluran transistor berskala kecil. Oleh itu, struktur alternatif seperti finFET telah diperkenalkan. Namun begitu, fokus dalam mengurangkan kebocoran arus elektrik dari struktur finFET ini masih lagi diperjuangkan. Hal ini kerana, ketebalan fin yang nipis menyumbang kepada peningkatan ketahanan parasit dalam transistor. Dalam kajian ini, process Silicidation akan dilaksanakan ke atas struktur 10nm finFET dan dianalisa melalui simulasi elektrikal. Pemerhatian pemboleh ubah dalam kajian in adalah treshold voltage (Vth), off current (Ioff), saturartion current (Isat), subthreshold voltage (SS) dan rintangan keluar (Rout). Proses Silicidation akan melibatkan penggunaan material seperti Silicide, Cobalt Silicide, Nickel Silicide, TiSilicide dan Tungsten Silicide. Hasil daripada simulasi kajian mendapati penurunan sebanyak 24% pada kebocoran kuasa pada transistor diperolehi apabila penambahan lapisan Nickle Silicide pada peranti dilakukan. Di masa kemudian, simulasi dan pengoptimuman boleh dilakukan untuk memberi wawasan data kepada jurutera dalam melaksanakan *Silicidation* dalam transistor berskala kecil.

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CHAPTER 1

INTRODUCTION

1.1 Problem Background

As the Moore's law states that the number of transistor doubles in every two years in the same chip area, the demand of scaling the size of transistor had been intensively studied to allow more transistor to be fit in a chip. There are many factors which motivate the transistor scalling in upward trend as shown in Figure 1-1. The leading player for transistor process manufacturer, Taiwan Semiconductor Manufacturing Company (TSMC) suggested that the innovation itself is one of the main factor for this upward motivation. As we progress from one technology to another, we require more transistor to fit in a single chip. For instance, for AI/5G technology would need approximately 1.2 billion of transistor to fit in one die area[1].

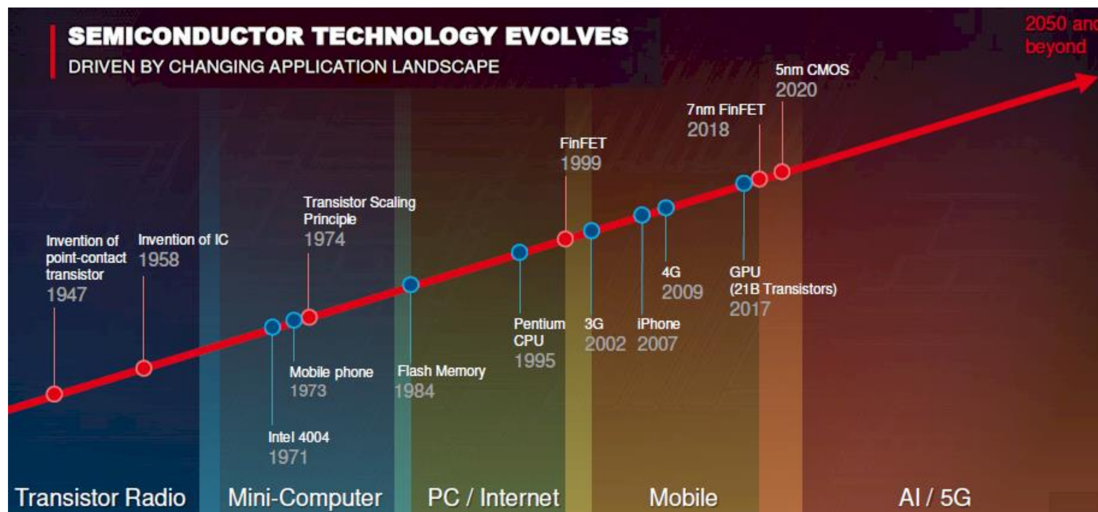

Figure 1.1 Device scalling based on TSMC Roadmap. [1]

As the scalling progress in semiconductor technology, more simulation and studies needed for more accurate system[2]. However, the device transistor starts to

experience problem commonly know as short channel issues as the technology scales as shown in Figure 1-1. For instance, drain induced barrier lowering, velocity saturation and hot carrier degradation. All these short channel effects will degrade the device performances. For instance, devices leakage issues due to short channel effect had increase the power consumption for SoC application [3] . Efforts have been made to overcome this great challenge by coming out with alternative device structure such as finFET.

FinFET, known as multi gate Metal Oxide Semiconductor Field Effect Transistor (MOSFET) as shown in Figure 1-2 (b) is an alternative structure for conventional planar FET as shown in Figure 1-2 (a). The multiple gates in finFET surrounds the thin FIN channel able to fully deplete the channel barrier. This provides better gate controllability and more current flow to reduce short channel effect. However, the device leakage issue still exists in short channel FinFET structure which mostly happen on static sub-threshold current during off state [3]. This results into higher power consumption for the device itself. To address this, the device can be fabricated on top of insulator [4] as one of the method to reduce the power consumption.

However, the power consumption are mostly happened due to high leakage subthreshold current issue which caused by high parasitic resistance of thin fin width. This high parasitic resistance needs to be overcomed to reduce the resistance value. The resistance can be reduced by implementing additional metal layer on top of source and drain contact. This has been implemented on transistor since 22nm technology process [5]. Among various extra metal implemented is silicide, which this material is favourable due to its low thermal resistivity when in contact with Silicon.

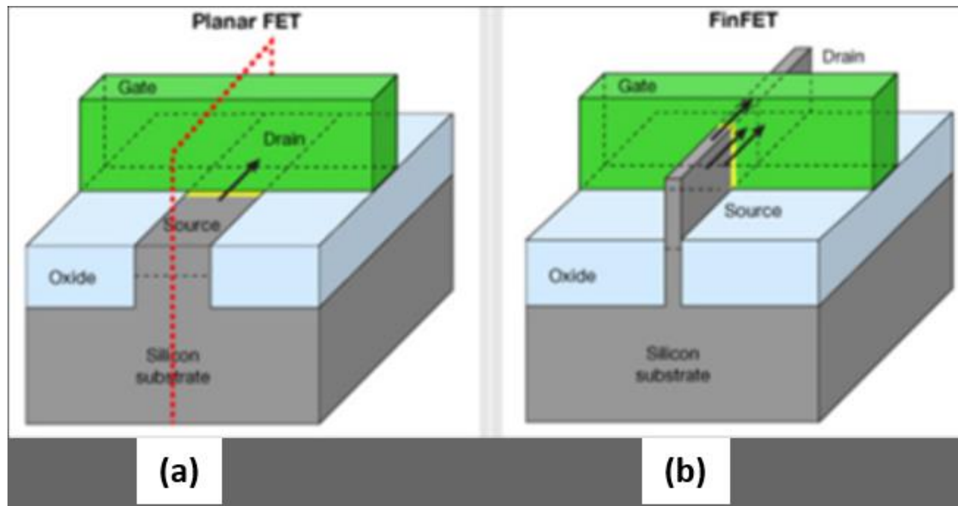

Figure 1.2 a.Planar FET cross section. b.FinFET cross section. [6]

1.2 Problem Statement

As the Moore's Law continues to ride an upward trend, the reduction of gate length follows, and device continues to loss its gate controlability. This leads to higher power consumption which happen mostly when the device is in off state. This leakage also knows as static leakage happen due to the flow of sub-threshold current (Ioff). Researches has come out with an alternative device structure such as Fin Field Effect Transistor (finFET), to overcome this issue in short channel devices.

However, as the fin width of device structure grows thinner, it has become a bottle neck for finFET structure to further improve their power performance. The parasitic resistance due to thin fin width is overcomed by adding additional metal layer on top of source and drain contact. The material used as additional layer is mainly Silicide. The method of overcoming this resistance issue is currently lacking the implementation on 10nm finFET device. Besides that, the benchmark for Silicide implementation with other doping material needed more additional work. Therefore, this research aims to investigate the performance of finFET silicide based through electrical simulations.

1.3 Research Objectives

The objectives of this project are:

a) To built 10nm FinFET structure using silicided source and drain contact using TCAD.

b) To simulate the electrical behaviour, I-V characteristics of device by varying Silicide materials in contact with source and drain.

c) To benchmark silicide material implemented on transistor that gives optimum power leakage reduction.

1.4 Research Scopes

This project focuses on the electrical properties of 10nm finFET implemented with Silicide. The research scopes of this study are listed as follows:

a) The 10nm device structure is constructed and simulated using TCAD software Sentaurus version P-2019-013-SP1 from Synopsys.

b) FinFET structure used in this research is Bulk FinFET.

c) The electrical simulation includes threshold voltage, off current, saturation current, subthreshold slope and out resistance of the device.

d) Static power leakage, off current is used as indicator for device performance.

e) Silicide materials used in this research are Silicide, Cobalt Silicide, Nickel Silicide, TiSilicide and Tungsten Silicide.

1.5 Thesis Outline

This thesis consists of five main chapters. Chapter 1 will discuss the project introduction, problem background, problem statement, research objectives, scopes, and thesis outline. The main objective of this project is to study the electrical simulation of 10nm finFET devices implemented with different Silicide contact.

In Chapter 2, the discussion and literature reviews of methods to improve device performance from previous work are discussed. Besides, this chapter will also present and discuss the similar Silicide implementation works from previous research.

In Chapter 3, the research methodology throughout the whole project is discussed. Firstly, the flowchart of the methodology used is presented and discussed. Then, the construction of 10nm FinFET bulk structure using Sentaurs TCAD is presented. Lastly, the simulation flow for this research will be inferred in this chapter as well.

The results and discussion obtained from this project are presented in Chapter 4. In this chapter, the results and findings are validated as well. Chapter 5 will conclude and states the significant of contribution from this research. This last chapter will also be listing recommendation on future works.

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