Two Stage Integrated Class-F RF Power Amplifier

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***Abstract*- A new design of an integrated two-stage class-F power amplifier (PA) for wireless application operating in the 1.65 GHz frequency range is described. The circuit utilizes a simple method to drive the output stage with a half sinusoidal waveform that is optimal for class-F operation. The circuit was fabricated in a Silterra's standard 0.18 μm RF CMOS technology. Measurement result shows a maximum power-added efficiency (PAE) of 42 % and a maximum gain of 19.7 dB. When operating from a 3V voltage supply, the PA delivers an output power of 18.9 dBm. This work demonstrates the feasibility of using class-F PAs for short-range and low-power applications.**

I. Introduction

The rapid growing of wireless communications in recent years has generated a demand for wireless systems that are low cost, power efficient, reliable and with small form-factor. The desired characteristic can potentially be obtained through integrating the whole wireless system onto a single chip utilizing CMOS technology. However, until now most PAs have been produced exclusively in GaAs due to its superior device performance. Although, there is a growing interest in utilizing CMOS technology for PAs, there are still many limitations posed by CMOS.

The continuous downscaling of CMOS into the deep sub-micron regime has made possible PA designs operating at GHz frequency. However with each scaling generation, the VDD and the transistor breakdown voltage are reduced even more, limiting the voltage headroom and the power handling capability of the PA. Therefore, for a fixed output power, higher current drive is needed in the circuit. Another major drawback for PA design in CMOS has been the lossy passive devices, especially on-chip inductors. As passive components play an important role in PA design, any parasitics associated with the passive elements have an adverse impact on the performance of the PA.

In this paper, a simple and effective method of driving the class-F PA is presented. The method is not restricted to class-F PA only and can be used in other classes of PA. A design example with measurement result is presented to show the feasibility of the method.

II. Class-F

The class-F boosts both efficiency and output power by using harmonic resonators in the output network to shape the drain waveforms such that the load appears to be a short for even harmonics and an open for odd harmonics [1]. Ideally (for a class-F PA), the transistor output voltage and current becomes a square wave and a truncated sinusoidal form, respectively. Fig. 1 presents the characteristic drain waveforms of class-F. When there is no overlapping between the drain voltage and drain current across the active device, there is zero power dissipation leading to a theoretical 100% drain efficiency.

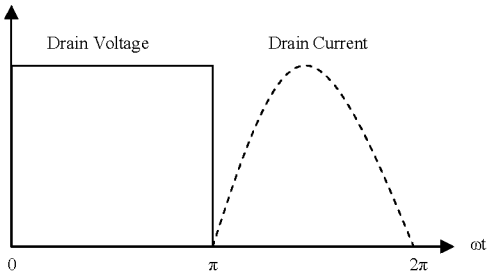

Fig. 1. Ideal Drain Waveform of Class-F

The ideal class-F assumes the inclusion of an infinite number of harmonics. In practice only a finite number of harmonics can be effectively controlled. To that end, the relevance of a suitable voltage harmonic component ratio has been stressed in the literature [2]-[4]. In particular, to increase the output power, efficiency and power gain, the optimum voltage harmonic components ratio between the fundamental and third harmonic has been demonstrated to be 1/6. The most widespread circuit

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used for this type of class-F PA is known as the third harmonic peaking circuit. It resonates on both the operating frequency and the third harmonic. The corresponding circuit is shown in Fig. 2. Theoretical design of the circuit is presented in [5], while the component values in the load network are derived and shown in Table I.

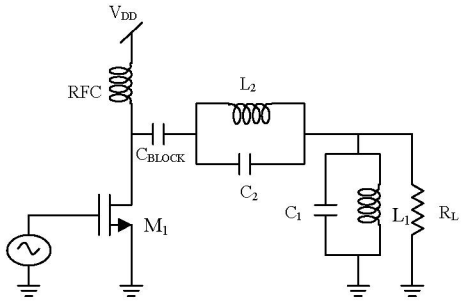

Fig. 2. Third Harmonic Peaking Class-F Circuit

TABLE I
CLASS-F POWER AMPLIFIER COMPONENT VALUE

Component	Parameter
C_1	$1/(R_L*BW)$
L_1	$1/(\omega^2*C_1)$
C_2	$0.50625*C_1$
L_2	$1/(9\omega^2*C_2)$
C_{BLOCK}	$8*C_2$

Generally, harmonics come from the nonlinear behavior of the transistor. By biasing the transistor with different conduction angle, different sets of harmonics appear at the output [6]. Since the third harmonic is critical for flattening the voltage waveform, the transistor is usually biased for more than half of the conduction angle (class-AB biasing) where the third harmonic is in opposite phase to the fundamental component.

III. BASIC OPERATION AND DESIGN IMPLEMENTATION

The circuit consists of two stages, a class-F output stage and a pre-driver stage. Most PA pre-drivers are based on inductor tuning [7]. However, this circuit is troublesome for high efficiency (reduced conduction angle) operation. Using this circuit, the amplitude of the sinusoidal has to be large, resulting in negative voltage swing at the input of the output stage. The negative voltage can potentially forward bias the drain junction diode in addition to increasing the peak voltage at the gate oxide making the breakdown voltage problem worse.

A half-sinusoidal driver would solve these problems. Fig. 3 shows the circuit configuration of the half-sinusoidal driver and its steady-state operation. The inductor L_1 constantly carries current into the circuit. The transistor M_1 acts as a switch. When the switch is on, current will flow into M_1 causing the voltage at V_D to remain at zero. When the switch is off, the current will start to charge capacitor C_1 and thus producing a half-sinusoidal waveform.

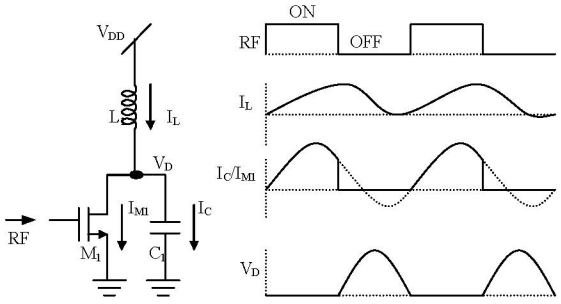

Fig. 3. Half-Sinusoidal Driver and its Steady-State Operation

In this design, the non-linear output capacitance of the transistor M_1, in addition to the gate capacitance of the transistor at the output stage, is high enough to be used as C_1 instead of a MIM-capacitor. The circuit is designed to have an optimum load of 50 Ω to avoid the use of an impedance transformation network which greatly degrades the efficiency of the PA.

IV. MEASUREMENT RESULTS

The circuit was fabricated in Silterra's standard 6-metal layer, 0.18μm RF CMOS technology. Fig. 4 shows a micrograph of the fabricated circuit. All major interconnections and inductors were laid out using the top metal layer to minimize the parasitic effects. The large transistors were divided into multiple cells, which have several fingers to reduce parastitic elements at the drain and gate. The Agilent E8267D PSG Vector signal generator was used to provide the RF input and the output was measured using Agilent E4440A PSA spectrum analyzer.

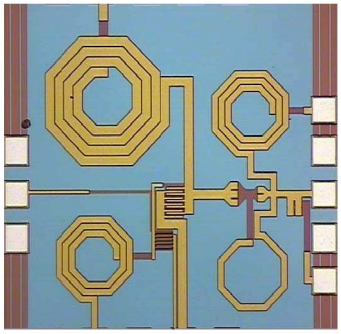

Fig. 4. Micrograph of the Fabricated Power Amplifier

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Fig. 5 shows the output power and PAE of the class-F PA at 1.65 GHz, as a function of the supply voltage. The PAE was calculated at a constant input signal of 2 dBm with supply voltage varied between 1.2 and 3 V. The circuit was not designed to operate above 3.3 V as the transistor will suffer from gate oxide breakdown.

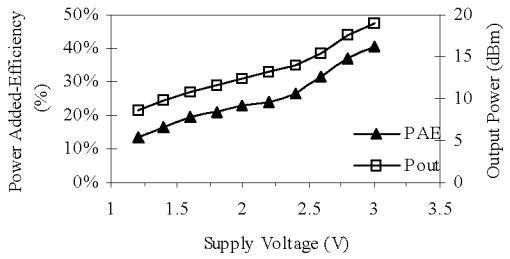

Fig. 5. Measured Output Power and PAE at 1.65GHz as a function of the supply voltage

The output power increases as the supply voltage increases since it is proportional to the square of the supply voltage. The PAE follows almost the same trend as the output power since both output power and DC power consumed from the supply increase together.

Fig. 6 and Fig. 7 show the PAE, Power Gain and output power respectively as a function of the input power at 1.65 GHz. PAE of the PA reaches saturation after 2 dBm. Highest PAE recorded by this PA stands at 42%. Power gain of the PA is consistent around 19 dB before it starts to drop off at the 1-dB compression point. Operating at the highest supply voltage, the 1-dB compression point for the PA is at –5 dBm. Having a low compression point is desirable in non-linear PAs like class-F since more harmonics will appear at the output of the transistor.

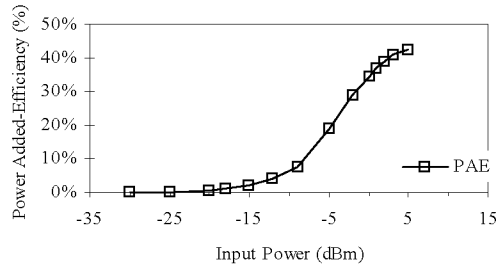

Fig. 6. Measured PAE at highest supply voltage as a function of input power at 1.65 GHz

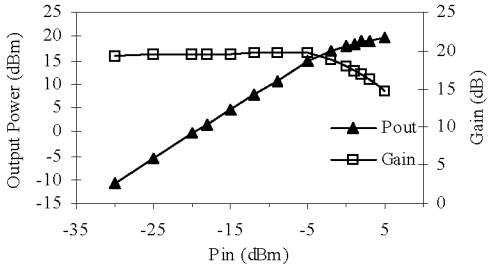

Fig. 7. Measured output power and power gain at highest supply voltage as a function of the input power at 1.65 GHz

V. Conclusion

A fully integrated 1.65 GHz class-F PA using a half-sinusoidal driver has been designed, fabricated and measured. The circuit can achieve output power of 18.9 dBm and PAE of 42 %.

Acknowledgment

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