IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received April 21, 2021, accepted May 3, 2021, date of publication May 6, 2021, date of current version May 17, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3077968

Asymmetrical 17-Level Inverter Topology With Reduced Total Standing Voltage and Device Count

M. SAAD BIN ARIF[1,2], (Member, IEEE), UVAIS MUSTAFA[1], SHAHRIN BIN MD AYOB[2], (Senior Member, IEEE), JOSE RODRIGUEZ[3], (Life Fellow, IEEE), ABDUL NADEEM[1], AND MOHAMED ABDELRAHEM[4,5], (Member, IEEE)

[1]Department of Electrical Engineering, Zakir Husain College of Engineering and Technology, Aligarh Muslim University, Aligarh 202002, India
[2]Power Engineering Department, School of Electrical Engineering, Universiti Teknologi Malaysia (UTM), Johor 81310, Malaysia
[3]Department of Engineering Sciences, Universidad Andres Bello, Santiago 8370146, Chile
[4]Chair of Electrical Drive Systems and Power Electronics (EAL), Technische Universität München, 80333 München, Germany
[5]Electrical Engineering Department, Faculty of Engineering, Assiut University, Assiut 71516, Egypt

Corresponding authors: Mohamed Abdelrahem (mohamed.abdelrahem@tum.de; mohamed.abdelrahem@aun.edu.eg) and Shahrin Bin Md Ayob (shahrin@fke.utm.my)

The work of Jose Rodriguez was supported by Agencia Nacional de Investigación y Desarrollo (ANID) under Project FB0008, Project ACT192013, and Project 1210208.

ABSTRACT Voltage source Multilevel Inverters (MLIs) are vital components for medium voltage and high-power applications due to their advantages like modularity and better power quality. However, the number of components used is significant. In this paper, an improved asymmetrical multilevel inverter topology is proposed producing 17-levels output voltage utilizing two dc sources. The circuit is developed to reduce the number of isolated dc-sources used without reducing output levels. The circuit utilizes six two-quadrant switches, three four-quadrant switches and four capacitors. The capacitors are self-balancing and do not require extra attention, i.e. the control system is simple for the proposed MLI. Detailed analysis of the topology under linear and non-linear loading conditions is carried out. Comparison with other similar topologies shows that the proposed topology is superior in device count, power quality, Total Standing Voltage (TSV), and cost factor. The performance of the topology is validated for different load conditions through MATLAB/Simulink environment and the prototype developed in the laboratory. Furthermore, thermal analysis of the circuit is done, and the losses are calculated via PLECS software. The topology offers a total harmonic distortion (THD) of 4.79% in the output voltage, with all the lower order harmonics being less than 5% complying with the IEEE standards.

INDEX TERMS Asymmetrical converters, multilevel inverter (MLI), reduced device count, total standing voltage (TSV), nearest level control (NLC).

I. INTRODUCTION

Multilevel Inverters (MLIs) are becoming very important for medium voltage high power applications day by day due to several advantages like improved power quality, lower switching stress, modularity of structures, no EMI, etc., [1]–[3]. The three basic topologies for the MLIs are Flying Capacitor (FC) MLIs, Neutral Point Clamped (NPC) MLIs, and Cascaded H-Bridge (CHB) MLIs. These were termed Conventional topologies. The main disadvantages of these topologies were the large number of devices incorporated and the complexity in the control of capacitors voltages [4]. Researchers have been looking for various topologies to remove these demerits [5]–[7]. Since the MLI produces stepped output, various dc sources/links are required, which are switched on in a predefined manner with semiconductor devices like IGBTs, MOSFETs, etc. Having a higher number of dc links ensures better waveforms of the output voltage and current. However, having a higher number of dc sources is a disadvantage as it increases complexity and cost to the system [8]. Capacitors can be employed to increase the dc links with a reduced number of dc sources, but this requires careful consideration. The capacitor may require extra effort to keep their voltages balanced [9]. Another method is to choose the magnitude of the dc sources in a specific ratio to maximize the number of levels. These are called asymmetric inverters [10].

Various topologies considering the above facts are available in the literature. Manjrekar *et al.* [11], [12] proposed an asymmetric configuration for the CHB inverters by

The associate editor coordinating the review of this manuscript and approving it for publication was Zhilei Yao.

choosing the magnitude of dc sources in a binary manner, thus increased the output voltage levels dramatically while keeping the number of devices the same. Another work is proposed in [13], where the author used several capacitors to increase the dc links. The main disadvantage of this work was that the capacitors required a complex control algorithm. In [14], the authors were concerned about reducing the voltage stress on the switches and producing a higher number of levels with fewer switches. The authors of [15] proposed another topology that offered lower switching stress and a higher number of levels, but the capacitors required extra attention by complex control. The topology in [16] had self-balancing capacitors, but the number of switches was high. In [17] though the topology offers high output voltage levels, it required an H-Bridge for polarity generation, thus necessitating higher rating switches.

In [18], a new topology comprised of three dc sources and eight switches is proposed. This topology can be used as symmetric or asymmetric. The topology offered 9-level output for symmetrical operation, while for asymmetrical operation where V_1:V_2:V_3 = 3:1:1, it offered 13-level output. In [19], a 17-level topology is proposed, but it requires four dc sources, four capacitors, and 16 switches. Thus the component count is too high. In [20], a new 17-level topology is proposed. The presented topology utilizes 12 switches, but the number of dc sources are four. Whereas in [21], another interesting topology producing 17-level output voltage is shown. The topology utilized 12 IGBTs (10 switches) and required 10 driver circuits, but the number of dc sources are still high, i.e. four.

Moreover, 17-level topologies are proposed in [22], [23], in both the topologies, four dc sources were utilized. Furthermore, in [23], the proposed MLI required 16 IGBTs and 14 driver circuits, which is relatively high. Apart from the above works, there are other improved recently proposed MLI topologies. Some of the notable works include [24]–[26]. The main limitations include higher device count or higher TSV. Device count can be reduced by asymmetrical configuration, but that increases the voltage stress on switches and, in turn, the TSV. Another attempt to increase the level generated with a low device count is made in [35]. A switched capacitor is used to boost the output. Therefore, there is a trade-off between the asymmetric configuration and the feasibility of the topology

The authors of this work proposed an improved topology capable of producing 17-output levels while utilizing a reduced number of dc sources and switches. The proposed circuit is developed to reduce the number of isolated dc-sources used without reducing output levels. This is one of the main contributions of the proposed topology. The authors employ two dc sources and have added self-balancing dc-link capacitors to generate a 17-level output voltage. The capacitors are self-balancing; thus, no other complex control algorithm is required for voltage balancing. Moreover, the proposed topology offers significantly less Total Standing Voltage (TSV), making it a feasible option in high voltage

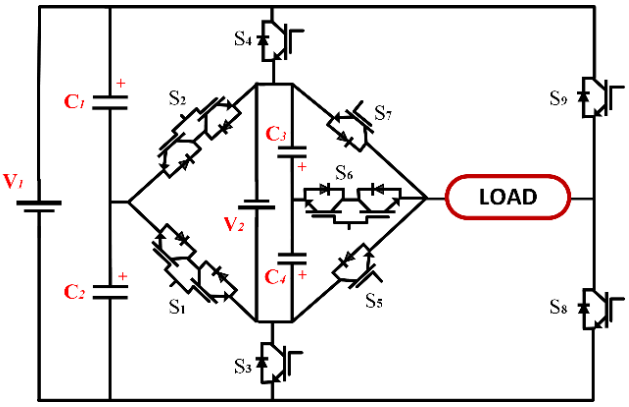


FIGURE 1. Circuit diagram of the proposed 17-Levels MLI topology.

applications. Thus, the contribution of this work can be summarised in the following points:

(a) The proposed topology utilizes only two DC sources and nine switches (12 IGBTs) for producing 17 levels of output voltage.
(b) Although the number of bidirectional switches is increased in the proposed topology, it offers a better N_L/N_{sw} ratio than the other compared topologies.
(c) The proposed topology utilizes dc-link capacitors, which are self-balancing; thus, no extra complex algorithm is required.
(d) The proposed topology has low TSV [p.u] than the other 17-level topologies, making it a viable option.

The paper's structure is as follows: the next section will discuss the circuit configuration, its working modes, and the Total Standing Voltage calculation. Extension of the proposed topology and its generalized equations were presented in section II. In sections III and IV, simulation analysis followed by hardware validation is discussed. The power loss analysis and the comparative analysis is presented in sections V and VI. Finally, the conclusion of the work is delivered in section VII.

II. PROPOSED CIRCUIT DESCRIPTION

The proposed topology is shown in Fig. 1. It consists of two dc sources and nine switches. Six switches are unidirectional, while the other three are bidirectional switches. It is capable of generating 17-level output voltage by utilizing two self-balancing capacitors across each dc source. The two dc sources are in the proportion of V_1:V_2 = 3 : 1. The capacitor provides a way to break each source's DC voltage into two equal magnitudes with bidirectional switches. The switches (S1, S3), (S2, S4), (S3, S4), (S5, S7), and (S8, S9) pairs should not conduct at the same time to prevent shoot-through fault. Table 1 shows the switching configuration and corresponding voltage level of the proposed MLI topology.

During the positive half cycle of output voltage with input voltage (V_1=6V, V_2=2V), where V is the voltage across the dc-link capacitor), voltage levels 0V, 1V, 2V, 3V, 4V, 5V, 6V, 7V, 8V are generated by modes 1, 2, 3, 4, 5, 6, 7, 8, 9 respectively. During mode 1, S4, S7, S9 switches are ON,

TABLE 1. Modes and switching scheme for one complete cycle.

MODE	Status of Switches									V_o
	S1	S2	S3	S4	S5	S6	S7	S8	S9	
1	0	0	0	1	0	0	1	0	1	0V
2	0	0	0	1	0	1	0	0	1	1V
3	0	0	0	1	1	0	0	0	1	2V
4	0	1	0	0	0	0	1	1	0	3V
5	0	1	0	0	0	1	0	1	0	4V
6	0	1	0	0	1	0	0	1	0	5V
7	0	0	0	1	0	0	1	1	0	6V
8	0	0	0	1	0	1	0	1	0	7V
9	0	0	0	1	1	0	0	1	0	8V
10	0	0	1	0	1	0	0	1	0	0V
11	0	0	1	0	0	1	0	1	0	-1V
12	0	0	1	0	0	0	1	1	0	-2V
13	1	0	0	0	1	0	0	0	1	-3V
14	1	0	0	0	0	1	0	0	1	-4V
15	1	0	0	0	0	0	1	0	1	-5V
16	0	0	1	0	1	0	0	0	1	-6V
17	0	0	1	0	0	1	0	0	1	-7V
18	0	0	1	0	0	0	1	0	1	-8V

and S1, S2, S3, S5, S6, S8 switches are OFF. It generates output voltage level 0 V. On mode 2, S4, S6, S9 switches are ON, and S1, S2, S3, S5, S7, S8 switches are OFF. During this mode, the circuit generates output voltage level 1V and so on. Similarly, during the negative half cycle, voltage levels 0V, −1V, −2V,−3V, −4V, −5V, −6V, −7V and −8V are generated by modes 10, 11, 12, 13, 14, 15, 16, 17 and 18 respectively. Fig. 2 shows the circuit configuration and current flow path during different modes of operation.

A. TOTAL STANDING VOLTAGE CALCULATION

The cost of the inverter indirectly controls the rating of switches. Lowering the switches' rating less costly will be the switches, which is only feasible if the voltage to be blocked by the switch is not high. The voltage stress on different switches should be determined. The amount of voltage stress on all switches can be referred to as Total standing voltage (TSV). An indication of switch rating in topology is a lower estimate of TSV. For the above topology and considering the voltage ratio of the DC sources, i.e. V1:V2 = 3:1, different switches experience different peak withstanding voltage which can be categorized as follows:

$$\text{Category 1: } V_{S1} = V_{S2} = 2(V_1/2 + V_2) = 5V_d$$
$$\text{Category 2: } V_{S3} = V_{S4} = V_1 + V_2 = 4V_d$$
$$\text{Category 3: } V_{S5} = V_{S7} = V_2 = V_d$$
$$\text{Category 4: } V_{S6} = 2(V_2/2) = V_d$$
$$\text{Category 5: } V_{S8} = V_{S9} = V_1 = 3V_d$$

Total Standing Voltage (TSV) can be obtained as [24]:

$$\begin{aligned} \text{TSV} &= V_{S1} + V_{S2} + V_{S3} + V_{S4} + V_{S5} + V_{S6} \\ &\quad + V_{S7} + V_{S8} + V_{S9} \\ &= 5V_d + 5V_d + 4V_d + 4V_d + V_d + V_d \\ &\quad + V_d + 3V_d + 3V_d \\ \text{or, TSV} &= 27V_d \end{aligned} \tag{1}$$

Sometimes, per-unit TSV, which is the ratio of TSV and the maximum output voltage, is also calculated. In this case,

Per Unit TSV, TSV (pu) = TSV/(Peak Output Voltage)

$$= 27V_d/8V_d = 3.375 \text{ pu} \tag{2}$$

Fig. 3 depicts the stress distribution of the different Switches used in the proposed inverter topology.

B. CAPACITOR SIZING AND INRUSH CURRENT

The size of the capacitor is an important factor in determining the feasibility of the converter. The capacitor size depends upon the energy required to handle by the capacitor in one cycle. Considering Fig. 7(c), it can be seen that the maximum discharging period of each capacitor is the same. Also, it is noticed that during half cycle, one of the capacitors pair is charged, and another pair is discharged. This process reverses for the rest of the half-cycle. Thus, the capacitance of the capacitors is the same. Considering the Capacitor C_1, it is discharged for the interval [π-2π]. During this period, the change in charge of capacitor C1 is depicted as below:

$$\Delta Q_1 = \int_{\pi}^{2\pi} \frac{i_L}{\omega} d(\omega t) \tag{3}$$

where i_L is the load current. For a resistive load of R, the charge ripple becomes,

$$\Delta Q_1 = \frac{8v_d}{2\pi f_s R}(2\pi - \pi) = \frac{4v_d}{f_s R} \tag{4}$$

where f_s is the switching frequency, R is the resistive load applied, and Vd is the voltage step chosen so as $8v_d$ represent the peak output voltage. For capacitor C_1, the maximum voltage ripple can be calculated by equation (5), and the optimum size of the capacitor is calculated using (6). Similarly, the capacitor size is calculated for the rest of the capacitors.

$$\Delta V_{rip} = \frac{4v_d}{f_s R C_1} \tag{5}$$

$$opt.C_1 = \frac{4v_d}{f_s R \Delta V_{rip}} \tag{6}$$

For every cycle, each of the capacitors is charged and discharged. The inrush current can cause the breaking of switches involved in its path if it is not controlled and appropriately analyzed. The inrush current mainly depends on the maximum voltage difference between the capacitor voltage and the source providing the charge and various circuit parameters involved in the charging loop. The peak value of charging current ($I_{charging\_max}$) is related to the maximum voltage difference, ΔV_{max}, as follows [32]:

$$I_{charging\_max} \approx \frac{\Delta V_{max}}{r_p} \tag{7}$$

where r_p is the total parasitic resistance of all the charging loop components, this maximum inrush charging current can be handled by inserting a small inductance L_r in the charging loop. L_r can be modelled based on the maximum inrush

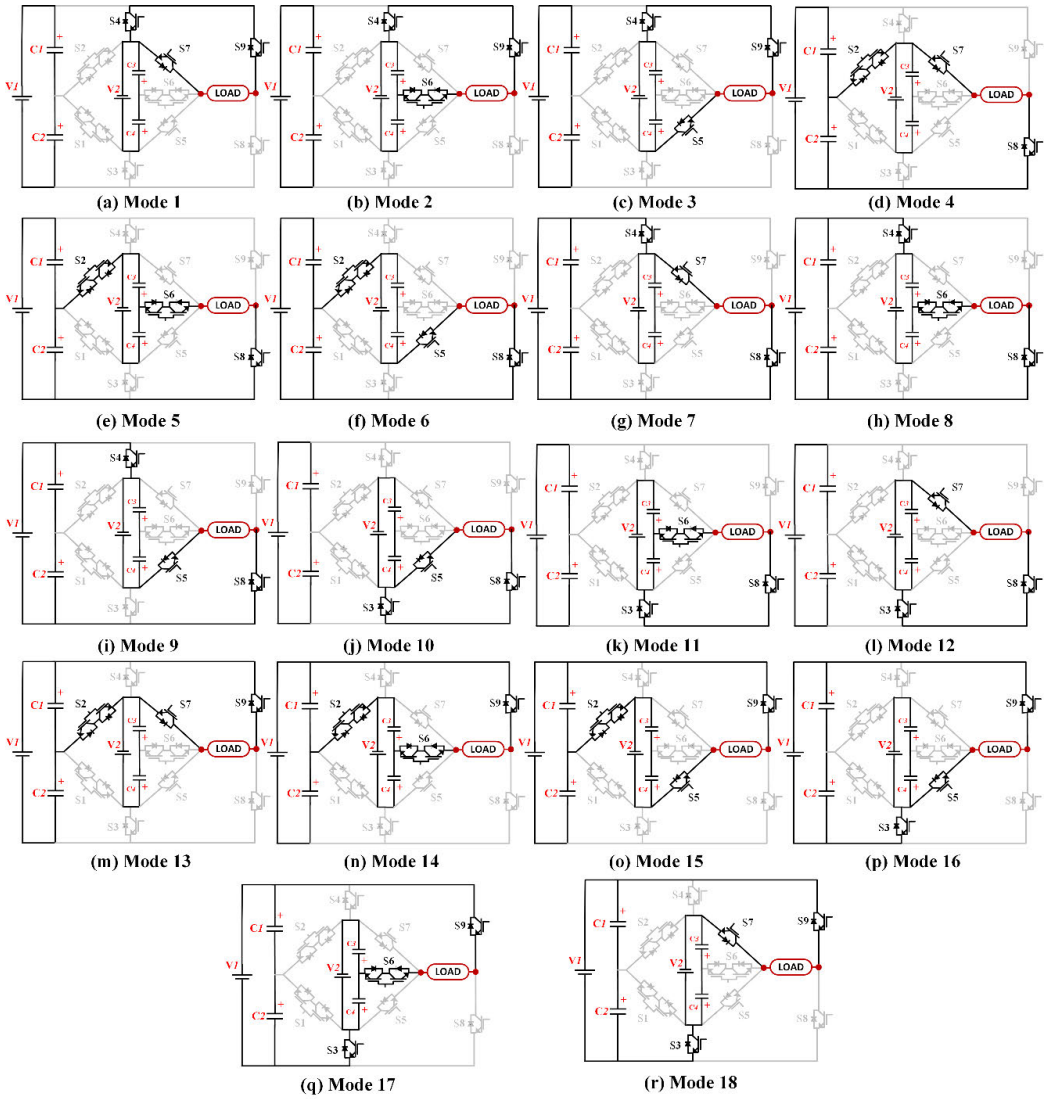


FIGURE 2. Circuit configuration of the proposed topology during different modes of operation in one complete cycle.

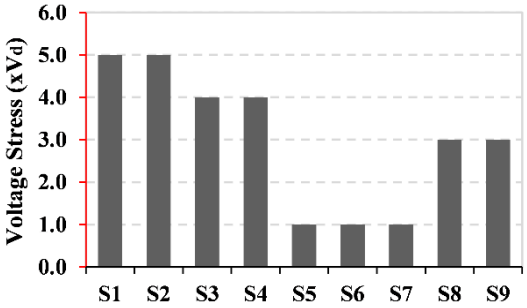
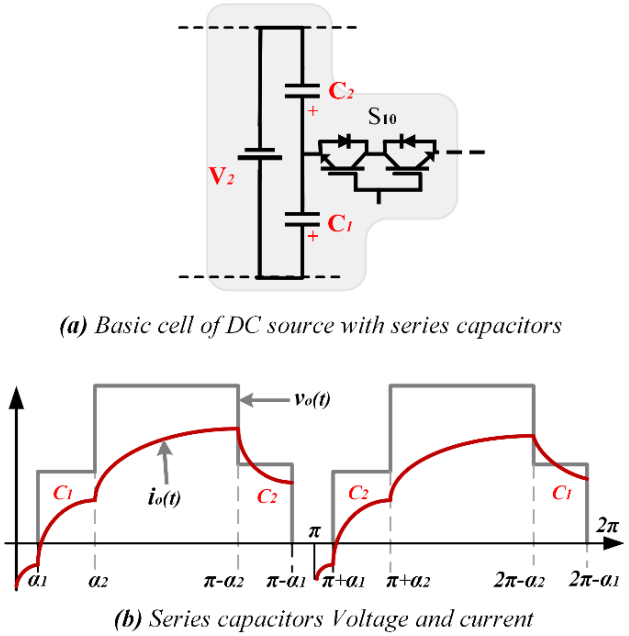


FIGURE 3. Voltage stress distribution of switches.

charging current. It acts as a short circuit during the steady-state operation, and during the transients, it protects against the maximum charging current. It reduces the peak of inrush charging current and provides di/dt protection. To avoid any negative impact, the value of this inductance is kept reasonably small and set below 1μH.

C. CAPACITOR CHARGE BALANCING

The self-balancing nature of two series capacitors connected across a DC source, shown in Fig. 4(a), depends upon the average power dissipated and absorbed by the capacitors during one complete cycle. It can be calculated as in [28], [32]. The typical current and voltage waveforms for these series capacitors are depicted in Fig. 4(b). The figure shows that the voltage and current waveform follow the same path for the interval [0-π] and the [π-2π]. The current-voltage for [α_1-α_2] and [(π + α_1) - (π + α_2)] are precisely similar. Thus, the area under the curve, i.e. power, remain the same. During half-cycle, one capacitor is charged while the other is utilized, and during the next half-cycle, the other capacitor is utilized. This is also evident from obtained results



(a) Basic cell of DC source with series capacitors

(b) Series capacitors Voltage and current

FIGURE 4. Self balancing of series capacitors.

shown in Fig 7(c) for the proposed topology. In light of the above discussion and Fig. 4, the following equations can be materialized:

$$\int_{\alpha_1}^{\alpha_2} [i_o(t)v_o(t).d\omega t = \int_{\pi+\alpha_1}^{\pi+\alpha_2} [i_o\,(t)\,.v_o\,(t)\,.d\omega t] \quad (8)$$

And,

$$\int_{\pi-\alpha_2}^{\pi-\alpha_1} [i_o(t)v_o(t).d\omega t] = \int_{2\pi-\alpha_2}^{2\pi-\alpha_1} [i_o(t).v_o(t).d\omega t] \quad (9)$$

For the above equations, it should be noted that v_o and i_o represent the voltage and current waveform corresponding to the cell shown in Fig. 4 (a) only and does not mean the output voltage and current of the converter. Thus, the average power during the various intervals remains the same and maintaining the voltage across the capacitors. During the interval [(π-α_1)-π], the current falls to zero as, during this interval, the capacitors are cut off from the current path. This describes the voltage balancing for the series capacitors with a DC source acting independently.

D. COST ANALYSIS OF THE CIRCUIT

The cost function of a topology approximates its implementation feasibility. It depends upon various factors like the number of semiconductors used (N_{IGBT}), number of DC sources utilized (N_{DC}), number of driver circuits utilized (N_{Dr}), number of capacitors used ($N_{cap.}$), number of diodes used (N_d) and the TSV_{pu}. The cost function can be calculated as follows [25]:

$$CF = N_{IGBT} + N_{DC} + N_{cap} + N_{Dr} + N_d + \alpha TSV_{pu} \quad (10)$$

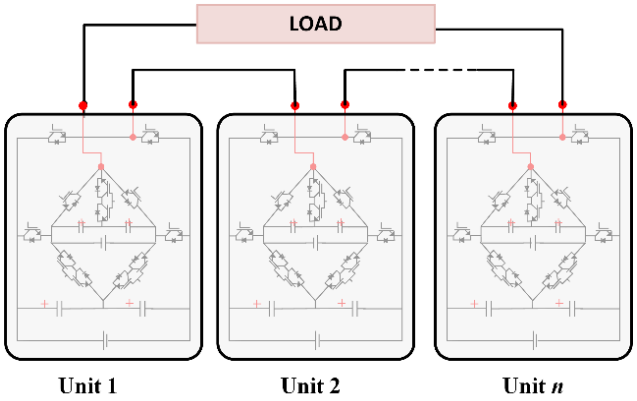


FIGURE 5. Cascaded structure of the topology.

Where α is the weighting coefficient for the TSV. Since the proposed topology lacks any diode, N_d can be ignored, and the cost factor, CF, can be calculated as:

$$CF = N_{IGBT} + N_{DC} + N_{cap} + N_{Dr} + \alpha TSV_{pu} \quad (11)$$

α can be selected greater than unity when more importance is required for the TSV. For moderate attention to TSV, it is chosen as between 0 and unity. For the former, α is selected as 1.5, and for the latter case, it is chosen 0.5.

For, $\alpha = 1.5$,

$$CF = 12+2+4+9+(1.5 \times 3.375) = 32.06$$
$$CF/Level = 32.06/17 = 1.88 \quad (12)$$

For, $\alpha = 0.5$,

$$CF = 12+2+4+9+(0.5 \times 3.375) = 28.69$$
$$CF/Level = 28.69/17 = 1.69 \quad (13)$$

E. CASCADED STRUCTURE

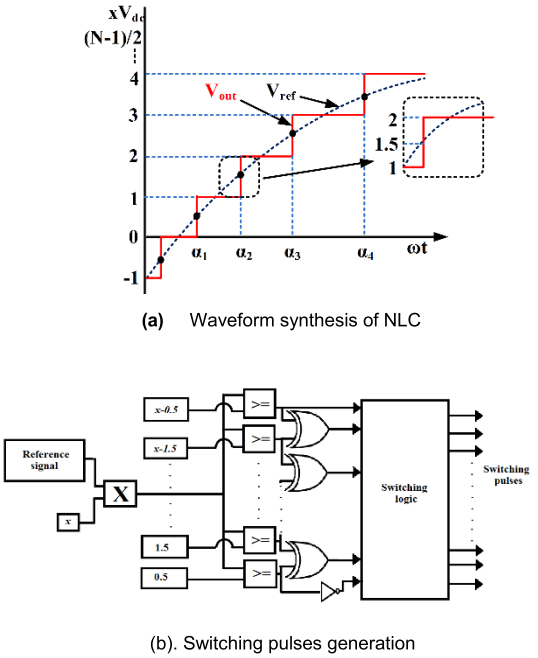
The basic unit of the proposed topology can be easily cascaded, as shown in Fig. 5. The generalized structure of the proposed topology is extended by using n-series connected basic units. The optimal generalized structures of proposed topology, regarding several factors such as number of switches (N_{sw}), number of dc sources (N_{dc}), number of capacitors (N_{cap}), number of gate driver circuit (N_{gd}) and total standing voltage (TSV) on the switches are also obtained and formulated. Formulated expressions based on the number of levels generated (N_L) are given below:

$$N_{dc} = (N_L - 1)/8 \quad (14)$$
$$N_{sw} = 3(N_L - 1)/4 \quad (15)$$
$$N_{cap} = (N_L - 1)/4 \quad (16)$$
$$N_{gd} = 9(N_L - 1)/16 \quad (17)$$
$$TSV = (N_L - 1)/30 \quad (18)$$

III. SIMULATION ANALYSIS AND DISCUSSION

The Above topology is designed and simulated in the Matlab/Simulink environment and checked for both linear and

non-linear load. For linear load, the circuit performance is analyzed for static and dynamic conditions. The value of the dc sources in simulation analysis is taken as 100V and 300V. IGBTs were used as switches. Although there are many different switching techniques available in the literature for switching and control due to the ease of implementation, Nearest Level control (NLC) is used in this work. Fig. 6 depicts the realization of the NLC algorithm as well as the switching strategy [27]. In the following section, analysis under different loading conditions and results obtained were presented and discussed in detail.



(a) Waveform synthesis of NLC

(b). Switching pulses generation

FIGURE 6. Switching pulses generation implementing NLC algorithm.

A. FIXED LOADING CONDITION

Under fixed loading conditions, constant R and RL load is considered. This kind of load can be found for household applications like heating elements, which emulate constant and varying R and RL loads. Using a fixed resistive load of R=100Ω, the obtained output voltage and current waveforms are shown in Fig. 7(a). By using a constant RL load of Z=100Ω+80mH, the obtained output voltage and current waveforms are shown in Fig. 7(b). By FFT analysis, it is reported that the THD of the output voltage is 4.83%. In both cases, the lower order harmonics are less than 5%.

B. CAPACITOR CHARGING AND DISCHARGING

The proposed topology consists of four DC link capacitors, two for each dc source. C_1, C_2 are connected in series across V_1, and C_3, C_4 are connected across V_2. To maintain equal charging and discharging times, the capacitors C_1 and C_2 are of equivalent capacitance. The same is true for C_3 and C_4. Fig. 7(c) shows the voltage across each capacitor during one complete cycle. The voltages across C_1 and C_2 are complementary to each other. If one is charging, the other is discharging, but the net energy transfer in one complete cycle across both the capacitors is zero; thus, capacitors are self-balancing. The same is true for the C_3 and C_4.

C. VARYING R AND RL LOAD

In real applications, the dynamic change in load condition is a widespread phenomenon. The dynamic load can either be a change in the R-type of load or RL-type of load. For example, heating loads such as heating furnaces and heating element used for room heating can be treated as R loads. Temperature change requires a change in R of the heating element. Thus, the heaters of the household can act as an R-type load of varying nature. The sudden change of load can occur in case of fault. Varying RL load can also be emulated during speed control of the motor. Therefore it becomes necessary to validate the performance of the proposed inverter topology for such type of dynamic loading conditions. The performance is assessed by the load's variation from the no-load condition to the gradual increment. This checks the stability of the topology in case of a sudden change of load. Fig. 8(a) and 8(b) depict the output voltage and current waveforms for the sudden change in R and RL load conditions, respectively. It can be seen in both cases that the voltage remains the same, and only the current waveform is changed as the load is changed. The transition in the current waveform is also smooth, as can be seen.

D. VARYING MODULATION INDEX

Fig. 8(c) shows the effect on voltage waveform due to the modulation index's variation from M=1 to 0.8 and then to 0.6. Decreasing the modulation index reduces the generated output voltage levels. As the modulation index reduced from 1 to 0.8, the output voltage levels also decreased from 17 to 13 and then finally reach 11 levels as the modulation index is further reduced to 0.6. This condition simulate a sudden fault in the control circuitry and check the dynamic stability of the circuit.

E. NON-LINEAR LOAD

In many applications, the inverter is required to feed non-linear loads such as variable speed control drives, rectifiers, computers, SMPS, etc. Unlike linear load, the current drawn by the non-linear load is non-sinusoidal. And the voltage and current don't follow proportional relation. Therefore it is vital to validate the performance of the inverter under non-linear loading condition. In this section, the performance of the inverter is evaluated considering two different non-linear loading conditions. First, the load is taken as a simple switched resistive load and is realized by a resistive impedance (R=100 ohm) connected in series with an AC phase controller (Triac). The second load considered is a variable speed control drives load and is realized as an inductive impedance (RL=100ohm+80mH) connected in series with an AC phase controller (Triac). Voltage and

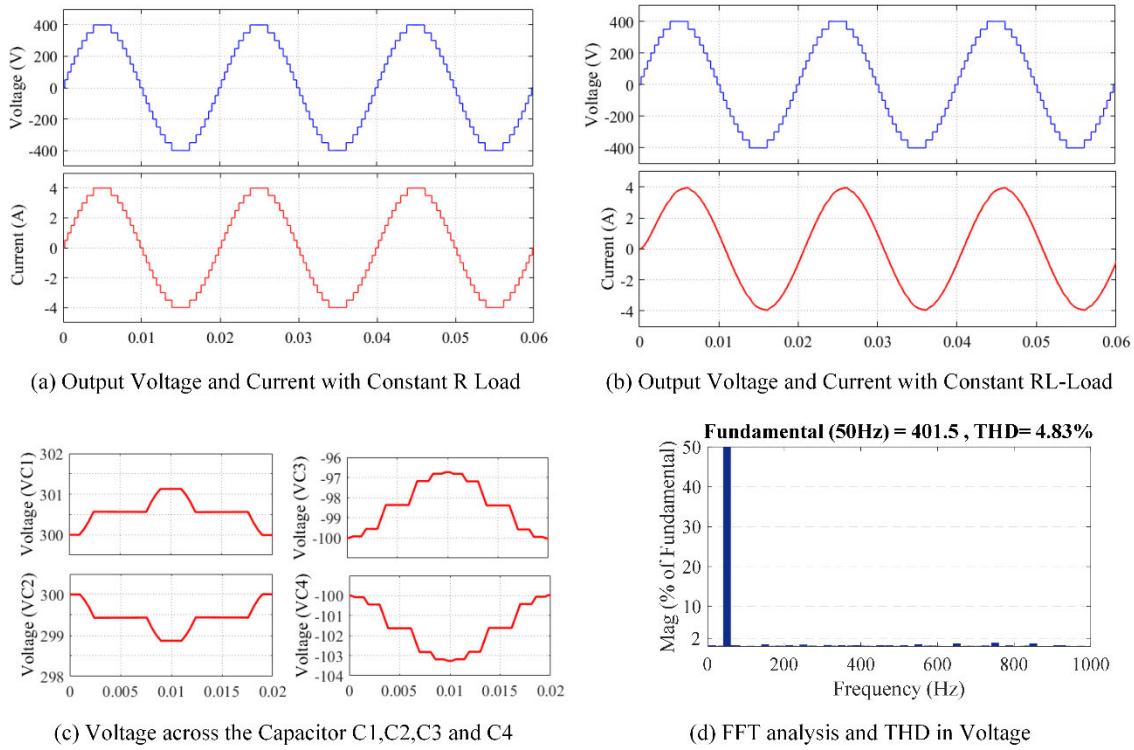


FIGURE 7. Simulation results obtained for the proposed topology with constant R and RL load condition.

current waveforms for both the loading conditions are shown in Fig. 9. The analysis validates the performance and proper operation of the proposed topology with linear and non-linear loading conditions.

IV. HARDWARE IMPLEMENTATION

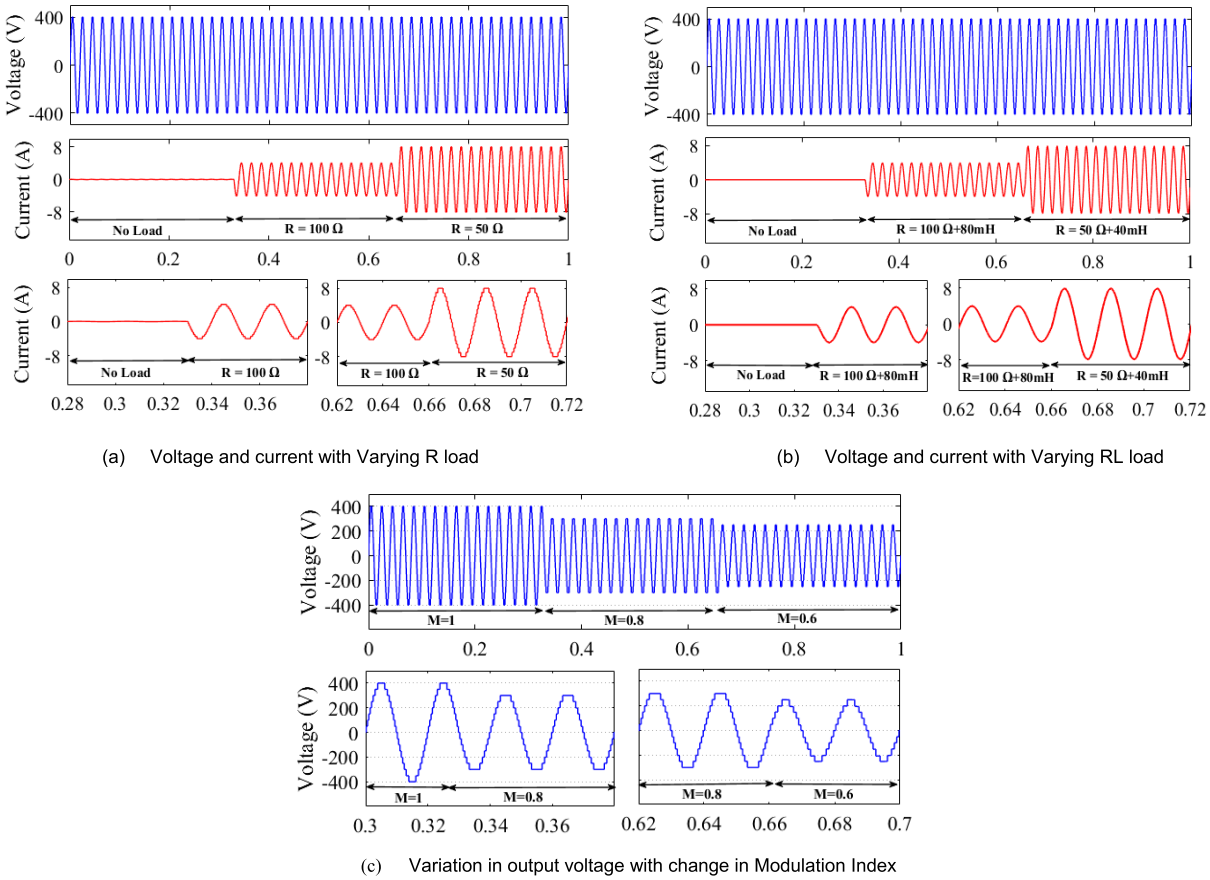
For hardware validation, a prototype of the proposed circuit is prepared in the laboratory environment. IGBTs model FGA25N120 are used as switches in the proposed circuit. The control signals are generated by using the DSP board TMS320F28379D microcontroller. For driving the IGBTs a driver circuit, TLP 250H based is utilized. Regulated dc power supplies, Scientech 4180, having a maximum channel voltage rating of 30V (individual channel) and 60V (channel in series), are used as dc sources. For the experimental validation of the circuit, the magnitude of the dc sources V1 and V2 are set to 45V and 15V, respectively. Resistive load of 50 Ω and an inductive load of 50 Ω+60mH are taken as fixed load. Load specifications for varying load and modulation index conditions are specified in Fig. 8. Different voltage and current waveforms are recorded using Yokogawa DL 1640 digital oscilloscope. The hardware setup prepared in the laboratory is shown in Fig. 10.

Fig. 11 presents the results obtained through the hardware analysis of the proposed topology. The output voltage and current waveforms for the pure R load of 50Ω are shown in Fig. 11(a). It can be seen that all the levels are stable and precise. Also, it is noticed that the current and voltage are in phase. Fig. 11(b) depicts the trace for static RL load. An inductive RL load of 50Ω+60mH is connected, and the current and voltage waveforms are traced. The current lags behind the voltage waveform due to the inductive effect. In Fig. 11(c) and 11(d), the load is changed from no-load to 80Ω and from 120Ω to 60Ω, respectively. The current remains in phase with the voltage waveform, but the magnitude is increased, as evident from the figures. Fig. 11(e) and 11(f) depict the effect of changing the modulation index on the output voltage. The modulation index is changed from 1 to 0.8 and from 0.8 to 0.6. As a result, the levels in the output waveform are reduced from 17 to 13 to 11 levels. Thus, the hardware results validate the performance and implementation feasibility of the proposed circuit.

V. POWER LOSS ANALYSIS

The loss calculation for a converter is a crucial criterion for evaluating the converter's performance as it directly affects the converter's efficiency. There are mainly two types of losses associated with a converter, conduction losses and switching losses. Conduction losses are associated with the conduction current, i(t) and turn on resistance RT and RD where T and D represent Transistor and Diode. Since a switch is a combination of Transistor with antiparallel diode, both are considered to calculate losses. Thus, both the losses can be estimated as below [28], [32]:

$$p_{c,T}(t) = \left[V_T + R_T i^{\beta}(t)\right] i(t) \tag{19}$$

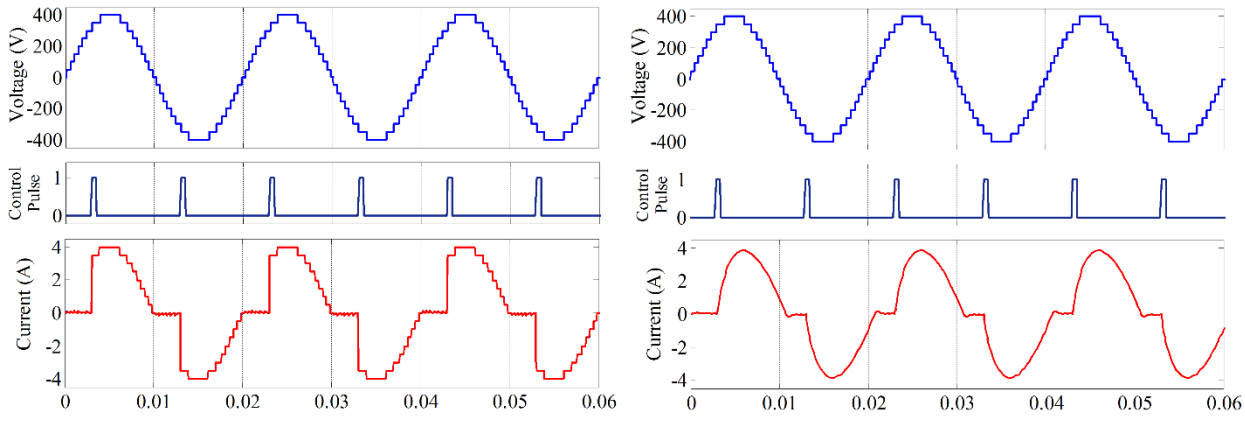


(a) Voltage and current with Varying R load

(b) Voltage and current with Varying RL load

(c) Variation in output voltage with change in Modulation Index

FIGURE 8. Simulation results obtained with changing load and modulation index.



(a) Output Voltage and Current with Non-Linear R Load

(b) Output Voltage and Current with Non-Linear RL-Load

FIGURE 9. Simulation results obtained with non-linear load.

$$p_{c,D}(t) = \left[V_D + R_D i^{\beta}(t)\right] i(t) \tag{20}$$

where β is a constant related to the Transistor specifications and can be noted from the Datasheet, the total conduction losses of a switch are the sum of the two equations above. The average conduction loss of a converter depends upon the number of transistors and diodes conducting instantly. Considering N_T transistors and N_D diodes are conducting at an instant t, then the average conduction loss will be

$$P_c = \frac{1}{2\pi}\int_0^{2\pi} [N_T(t)p_{c,T}(t) + N_D(t)p_{c,D}(t)]dt \tag{21}$$

The switching losses comprise turn-off losses and turn-on losses and depend on the energy dissipated during each

TABLE 2. Comparison of proposed topology with other seventeen level topologies.

Topology [Ref]	N_{dc}	N_v	N_{IGBT}	N_L/N_{IGBT}	N_{Dr}	$N_{cap.}$	$TSV_{p.u.}$	$MBV_{p.u.}$	CF/Level	
									$\alpha = 1.5$	$\alpha = 0.5$
[19]	4	2	16	1.06	14	4	2.75	1.00	4.02	3.38
[20]	4	2	12	1.42	09	0	6.00	1.00	2.00	1.66
[21]	4	2	12	1.42	10	0	5.50	1.67	2.01	1.70
[22]	4	2	10	1.70	08	0	6.00	1.00	1.82	1.47
[29]	4	2	10	1.70	10	0	4.50	1.00	1.81	1.54
[30]	6	1	14	0.93	14	0	2.00	0.50	2.84	2.40
[31]	4	2	10	1.70	10	0	4.00	0.75	1.77	1.53
[14]	2	2	18	0.94	14	4	6.00	1.00	5.52	4.82
[P]	**2**	**2**	**12**	**1.42**	**09**	**4**	**3.375**	**0.625**	**1.88**	**1.69**

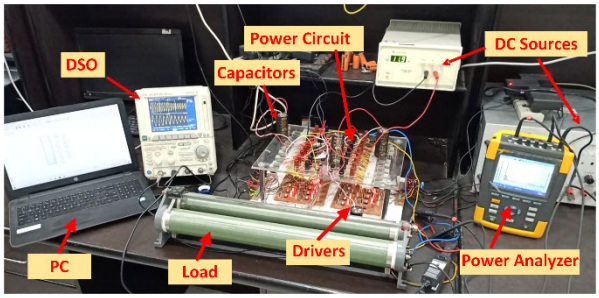


FIGURE 10. Photograph of the hardware setup in the laboratory.

process. These can be calculated as below:

$$E_{off,k} = \int_0^{t_{off}} v(t)\, i(t)\, dt = \int_0^{t_{off}} \left[\left(\frac{V_{sw,k}}{t_{off}} t \right) \left(-\frac{I}{t_{off}} (t - t_{off}) \right) \right] dt = \frac{1}{6} V_{sw,k} I t_{off} \quad (22)$$

Similarly,

$$E_{on,k} = \int_0^{t_{on}} v(t)\, i(t)\, dt = \int_0^{t_{on}} \left[\left(\frac{V_{sw,k}}{t_{on}} t \right) \left(-\frac{I'}{t_{on}} (t - t_{on}) \right) \right] dt = \frac{1}{6} V_{sw,k} I' t_{on} \quad (23)$$

where $E_{off,k}$ and $E_{on,k}$ are the energy loss during the turn-off and turn-on period of the kth switch. And t_{off} and t_{on} is the turn-off and turn-on time while t is the period, I is the current through the switch just before turning off, and I' is the current through the switch just after turning it on, $V_{sw,k}$ is the voltage of the switch after it is turned off. The power loss due to switching transitions in one complete cycle can be written as:

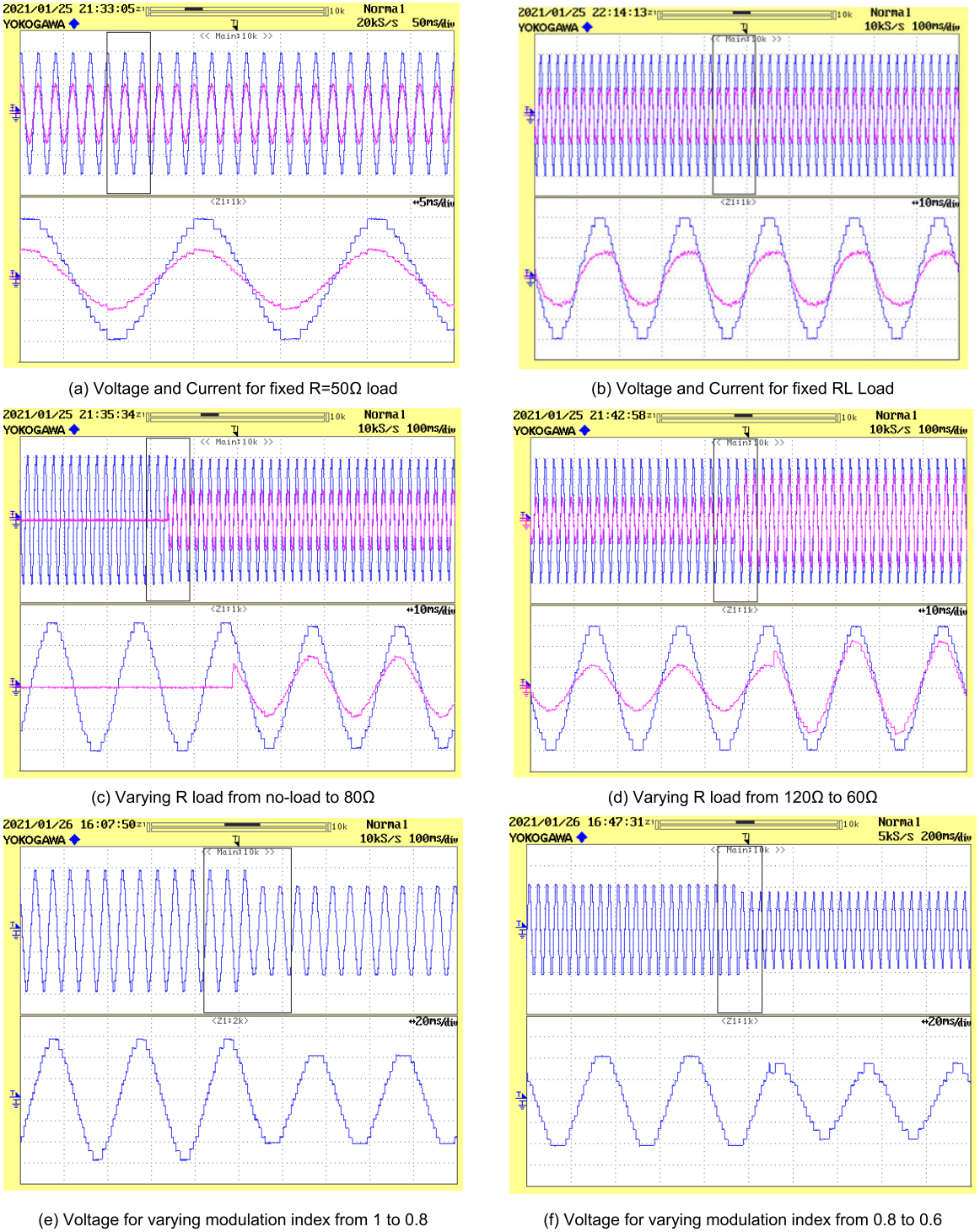
$$P_{sw} = f \sum_{k=1}^{N_{switch}} \left(\sum_{i=0}^{N_{on,k}} E_{on,ki} + \sum_{i=0}^{N_{off,k}} E_{off,ki} \right) \quad (24)$$

where f is the fundamental frequency, $N_{on,k}$ and $N_{off,k}$ are the number of times k^{th} switch turn on or turn off in one fundamental cycle. Finally, total losses are given as:

$$P_{totalloss} = P_c + P_{sw} \quad (25)$$

The above equations are simulated to calculate the losses and, in turn, the efficiency of the circuit through thermal modelling using PLECS software. Conduction losses and switching losses are calculated for different loads shown in Fig. 12(a) and 12(b), respectively. Three different power rating loads are considered for the analysis as Z1=200W (400Ω), Z2=500W (150Ω+70mH), and Z3=1kW (60Ω+100mH). The switching losses are smaller than the conduction losses due to the low switching frequency. Efficiency and total power for three different loads are calculated and are shown in Fig. 12(c) and 12(d). The inverter's efficiency with the change in rated output power is analyzed and shown in Fig. 13. Maximum efficiency of 99.37% is obtained at 200W load, and a slight decrease in efficiency is noted with the increase in output power.

The current stress and temperature profile of the switches used in the proposed topology are shown in Fig. 14. Both the parameter is very much helpful in selecting proper rating switches for different application. The temperature profiles are obtained by thermal analysis of the proposed circuit. Fig. 14(a) presents the temperature profiles of all the switches when the inverter is feeding a 1kW output load. To further enhance the selection criterion of the IGBTs,



(a) Voltage and Current for fixed R=50Ω load

(b) Voltage and Current for fixed RL Load

(c) Varying R load from no-load to 80Ω

(d) Varying R load from 120Ω to 60Ω

(e) Voltage for varying modulation index from 1 to 0.8

(f) Voltage for varying modulation index from 0.8 to 0.6

FIGURE 11. **Hardware results with different load and varying modulation index conditions.**

Fig. 14(b) depicts the current stress of different switches utilized.

VI. DISCUSSION AND COMPARATIVE ANALYSIS

The above simulation and hardware results confirm the static as well as dynamic response of the proposed circuit. It performs reliably in sudden load change or load power factor change with no spike or latching of any kind. Moreover, the capacitors are self-balancing, thus reduced the complexity of balancing. The loss analysis shows that for $Z_3 = 1$kW, the circuit has the highest power losses due to the high conduction current. The claim of better performance of

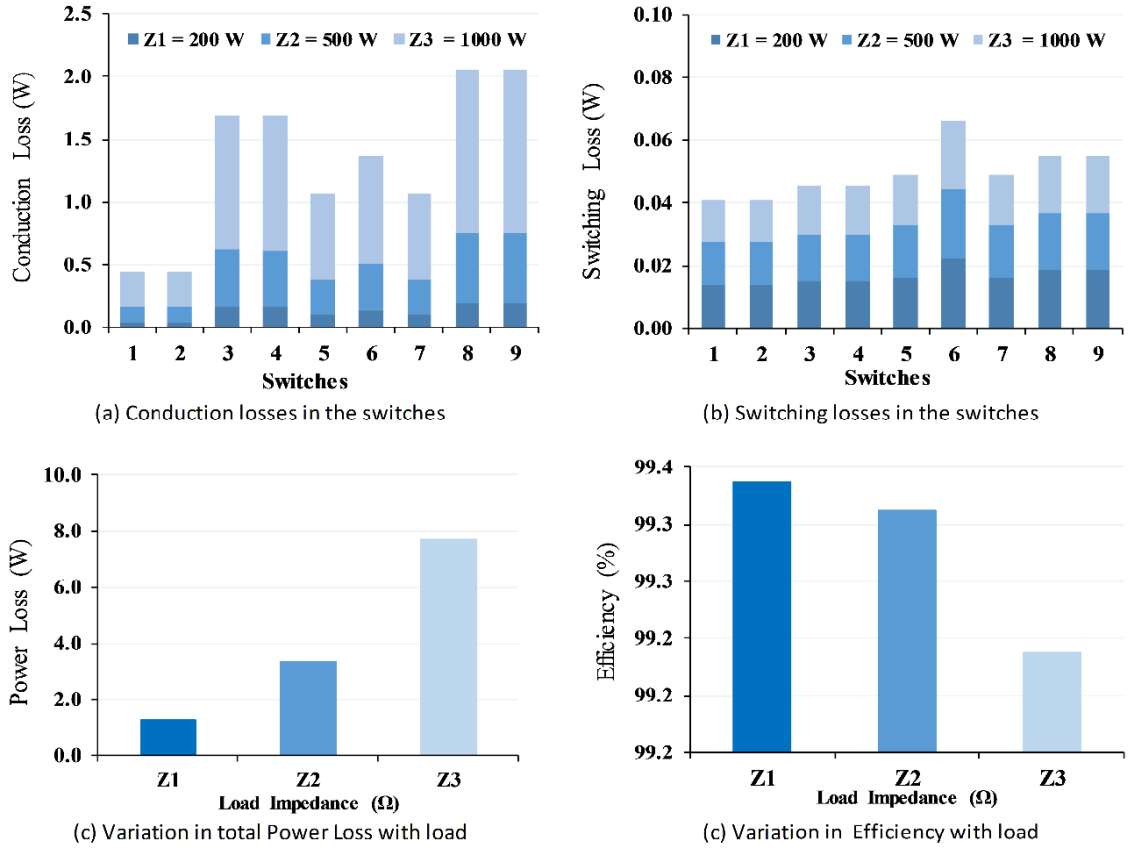


FIGURE 12. Power losses and efficiency of the proposed inverter topology with different loading conditions.

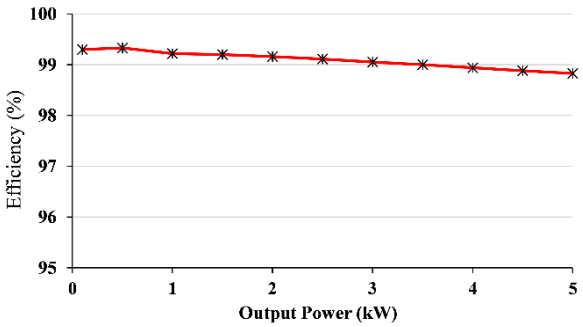


FIGURE 13. Variation in efficiency and output power.

the proposed topology is further validated by comparing it with other seventeen-level topologies present in the literature. Comparison in terms of different parameters with other topologies has been carried out, and the results obtained from the analysis are tabulated in Table 2.

The parameters taken for the comparison are the Number of IGBT used (N_{IGBT}), Number of DC sources used (N_{dc}), Number of Gate Drivers (N_{Dr}), number of capacitors used ($N_{cap.}$), Cost factors per level and per unit TSV are compared. Since the topologies compared have different IGBT (N_{IGBT}), N_L/N_{IGBT} ratio is used. Variety of DC sources (N_v) and Maximum Blocking Voltage per unit ($MBV_{p.u.}$) are also compared to present a fair and extensive comparison. Gate drivers add to the cost, so they are also used in the comparison. Finally, TSV is an essential aspect of the topology as it helps in deciding the switch ratings. Higher the switch rating, more would be its cost, so the TSV is also used to compare.

The proposed topology utilizes 12 IGBTs. Although the topologies in [22], [29], [31] use a lower number of IGBTs and driver circuits than the proposed circuit, the $TSV_{p.u}$ is significantly higher than the $TSV_{p.u}$ of the proposed MLI. Also, the MBVp.u. of the proposed topology is lower. The topology in [19] has the lowest TSV pu of 2.75 only, but it utilizes 4 DC sources and 16 IGBTs to produce the 17 level output. Though with a slight change in the DC source magnitude, it can produce 49 level output with the same IGBTs. The MLI in [30] has the best performance in terms of TSV and MBV p.u. but it utilizes 14 IGBTs, and its cost factor per level is higher. The MLI in [31] has the best Cost Factor per level among all the topologies present in the comparison, but it has higher TSV and MBV p.u. Though it is not very high, the proposed topology has lower TSV and MBV while having a comparable Cost Factor per level.

From the analysis, it can be said that the proposed topology offers a better trade-off between all the parameters. This asserts the implementation feasibility of the proposed circuit. The above discussion asserts the advantages of the proposed

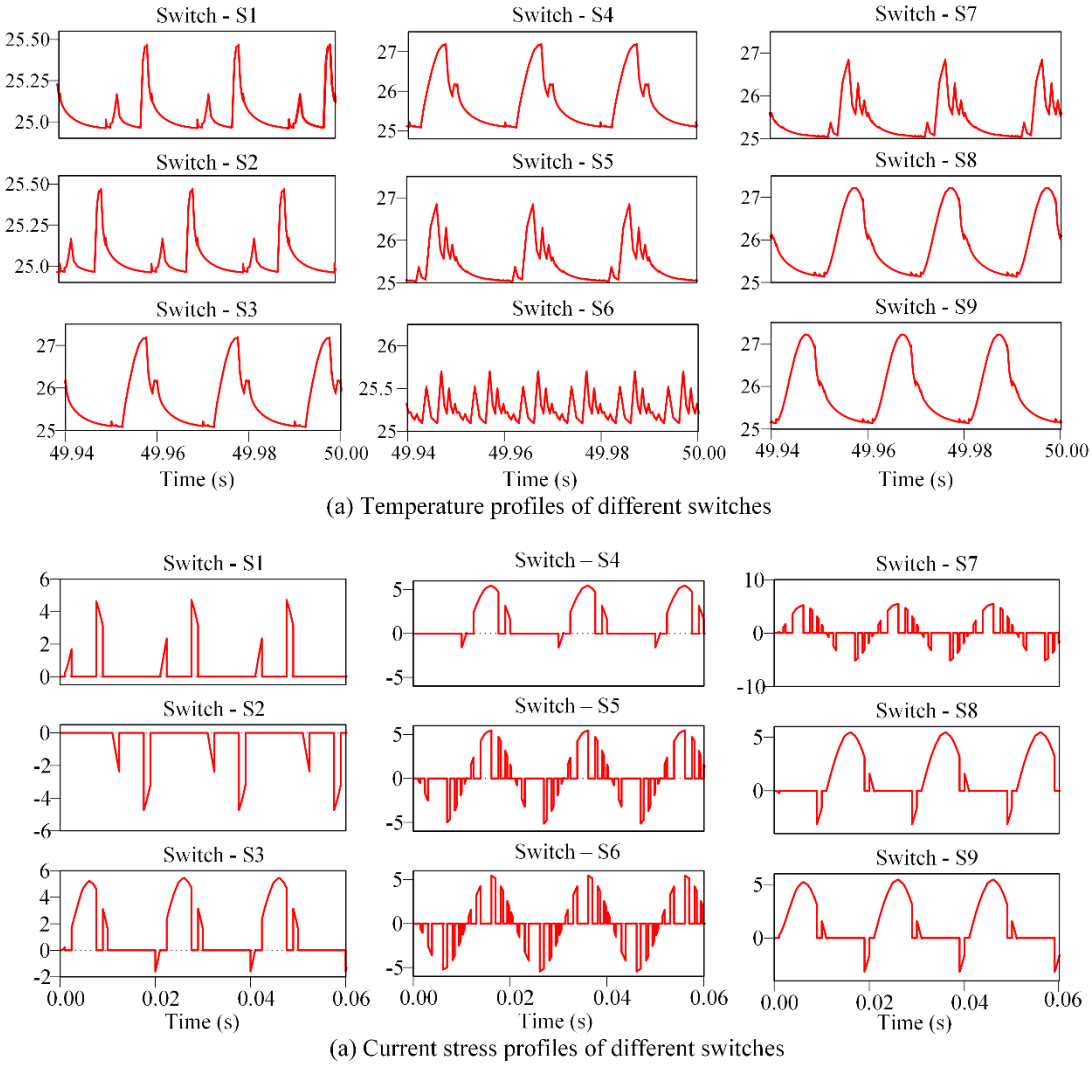


FIGURE 14. Current stress and temperature profiles of the switches.

topology. One of the main limitations of the proposed structure is the utilization of bi-directional switches, which adds to the device count and increases the TSV p.u. Although MLIs find application in various fields, integrating renewable resources into the utility grid is one of the most prominent applications [8]. The proposed topology based on the above discussion is suitable for solar PV applications.

VII. CONCLUSION

This paper presented an improved asymmetrical multilevel inverter topology. The proposed topology generates seventeen output voltage levels by utilizing two DC sources and nine switches; three of these switches are bidirectional switches. The concept of a dc-link capacitor across the sources is used to increase the output levels. The capacitors are self-balancing, and no extra effort is required for the balancing operation of the capacitors. The results obtained for different load conditions confers the static and dynamic stability of the topology. Moreover, power loss analysis gives insight into the dynamics of the switches used. Based on the comparative analysis, it can be concluded that the proposed topology offers superior performance than other compared topologies present in the literature. The topology is highly efficient and is much suitable for renewable energy applications like grid-tied solar PV systems.

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M. SAAD BIN ARIF (Member, IEEE) was born in Aligarh, India. He received the degree in electrical engineering, in 2010, and the master's degree in electrical engineering with a specialization in power system and drives, in 2010. He has research/teaching experience of more than eight years. His research interests include multilevel inverters, MPPT, and power electronics in renewable energy systems, energy systems, and engineering education.

UVAIS MUSTAFA was born in Meerut, India, in 1995. He received the B.Tech. degree in electrical engineering and the M.Tech. degree (Hons.) in instrumentation and control from Aligarh Muslim University, in 2016 and 2019, respectively. In 2019, he joined University Polytechnic, Aligarh Muslim University, as an Assistant Professor. He has published journal articles and conference papers. His research interests include power electronics converters, renewable energy, and control of power electronics converters. He was awarded the Gold Medal for holding the First Rank in his master's degree.

SHAHRIN BIN MD AYOB (Senior Member, IEEE) was born in Kuala Lumpur, Malaysia. He received the degree in electrical engineering, the master's degree in electrical engineering (power), and the Ph.D. degree from Universiti Teknologi Malaysia, in 2001, 2003, and 2009, respectively. He is currently an Associate Professor with the Faculty of Engineering, School of Electrical Engineering, Universiti Teknologi Malaysia. He is also a registered Graduate Engineer under the Board of Engineer Malaysia (BEM). His current research interests include solar photovoltaic systems, electric vehicle technology, fuzzy systems, and evolutionary algorithms for power electronics applications.

JOSE RODRIGUEZ (Life Fellow, IEEE) received the degree in electrical engineering from Universidad Técnica Federico Santa María, Valparaíso, Chile, in 1977, and the Dr.-Ing. degree in electrical engineering from the University of Erlangen, Erlangen, Germany, in 1985.

Since 1977, he has been with the Department of Electronics Engineering, Universidad Técnica Federico Santa María, where he was a Full Professor and the President. Since 2015, he has been the President of Universidad Andrés Bello, Santiago, Chile. He has coauthored two books, several book chapters, and more than 400 journal articles and conference papers. His main research interests include multilevel inverters, new converter topologies, control of power converters, and adjustable-speed drives. He is a member of the Chilean Academy of Engineering. He has received a number of best paper awards from journals of the IEEE. He received the National Award of Applied Sciences and Technology from the Government of Chile, in 2014, and the Eugene Mittelmann Award from the Industrial Electronics Society of the IEEE, in 2015.

ABDUL NADEEM received the B.Tech. degree in electrical engineering from Dr. A.P.J. Abdul Kalam Technical University, in 2015, where he is currently pursuing the master's degree in instrumentation and control. His research interests include multilevel inverters, switching control of power converters, and control of power electronics converters.

MOHAMED ABDELRAHEM (Member, IEEE) was born in Assiut, Egypt, in 1985. He received the B.Sc. (Hons.) and M.Sc. degrees in electrical engineering from Assiut University, Assiut, in 2007 and 2011, respectively, and the Ph.D. degree (Hons.) in electrical engineering from the Technical University of Munich (TUM), Munich, Germany, in 2020.

Since 2014, he has been teaching power electronics and renewable energy systems at TUM. Furthermore, he has been supervising several master theses in the field of control of power electronics, photovoltaic energy systems, and variable-speed wind energy conversion systems. Since 2019, he has been the Head of the Renewable Energy Systems Research Group, Institute for Electrical Drive Systems and Power Electronics (EAL), TUM. Since 2020, he has been an Assistant Professor with Assiut University. His research interests include power electronics, predictive and encoderless control of variable-speed wind generators, photovoltaic energy systems, and energy storage systems. He has received a number of best paper awards from high-prestigious international conferences of the IEEE.