Received 8 May 2021; revised 22 June 2021; accepted 29 June 2021. Date of publication 6 July 2021; date of current version 20 July 2021.
The review of this article was arranged by Editor A. G. U. Perera.

Digital Object Identifier 10.1109/JEDS.2021.3094795

Size Effects of Poly-Si Formed by Laser Annealing With Periodic Intensity Distribution on the TFT Characteristics

AKIRA MIZUTANI [1], FUMINOBU HAMANO [2], DAISUKE NAKAMURA [2] (Member, IEEE), TETSUYA GOTO [3], SITI RAHMAH AID [4], AND HIROSHI IKENOUE [1,2] (Member, IEEE)

1 Department of Gigaphoton Next GLP, Kyushu University, Fukuoka 819-0395, Japan
2 Graduate School of Information Science and Electrical Engineering, Kyushu University, Fukuoka 819-0395, Japan
3 New Industry Creation Hatchery Center, Tohoku University, Sendai 980-8579, Japan
4 Malaysia-Japan International Institute of Technology, Universiti Teknologi Malaysia, Kuala Lumpur 54100, Malaysia

CORRESPONDING AUTHOR: A. MIZUTANI (e-mail: mizutani.akira.072@m.kyushu-u.ac.jp)

ABSTRACT Currently, low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs), which are characterized by high mobility of electrons, are fabricated by excimer laser annealing. High mobility in low-temperature polycrystalline silicon is achieved by controlling the grain size to approximately 300 nm. However, with future potential growth of active-matrix organic light-emitting diodes in terms of their increasing use as backlight in active matrix micro-LEDs, even higher mobility is required. One of the methods to improve mobility is to produce grains of sizes above 300 nm. However, as far as we know, there are no reports of investigating the dependence between the device characteristics and the grain size of above 300 nm. In this study, we examine the possibility of controlling the grain size above approximately 350 nm by laser annealing with an intensity distribution and investigate the grain size dependence of the TFT characteristics. We show that the grain size can be controlled approximately in the range of 1–2.5 μm, and mobility of 248±28 cm^2 V^{-1} s^{-1} is achieved at a grain size of 2.5 μm. Furthermore, we compare the device characteristics of the step-and-repeat and scan annealing and verify that the device characteristics do not deteriorate even during scan annealing. The study confirms that it is technically possible to produce LTPS with grain sizes controlled in the range of 1-2.5 μm for customizing device characteristics.

INDEX TERMS Low temperature polycrystalline Si (LTPS), thin-film-transistor (TFT), excimer laser annealing (ELA).

I. INTRODUCTION

Low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) crystallized using the excimer laser annealing (ELA) method [1]–[6] have higher mobility than amorphous silicon (a-Si) and oxide semiconductor transistors, and are used as a standard material for active-matrix organic light-emitting diode backplanes of mobile devices [7]. It has been reported that grain sizes in the range of 50–350 nm can be obtained while annealing a-Si with a top-flat shape laser beam of ELA [8], [9], with a maximum size of approximately 300 nm to obtain uniformity in grain size distribution for mass production [10]. A typical value of the mobility of LTPS obtained through ELA is approximately 100–150 cm^2 V^{-1} s^{-1}, which satisfies the requirement of the current common display applications [10]. A rapid growth in display technology will increase the demand for higher pixel density, higher frame rate, and higher brightness. For example, a higher frame rate is required in the automobile application and higher brightness is required to ensure visibility under sunlight such as signage and transparent displays. In active matrix micro-LED displays, TFTs have been widely used for backplanes, and high mobility is required [11]. The mobility of the LTPS TFTs can be increased by making the grain size larger than 350 nm. To realize this, it is important to control the grain size in the range of more than 350 nm and estimate the grain size

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

dependency of mobility. As a previous study on controlling grain size, van der Wilt *et al.* reported that a square-grained polycrystalline material obtained using dot-SLS [12], [13] and position-controlled square crystals with a side of 3 μm could be formed by using substrate-embedded seeds [14]. As a similar study, Moschou *et al.* reported the shape dependence of the TFT characteristics when the grain shape was manipulated using a mask-shaped laser beam. The grain size dependency, however, was not discussed [15]. Meanwhile, as a previous study on the relationship between mobility and grain size Choi *et al.* fabricated an LTPS TFT where poly-crystallization was performed using the sequential lateral solidification method. They reported that the tendency of the field-effect mobility increases with the increase in the grain size [16]. As a similar study, Ishihara reported grain size dependence of the TFT device characteristics in the range of grain size of less than 1 μm [17]. Taking these into account, this study demonstrated controlling the LTPS grain size in the range of more than 1 μm using ELA with the intensity distribution. The grain size dependence of the TFTs' mobility was also investigated and compared with the theory for the first time. Furthermore, we compared the device characteristics of the step-and-repeat and scan annealing and clarified that the device characteristics did not deteriorate even during scan annealing.

II. EXPERIMENTAL METHODS

A. LASER ANNEALING SYSTEM

In this study, a dot array mask and a projection optical system with a reduction rate of 1/20 were used to generate the laser intensity distribution. The mask consisted of circular metal thin films of diameter 10 μm at the grid position to block the irradiated laser beam. Crystal growth started around the blocked part of the dot array, and square grains were formed [refer to Fig. 1(a)]. The pitch size of the dot array was varied in the range of 15 μm to 80 μm to control the size of the grain between 0.75 μm and 4 μm. Seven types of masks with different grid sizes were used for this purpose. Fig. 1(b) shows the schematic of the laser annealing system. The light source was an excimer laser [GT600K/ Gigaphoton Inc., wavelength: 248 nm, pulse duration (full width at half-maximum): 80 ns]. The dot array mask was illuminated using light from the illumination optical system that equalizes illuminance. The projection optical system projected light from a dot array mask in a 200 μm × 200 μm area on the sample surface. A projection lens with NA = 0.36 was used to reduce diffraction at the edges of the dot array. The thickness of the thin films of the mask was 125 nm. Before annealing, the tilt adjustment and the focus adjustment were performed using the tilt stage, z stage, and laser length measuring sensor to vertically incident the laser on the sample and match the image plane to the sample surface. As shown in Fig. 1 (c) annealing was performed in two ways: step-and-repeat annealing, in which the effects of the vibration of the stage can be ignored, and the scan annealing that is important in industrial processes. In the step-and-repeat

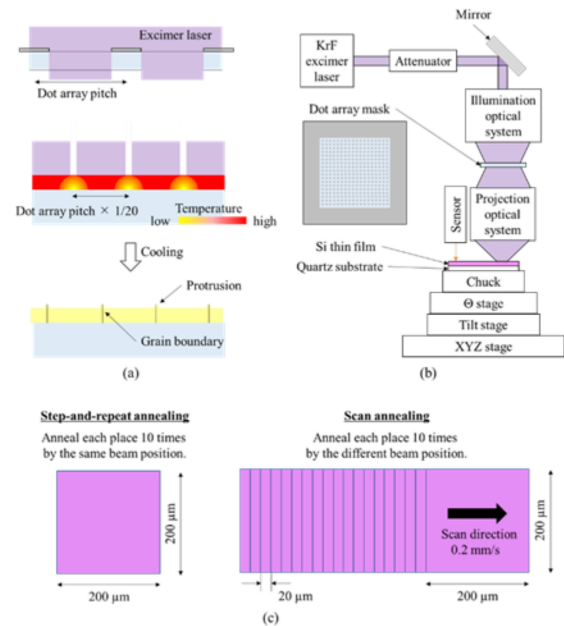

FIGURE 1. (a) Concept of laser annealing with intensity distribution using dot array mask. (b) Schematic of excimer-laser annealing setup. (c) Schematic of step-and-repeat annealing and scan annealing.

annealing, the laser irradiation was superimposed at each fixed area of 200 μm × 200 μm. In the scan annealing, laser irradiation was performed with a pitch of 20 μm by moving the substrate at a scan speed of 0.2 mm/s. The grain shapes and sizes were investigated by scanning the electron microscopy (SEM) observation of a defect-etched poly-Si film. For defect-etching, poly-Si film was dipped in the secco-solution (5 wt.% $K_2Cr_2O_7$: 50 wt.%HF = 3: 1) for 40 s and was rinsed with H_2O at approximately 300 K. The actual grain size was defined as the length of one side assuming that the shape was square. The area of grains was calculated by image processing the SEM images. The protrusion heights were investigated by analyzing transmission electron microscopy (TEM) observation.

B. TFT FABRICATION

Fig. 2(a) shows the schematic of the top-gate transistor fabrication process, and Fig. 2(b) shows the optical image of the fabricated LTPS TFTs on the glass. The length (L) and width (W) of the fabricated TFT channels were 20 μm and 30 μm, respectively. The process flow is as follows: First, a-Si (100 nm) films were deposited onto a quartz substrate through low-pressure chemical vapor deposition at 550 °C. Next, the a-Si film was crystallized using ELA. The number of laser shots was 10, and the laser fluence was 660 mJ/cm^2. These values were experimentally optimized. The repetition rate of the laser was 10 Hz. After poly-crystallization of the Si film through ELA, the poly-Si film was defined as having island patterns using photolithography and wet etching. The Si film etchant was a mixture of HF, HNO_3, and H_2O. A gate-insulator SiO_2 film with a thickness

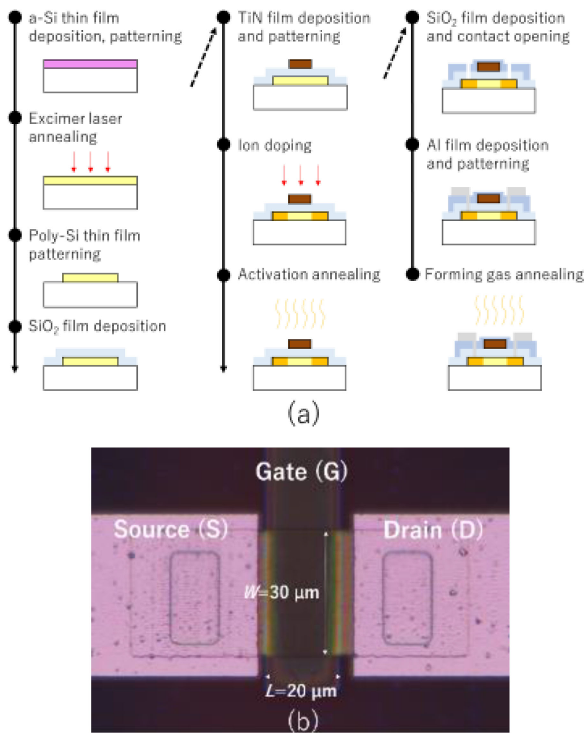

FIGURE 2. **(a) Schematics of top-gate transistor fabrication process. (b) Optical image of fabricated TFT with the channel length (*L*) of 20 µm and channel width (*W*) of 30 µm.**

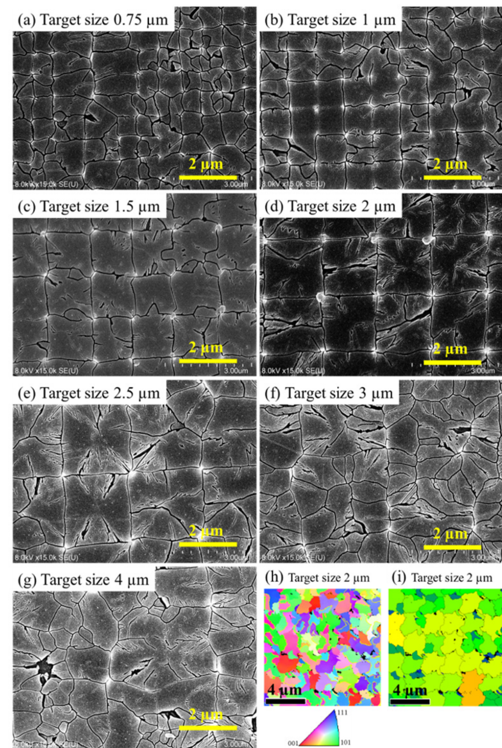

FIGURE 3. **(a)–(g) Scanning the electron microscopy images of each dot array pitch in step-and-repeat annealing. (h) The inverse pole figure map of target size of 2 µm. (i) Unique grain map of target size of 2 µm.**

of 100 nm was deposited at 350 °C through microwave-excited plasma-enhanced chemical vapor deposition. For the gate electrode, TiN film with a thickness of 150 nm was deposited using reactive DC magnetron sputtering and patterned by wet etching (a mixture of HF, HNO_3, and H_2O). P+ ions at 140 keV with a dose of 5×10^{15} cm^{-2} were implanted to form a self-aligned source/drain region utilizing the gate electrode pattern as a mask. This was followed by activation annealing in N_2 atmosphere at 550 °C for 1 h. Next, a dielectric film of SiO_2 (150 nm) was deposited through atmospheric pressure CVD at 400 °C. The contact holes were opened using wet etching (HF solution). A contact metal of Al was deposited through DC magnetron sputtering and patterned by wet etching (mixture of H_3PO_4, CH_3COOH, HNO_3, and H_2O). Finally, the forming gas (Ar/H_2 = 900/100 sccm) annealing was performed at 400 °C for 0.5 h.

C. MEASURING TFT CHARACTERISTICS

The electrical characteristics (drain current (I_{DS})–gate voltage (V_{DS}) characteristics) of the fabricated TFTs were measured at about 300 K using a Keysight B1500A semiconductor device analyzer. The TFT field-effect mobility (μ_{FE}) was obtained using the following equation:

$$\mu_{FE} = \frac{L}{W}\frac{1}{C_{OX}V_{DS}}\frac{\partial I_{DS}}{\partial V_G}, \tag{1}$$

where C_{OX} is the gate oxide capacitance per unit area, I_{DS} is the drain current, V_{DS} is the drain bias, and V_G represents the gate bias. The threshold voltage (V_{th}) was obtained as the gate voltage at which $I_{DS}\times L/W$ is equal to 100 nA at drain bias (V_{DS}) = 0.05 V. Subthreshold swing (SS) was obtained using the following equation:

$$SS = \frac{\partial V_G}{\partial log_{10}(I_{DS})} \tag{2}$$

The gate-induced drain leakage (GIDL) current was calculated from the difference at the gate voltage of 0 V of I_{DS} and the tangent on I_{DS} at drain bias (V_{DS}) = 10 V [18], [19].

III. RESULTS AND DISCUSSION

Fig. 3 (a)-(g) shows the SEM images with a target grain size of 0.75 µm to 4 µm in the step-and-repeat annealing. The white dots in the grid position of the SEM images represent conical protrusions, and the black lines represent grain boundaries. Fig. 3 (h) shows the inverse pole figure map and Fig. 3(i) shows the unique grain map of target size of 2 µm. A grain boundary with an orientation difference of 5 degrees or more was defined as a grain boundary, and the Σ3 boundary was defined as not a grain boundary in Fig. 3 (i). In addition to the square grain boundary, the Σ3 boundary is also present inside the square. The crystal orientation was random in each grain. In the following analysis of grain size, we will not treat the Σ3 boundary as a grain boundary. Fig. 4 shows the TEM image of the grain boundary with a dot array pitch of 40 µm. The protrusions of approximately 20 nm were formed on the sides of the

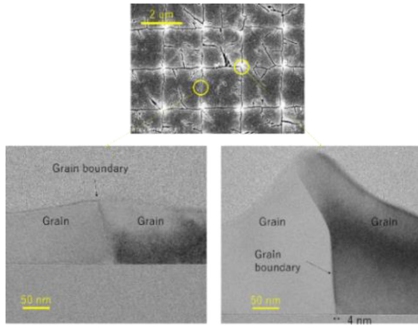

FIGURE 4. Transmission electron microscopy images of protrusions with a grain size of 2 µm.

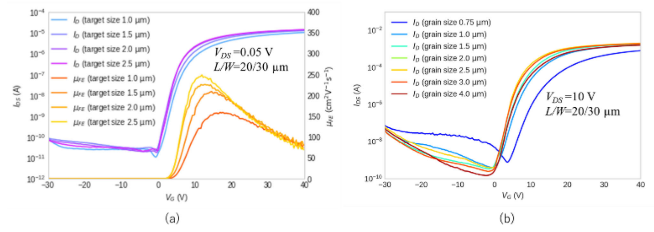

FIGURE 5. (a) Transfer curves of the target grain size of 1 to 2.5 µm at V_{DS} = 0.05 V (b) Transfer curves of all target size at V_{DS} = 10 V.

TABLE 1. Actual size, μ_{FE}, V_{th}, *SS* and GIDL of each target grain size.

Target grain size (µm)	0.75	1	1.5	2	2.5	3	4
Actual grain size ave ± 1σ (µm)	0.44 ±0.29	0.92 ±0.47	1.58 ±0.21	1.93 ±0.05	2.27 ±0.17	1.19 ±0.61	1.04 ±0.49
μ_{FE} (cm^2 V^{-1} s^{-1})	73 ±4	159 ±16	210 ±14	215 ±26	248 ±28	224 ±20	155 ±56
V_{th} (V)	8.0 ±0.3	4.6 ±0.2	3.7 ±0.2	3.3 ±0.3	3.1 ±0.5	3.4 ±0.3	5.7 ±2.7
SS (V/dev)	0.8 ±0.6	1.38 ±0.06	1.26 ±0.08	1.2 ±0.1	1.0 ±0.1	1.0 ±0.1	1.0 ±0.5
GIDL (nA)	1.7 ±1.3	0.3 ±0.2	0.1 ±0.01	0.7 ±0.5	0.6 ±0.5	0.1 ±0.1	0.5 ±0.5

square grains and approximately 200 nm on the diagonal. These protrusions were formed at grain boundaries during the cooling process after laser annealing due to the difference in mass densities of the liquid phase and the solid phase silicon [20]. This difference in mass density causes liquid silicon to accumulate in the final solidification region, resulting in the formation of redundant silicon protrusions in the grain boundary region [21]. We will discuss the influence of protrusions later. By comparing the SEM images of each dot array pitch in Fig. 3, it can be seen that square grains have been formed with a target grain size of 1 to 2.5 µm. With a target grain size of 0.75 µm, there were many regions where square grains of 0.75 µm were not formed. Forming grains of 0.75 µm is difficult because the resolution of reduced transcription ($0.61 \times \lambda$ / NA = 0.42 µm by Rayleigh's criterion) was insufficient for the intensity distribution interval of 0.75 µm. Therefore, using a lens with higher NA, it is possible to form a grain size of 0.75 µm or less via this method. With a target grain size of 3 µm, there were grain boundaries on the contour of the square of 3 µm, but there were also many grain boundaries inside the square. With a target grain size of 4 µm, there were almost no grain boundaries on the square, and the grains were almost random. Therefore this method has shown that there was a limit to the grain growth size of about 3 µm. Previous studies in which the grain size was controlled using a-Si spacers reported that the grain size was limited to about 2.5 µm for 100 nm a-Si film [22], which is consistent with this result. In a previous study [23] that experimentally clarified the relationship between the lateral growth length and the fluence gradient, the lateral growth length was approximately 1.5 µm at the fluence gradient of over 200 mJ cm^{-1} µm^{-1}. This lateral growth length of approximately 1.5 µm (approximately 3 µm as the grain size) is good agreement with the grain size of 2.5 µm in this study, in which the fluence gradient was 1200 mJ cm^{-1} µm^{-1}. Therefore, the grain size of 2.5∼3 µm would be the limit size annealed by this step and repeat method.

Fig. 5 (a) shows the transfer curves at the drain current of 0.05 V with the target grain size of 1–2.5 µm. Fig. 5 (b) shows the transfer curves at the drain current of 10 V with the all target grain size. Each transfer curve was the result of measuring typical TFT out of the 25 TFTs fabricated. The ON–OFF ratio of drain current of approximately 10^6 was obtained. Table 1 shows the actual grain size, μ_{FE}, V_{th}, *SS* and GIDL of each target grain size. With the target grain size of 2.5 µm, the field effect mobility was 248 ± 28 cm^2 V^{-1} s^{-1}. The mean and standard deviation of actual grain size, μ_{FE}, V_{th}, *SS* and GIDL were calculated from 25 TFTs fabricated. With the target grain size ranging from 1 µm to 2.5 µm, the larger the grain size, the more improved the mean value of μ_{FE}, V_{th}, and *SS*. As the grains became larger, the ratio of the volume occupied by the grain boundaries to the volume occupied by the grains decreased, thereby decreasing the number of trap state and improving μ_{FE}, V_{th}, and *SS*. The standard deviation tends to increase as the grain size increases because the statistical error increases as the number of grain boundaries present in the channel decrease. With the target size of 4 µm, the variation in the formed grain size was very large; therefore, the variation in field-effect mobility was also large. This is consistent with the prediction stated in previous studies that the variation in mobility increases as the variation in grain size increases [3], [24].

Fig. 6 (a) shows the relationship of actual grain size and target grain size. As above, with the target size of 1-2.5 µm, the target size is approximately equal to the actual grain size. Fig. 6 (b) shows the dependence of GIDL current on the actual grain size. As the grains became larger in the size of less than 1.5 µm, the ratio occupied by the grain boundaries decreased, so the GIDL was reduced. It is suggested that

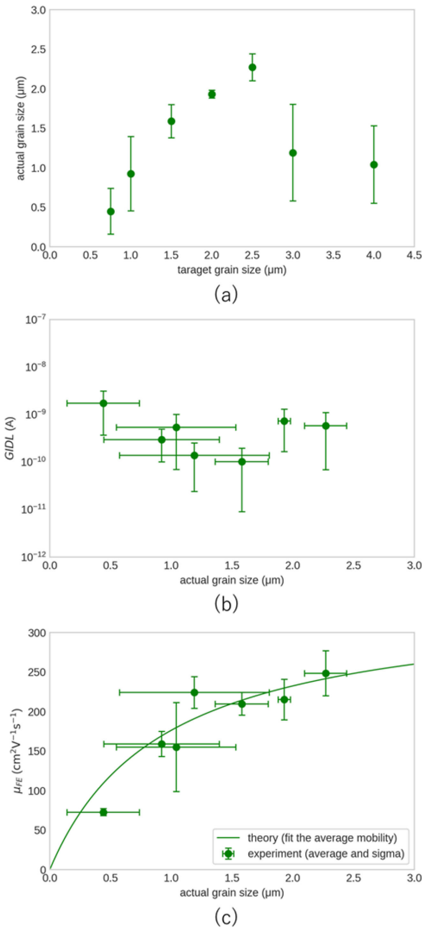

FIGURE 6. (a) Relationship of actual size and target grain size (b) Experimental result of GIDL of each actual size. (c) Experimental result and the fitting curve of field effect mobility of each actual size.

GIDL of actual grain size larger than 2 μm were higher than GIDL of less than 1.5 μm due to radial grain boundaries. Fig. 6 (c) shows the actual grain size dependence of the field-effect mobility. The plots in Fig. 6 (c) show the field effect mobilities of each actual grain size. The solid line represents a fitting curve that fits the average value of each actual size of field-effect mobility. The experimental results show that the larger the actual grain size, the higher the field-effect mobility. We utilized the following equation to calculate the fitting curve of the relationship between the field-effect mobility and grain size:

$$\frac{1}{\mu_{FE}} = \frac{1}{\mu_{GB}} + \frac{1}{\mu_G}. \tag{3}$$

Here, μ_G is the mobility due to scattering in the grain, and μ_{GB} is the mobility due to scattering in the grain boundary expressed as follows:

$$\mu_{GB} = \frac{qL_G}{\sqrt{2\pi m^* kT}} \exp\left(-\frac{qE_B}{kT}\right). \tag{4}$$

TABLE 2. Calculation parameters and fitting parameters used to calculate the theoretical value of field-effect mobility.

		Symbol	Value/ Unit
Parameters used in the calculations	Temperature	T	300 K
	Effective mass	m*	$0.26\times9.11\times10^{-31}$ kg
	Boltzmann constant	k	1.38×10^{-23} m² kg s⁻² K⁻¹
	Electron charge	q	1.60×10^{-19} C
Fitting parameters	Potential barrier	E_B	0.10 V
	Mobility from the scattering in the grain	μ_G	340 cm² V⁻¹ s⁻¹

This is called Seto's model [25]. Combining (3) and (4), the field effect mobility is expressed as follows:

$$\frac{1}{\mu_{FE}} = \frac{\sqrt{2\pi m^* kT}}{qL_G} \exp\left(\frac{qE_B}{kT}\right) + \frac{1}{\mu_G}. \tag{5}$$

Fitting parameters, E_B and μ_G in (5), were fitted to match the experimental results. A summary of the calculation parameters and fitting parameters is shown in Table 2.

Consequently, the fitting parameters were $E_B = 0.10$ V and $\mu_G = 340$ cm^2 V^{-1} s^{-1}. Billah *et al.* reported that $E_B = 0.075$ V at the grain boundary protrusion with a height of 35 nm [26]. They also reported that the lower the height of the protrusion was, the lower the drain current (mobility) was [26]. Seto's model shows that smaller E_B leads to smaller mobility. Therefore, it is suggested that the higher the protrusion, the higher E_B. The protrusion was higher in our study because the grain size was larger (more than 1 μm) than the grain size used in the previous report (about 350 nm). Helen *et al.* fabricated a TFT through super lateral growth (SLG) and measured the field-effect mobility parallel to the growth direction. They obtained a field-effect mobility of 510 cm^2 V^{-1} s^{-1}, which was mainly limited by the electron properties of the intragrain region [27]. Meanwhile, Ishihara *et al.* formed square crystal grains on the substrate-embedded seeds by ELA, investigated the effect of coincident site lattice (CSL) boundary in the grain on mobility. They reported that the mobility of more than 500 cm^2 V^{-1} s^{-1} can be obtained even if the Σ3 boundary exists but the value of mobility decreased to 320 cm^2 V^{-1} s^{-1} when the Σ9 boundary exists in the grain [28]. This suggests that the value of mobility is 340 cm^2 V^{-1} s^{-1} due to Σ9 boundary existed inside the grains in this study.

From the results of this experiment and comparison with the theoretical formula, decreasing E_B and increasing μ_G increased the mobility. To reduce E_B, it would be effective to reduce the protrusion [26]. Therefore, we are researching reducing protrusions through additional irradiation. We have reported that we reduced the height of the protrusions and flattened the surface by introducing additional irradiation and increasing the field-effect mobility [29]. Another method is increasing μ_G. To achieve this, it is important to reveal the mechanism through which Σ9 boundaries are formed and prevent the formation of Σ9 boundaries.

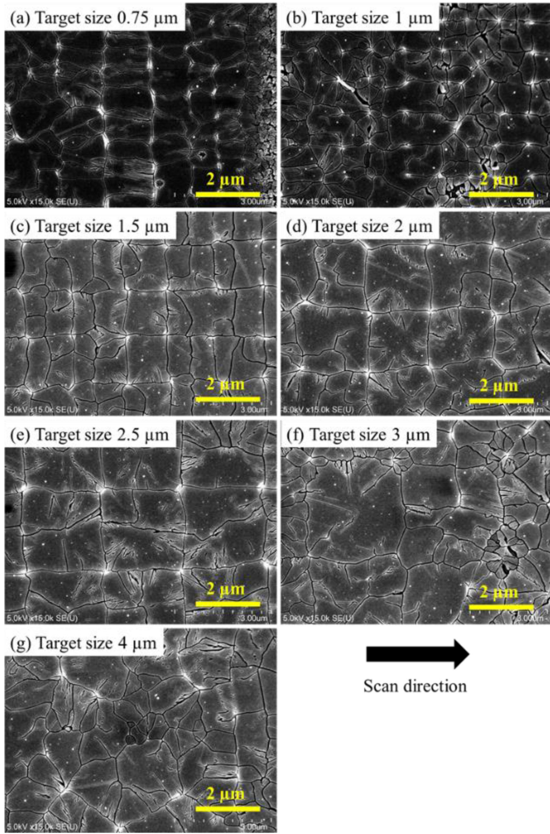

FIGURE 7. (a)–(g) Scanning the electron microscopy images of each target grain size in scan annealing.

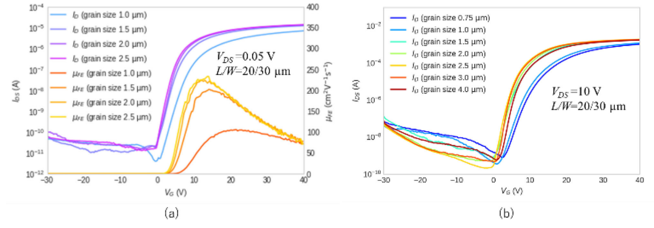

FIGURE 8. (a) Transfer curves of the target grain size of 1 to 2.5 μm at V_{DS} = 0.05 V (b) Transfer curves of all target size at V_{DS} = 10 V in scan annealing.

TABLE 3. μ_{FE}, V_{th}, *SS* and GIDL of each target grain size.

Target grain size (μm)	0.75	1	1.5	2	2.5	3	4
Actual grain size ave ± 1σ (μm)	0.91 ± 0.51	1.13 ± 0.54	1.37 ± 0.41	1.95 ± 0.85	2.45 ± 0.78	2.19 ± 0.89	1.41 ± 0.68
μ_{FE} ave ± 1σ ($cm^2 V^{-1} s^{-1}$)	94 ±11	109 ±13	201 ±15	224 ±22	233 ±38	232 ±26	192 ±25
V_{th} (V)	7.4 ±0.7	5.7 ±0.9	3.6 ±0.4	3.3 ±0.4	3.2 ±0.6	3.2 ±0.6	4.0 ±0.8
SS (V/dev)	1.5 ±0.1	1.47 ±0.08	1.2 ±0.2	1.17 ±0.08	1.02 ±0.1	1.0 ±0.1	1.1 ±0.6
GIDL (nA)	2.3 ±1.6	1.9 ±1.3	1.0 ±0.7	1.4 ±1.3	0.7 ±0.7	0.9 ±0.8	0.4 ±0.2

In the scan annealing, laser irradiation was performed while moving the stage. Vibration measurements were performed to evaluate the effects of vibration on the electric stage. Consequently, during the operation of the stage, there was vibration with a maximum vibration amplitude of ± 0.2 μm (standard deviation is ±0.1 μm) in the horizontal direction. The vibration amplitude of the vibration in the z direction was less than 0.1 μm. Fig. 7 shows the SEM images with a target grain size ranging from 0.75 μm to 4 μm in the scan annealing. Even in the scan annealing with the vibration, uniform square-shaped grains were formed with a target grain size ranging from 1.5 μm to 2.5 μm. However, with the target grain sizes of less than 2 μm, the position of protrusion was displaced, and the grains were distorted compared with the step-and-repeat annealing. With the target grain size of less than 1.5 μm, there was a disorder of the grains period. This occurred because the beam irradiation pitch of 20 μm was not an integral multiple of the grain size. In other words, it is important to select an appropriate scan speed. With the target grain size of 0.75 μm, the shape of the crystal grains was on a distorted rectangle extending in the scanning direction. This is due to the effects of stage movement and vibration. With the target grain size of 1 μm, as in the case of step-and-repeat annealing, a region where 1 μm square crystal grains were formed and a region where the crystal grains were disturbed coexisted. This is suggested to be due to the influence of the vibration of the stage. With the target grain sizes of 3 μm and 4 μm, the form of the grain was as disturbed as that of step-and-repeat annealing.

Fig. 8 (a) shows the transfer curves at the drain current of 0.05 V with the target grain size of 1–2.5 μm. Fig. 8 (b) shows the transfer curves at the drain current of 10 V with the all target grain size. Each transfer curve was the result of measuring the typical TFT out of the 25 TFTs fabricated. The ON–OFF ratio of the drain current of approximately 10^6 was obtained, which was comparable to that of the step-and-repeating annealing. Table 3 shows the average and deviation values of the actual grain size, μ_{FE}, V_{th}, *SS* and GIDL in the scan annealing. The grain size dependence of the actual grain size, μ_{FE}, V_{th} and *SS* was the same as that of the step-and-repeat annealing. With the target grain size range of 1.5 μm to 2.5 μm, the average and deviation of the scan annealing were comparable to that of the step-and-repeat annealing. Fig. 9 shows the comparison between the field-effect mobilities of scan annealing and step-and-repeat annealing. Even in the scanning method with vibration of ±0.2 μm, the grain boundary scattering did not increase compared to the step-and-repeat method. By reducing the vibration of the stage, it is possible to achieve the same performance as the step-and-repeat annealing, even with a target grain size of less than 1 μm. Figs. 10 and 11 show the grain size dependence of the average values of V_{th} and *SS*, respectively. V_{th} and *SS* did not deteriorate

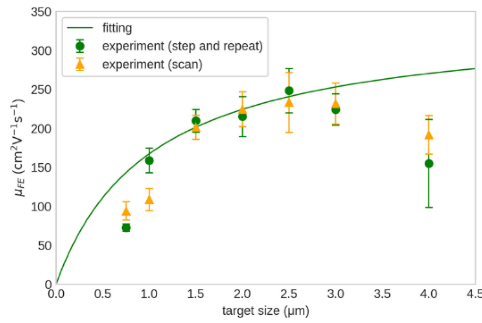

FIGURE 9. Experimental values of step-and-repeat and scan annealing, and theoretical values of field-effect mobility for each target grain size.

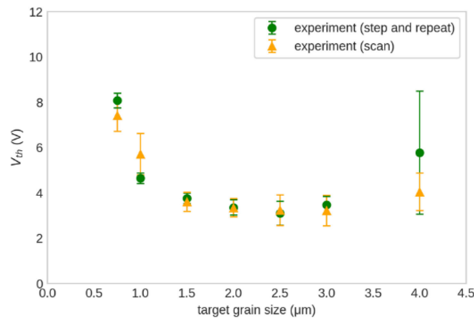

FIGURE 10. Experimental values of V_{th} for each target grain size in step-and-repeating and scan annealing.

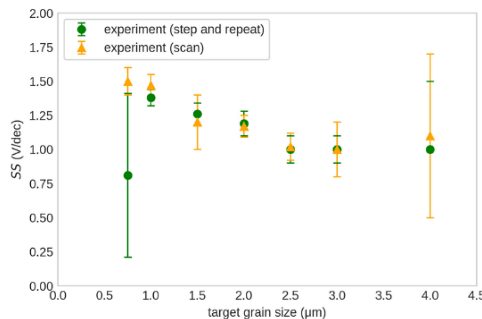

FIGURE 11. Experimental values of *SS* for each target grain size in step-and-repeating and scan annealing.

with scan annealing. Figs. 10 and 11 show that V_{th} and *SS* decreased as the target grain size increased. In the range of the target grain size of less than 2.5 μm, the actual grain size decreased with respect to the decreasing of the target grain size. Therefore, the volume ratio of the grain boundaries to the entire grain decreased and the number of trap density state decreased. In a previous study simulating the relationship between the volume ratio of crystal grains and grain boundaries and V_{th} and *SS*, it has been reported that V_{th} and *SS* decreases as the crystal grain size increases [24]. Fig. 12 shows the GIDL current was higher with the scan annealing. It is suggested that the cause of the increase in GIDL was that the grains were disturbed by the vibration of the stage.

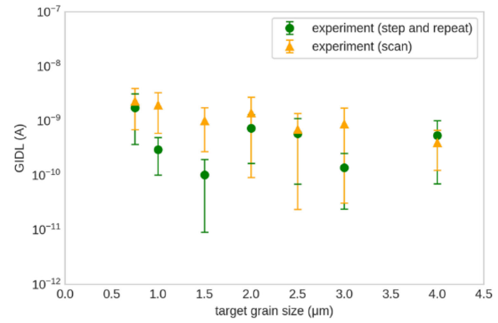

FIGURE 12. Experimental values of GIDL for each target grain size in step-and-repeating and scan annealing.

From the above, we have shown that it was possible to overlay uniform grains together using the proposed method. In scan annealing, GIDL becomes approximately an order of magnitude larger, but it was shown that mobility, V_{th} and *SS* can achieve the same performance as step & repeat annealing.

IV. CONCLUSION

As a result of performing laser annealing with an intensity distribution using a step-and-repeat method, it was verified experimentally that the grain size can be controlled in the range of approximately 1–2.5 μm. It was also experimentally verified that the larger the grain size, the higher the field-effect mobility and the lower the V_{th} and *SS*. The TFT with a grain size of 2.5 μm fabricated in this study had high field-effect mobility of 248 ± 28 cm^2 V^{-1} s^{-1}. In addition, regarding the scan annealing, the grain size can also be controlled in the same way as with the step-and-repeat method. The mobility, V_{th}, and *SS* were comparable to those of step-and-repeat annealing. The results of this study show that it would be technically possible to produce LTPS that can control the grain size of 1-2.5 μm for customizing the device characteristics.

REFERENCES

[1] T. Sameshima, S. Usui, and M. Sekiya, "XeCl Excimer laser annealing used in the fabrication of poly-Si TFT's," *IEEE Electron Device Lett.*, vol. 7, no. 5, pp. 276–278, May 1986, doi: 10.1109/edl.1986.26372.

[2] K. Shimizu, H. Hosoya, O. Sugiura, and M. Matsumura, "High-mobility bottom-gate thin-film transistors with laser-crystallized and hydrogen-radical-annealed polysilicon films," *Jpn. J. Appl. Phys.*, vol. 30, no. 12S, p. 3704, 1991.

[3] A. Hara, F. Takeuchi, and N. Sasaki, "Mobility enhancement limit of excimer-laser-crystallized polycrystalline silicon thin film transistors," *J. Appl. Phys.*, vol. 91, p. 708, Jan. 2002, doi: 10.1063/1.1420766.

[4] Y. Nakazaki *et al.*, "Characterization of novel polycrystalline silicon thin-film transistors with long and narrow grains," *Jpn. J. Appl. Phys. I, Reg. Paper Short Notes Rev. Paper*, vol. 45, p. 1489, Mar. 2006, doi: 10.1143/JJAP.45.1489.

[5] M. Mitani, T. Endoy, S. Tsuboiz, T. Okaday, G. Kawachix, and M. Matsumura, "Relationship between thin-film transistor characteristics and crystallographic orientation in excimer-laser-processed pseudo-single-crystal-silicon films," *Jpn. J. Appl. Phys.*, vol. 49, Dec. 2010, Art. no. 124001, doi: 10.1143/JJAP.49.124001.

[6] T. Goto *et al.*, "LTPS thin-film transistors fabricated using new selective laser annealing system," *IEEE Trans. Electron Devices*, vol. 65, no. 8, pp. 3250–3256, Aug. 2018, doi: 10.1109/TED.2018.2846412.

[7] J. Souk, S. Morozumi, F.-C. Luo, and I. Bita, *Flat Panel Display Manufacturing*. New York, NY, USA: Wiley, 2018.

[8] E. Fogarassy *et al.*, "Surface melt dynamics and super lateral growth regime in long pulse duration excimer laser crystallization of amorphous Si films," *Thin Solid Films*, vol. 337, pp. 143–147, Jan. 1999, doi: 10.1016/S0040-6090(98)01434-5.

[9] A. T. Voutsas, "A new era of crystallization: Advances in polysilicon crystallization and crystal engineering," *Appl. Surface Sci.*, vols. 208–209, pp. 250–262, Mar. 2003, doi: 10.1016/S0169-4332(02)01343-0.

[10] M. Sobey, K. Schmidt, B. Turk, and R. Paetzel, "Status and future promise of Excimer laser annealing for LTPS on large glass substrates," in *Soc. Inf. Display Int. Symp. Dig. Tech. Paper*, 2014, pp. 79–82, doi: 10.1002/j.2168-0159.2014.tb00022.x.

[11] H.-A. Ahn, S.-K. Hong, and O.-K. Kwon, "An Active matrix micro-pixelated LED display driver for high luminance uniformity using resistance mismatch compensation method," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 6, pp. 724–728, Jun. 2018, doi: 10.1109/TCSII.2018.2790412.

[12] P. C. van der Wilt, B. A. Turk, A. B. Limanov, A. M. Chitu, and J. S. Im, "A hybrid approach for obtaining orientation-controlled single-crystal Si regions on glass substrates," in *Proc. Photon Process. Microelectron. Photon. V*, vol. 6106, 2006, Art. no. 61060B, doi: 10.1117/12.651139.

[13] P. C. Van Der Wilt, A. M. Chitu, B. A. Turk, U. J. Chung, A. B. Limanov, and J. S. Im, "(Eq100) textured Si films with controlled microstructures obtained via hybrid SLS," in *Proc. Int. Meeting Inf. Display*, vol. 2006, 2006, pp. 768–771.

[14] P. C. Van Der Wilt, B. D. Van Dijk, G. J. Bertens, R. Ishihara, and C. I. M. Beenakker, "Formation of location-controlled crystalline islands using substrate-embedded seeds in excimer-laser crystallization of silicon films," *Appl. Phys. Lett.*, vol. 79, p. 1819, Jul. 2001, doi: 10.1063/1.1402641.

[15] D. C. Moschou, M. A. Exarchos, D. N. Kouvatsos, G. J. Papaioannou, and A. T. Voutsas, "Performance and reliability of SLS ELA polysilicon TFTs fabricated with novel crystallization techniques," *Microelectron. Rel.*, vol. 47, pp. 1378–1383, Sep./Nov. 2007, doi: 10.1016/j.microrel.2007.07.073.

[16] J. B. Choi *et al.*, "9.2: Sequential lateral solidification (SLS) process for large area AMOLED," in *SID Int. Symp. Dig. Tech. Paper*, 2008, pp. 97–100, doi: 10.1889/1.3069845.

[17] R. Ishihara, "Effects of grain-boundaries in excimer-laser crystallized poly-Si thin-film transistors," in *Proc. 31st Eur. Solid-State Device Res. Conf.*, Nuremberg, Germany, 2001, pp. 479–482, doi: 10.1109/ESSDERC.2001.195305.

[18] J. S. Chauhan *et al.*, *FinFET Modeling for IC Simulation and Design*. London, U.K.: Academic, 2015.

[19] M. Galeti, M. Rodrigues, J. A. Martino, N. Collaert, E. Simoen, and C. Claeys, "GIDL behavior of p- and n-MuGFET devices with different TiN metal gate thickness and high-k gate dielectrics," *Solid-State Electron.*, vol. 70, pp. 44–49, Apr. 2012, doi: 10.1016/j.sse.2011.11.015.

[20] B.-W. Chen *et al.*, "Surface engineering of polycrystalline silicon for long-term mechanical stress endurance enhancement in flexible low-temperature poly-Si thin-film transistors," *ACS Appl. Mater. Interfaces*, vol. 9, no. 13, pp. 11942–11949, 2017, doi: 10.1021/acsami.6b14525.

[21] H.-T. Chen, Y.-C. Chen, J.-X. Lin, S.-I. Hsieh, and Y.-C. King, "Roughness effect on uniformity and reliability of sequential lateral solidified low-temperature polycrystalline silicon thin-film transistor," *Electrochem. Solid-State Lett.*, vol. 9, p. H81, Jun. 2006, doi: 10.1149/1.2209430.

[22] H.-C. Cheng *et al.*, "Periodically lateral silicon grains fabricated by Excimer laser irradiation with a-Si spacers for LTPS TFTs," *J. Electrochem. Soc.*, vol. 154, no. 1, p. J5, 2007, doi: 10.1149/1.2382420.

[23] M. Lee, S. Moon, M. Hatano, K. Suzuki, and C. P. Grigoropoulos, "Relationship between fluence gradient and lateral grain growth in spatially controlled excimer laser crystallization of amorphous silicon films," *J. Appl. Phys.*, vol. 88, p. 4994, Oct. 2000, doi: 10.1063/1.1314303.

[24] K. Shirai, F. Oshiro, T. Noguchi, H. M. Koo, and H. S. Choi, "Influence of grain size deviation on the characteristics of poly-Si thin film transistor," *J. Korean Phys. Soc.*, vol. 59, no. 2, pp. 298–303, 2011, doi: 10.3938/jkps.59.298.

[25] J. Y. W. Seto, "The electrical properties of polycrystalline silicon films," *J. Appl. Phys.*, vol. 46, no. 12, pp. 5247–5254, 1975, doi: 10.1063/1.321593.

[26] M. M. Billah *et al.*, "Effect of grain boundary protrusion on electrical performance of low temperature polycrystalline silicon thin film transistors," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 503–511, 2019, doi: 10.1109/JEDS.2019.2911088.

[27] Y. Helen *et al.*, "High mobility thin film transistors by Nd:YVO4-laser crystallization," *Thin Solid Films*, vol. 383, nos. 1–2, pp. 143–146, 2001.

[28] R. Ishihara *et al.*, "Electrical property of coincidence site lattice grain boundary in location-controlled Si island by excimer-laser crystallization," *Thin Solid Films*, vol. 487, nos. 1–2, pp. 97–101, 2005, doi: 10.1016/j.tsf.2005.01.044.

[29] F. Hamano, A. Mizutani, K. Imokawa, D. Nakamura, T. Goto, and H. Ikenoue, "Improvement of the surface roughness of LTPS thin films with additional laser irradiation," in *Proc. 27th Int. Display Workshop*, 2020, pp. 322–324. [Online]. Available: https://confit.atlas.jp/guide/event-img/idw2020/FMCp3-07/public/pdf_archive?