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Impact of phonon scattering mechanisms on the performance of silicene nanoribbon field-effect transistors

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ABSTRACT

Rigorous efforts are invested globally in the semiconductor industry to leverage next-generation nanoelectronics beyond Moore's law. Among them, silicene is foreseen as a viable two-dimensional (2D) material for future transistor applications. In this study, we assessed the performance of field-effect transistors (FETs) based on silicene nanoribbons (SiNRs) in terms of width scaling, length scaling and non-ballistic phonon scattering effects. Simulation of the channel material and transistor is performed based on the nearest neighbour tight-binding model and the top-of-the-barrier nanotransistor model, respectively. The device performance is analysed by graphically extracting the on-to-off current ratio, subthreshold swing and drain-induced barrier lowering from the current–voltage characteristics. It is also revealed that the impact of phonon scattering effects becomes less significant as the channel lengths of the SiNR FETs become shorter than the mean free paths. Overall, it is shown that the width and length scaling are among the crucial factors in designing nanoribbon-based FETs owing to their unique properties.

Introduction

Technology innovations in the miniaturisation of computer components, especially semiconductor transistors, have improved the computing power in our modern lives [1]. Unfortunately, the transistor miniaturisation, which is governed by the famous Moore's Law, is at its bottleneck as transistors are scaled down to the sub-10-nm atomic scales [2–4]. Therefore, the development of the next-generation field-effect transistors (FETs) to leverage nanoelectronics beyond Moore's law, has become one of the mainstream research topics.

Numerous R&D funding and programmes are invested globally for exploring a viable solution for this issue, including 2D materials-based electronics and nanoelectronics research [5]. Common 2D materials include graphene [6], black phosphorus [7], transition metal dichalcogenide monolayers [8], silicene [9], and others. In general, 2D materials offer high carrier mobility. For instance, the highest hole mobility reported by Feng *et al.* for black phosphorus is approximately $862 cm^2 V^{-1} s^{-1}$ [7]; and the intrinsic electron mobility reported by Li *et al.* for silicene is approximately $1200 cm^2 V^{-1} s^{-1}$ [10].

Among the discovered 2D materials, silicene is foreseen as a competitive contender due to its high carrier mobility [11] and compatibility with the cutting-edge silicon (Si) semiconductor technology [12]. Moreover, silicene is included as a potential material for transistor miniaturisation in the International Roadmap for Devices and Systems (IRDS) [13]. Interestingly, the electronic properties of silicene (such as bandgap and transport effective mass) can be tuned by tailoring silicene nanosheets into silicene nanoribbons (SiNRs) owing to the impact of quantum confinement in the width direction [14]. As a result, the SiNR FETs can be carefully designed to achieve the desired current–voltage (I-V) characteristics through width scaling [15].

The first silicene-based transistor operating at room temperature was demonstrated by Tao *et al.* in 2015. In addition, silicene nanosheets have successfully been fabricated on various substrates in their buckled [16–18] and planar [19] forms. Overall, most of the studies reported deposition of silicene on metal substrates of which the electronic properties are differ from the theoretically predicted limits. Nevertheless, a direct growth of silicene or other 2D materials on insulating layers, such as dielectrics or oxides [20], is more preferable for transistor applications. While waiting for the breakthrough in silicene-based fabrication research domain, computational models are rigorously used to predict

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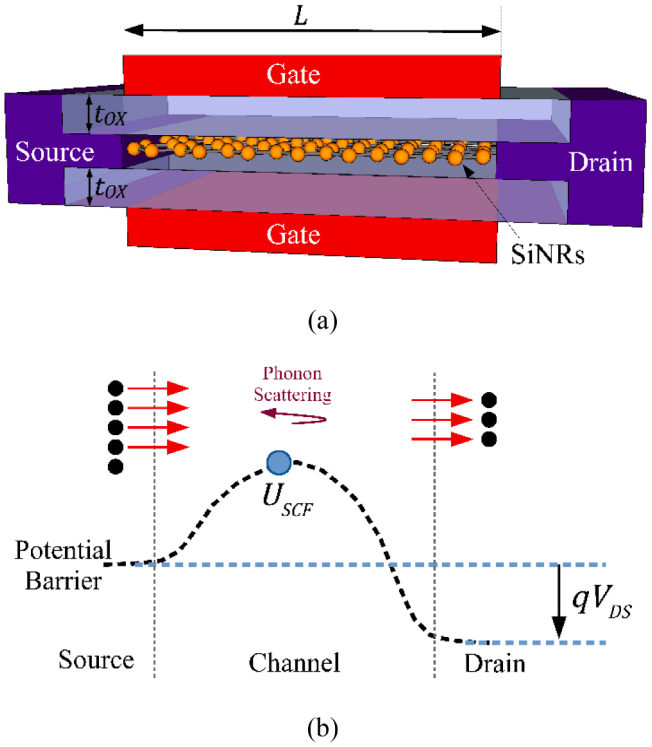


Fig. 1. Schematic diagrams of (a) the structure of SiNR FET and (b) the simplified quasi-ballistic transport of carriers at the top of the barrier.

the transistor performance of silicene-based transistors [21–24].

Among the existing models on silicene-based transistors [9,25], there is still minimal work focusing on the non-ballistic effects on the device performance. Therefore, in this paper, we proposed an extension to the existing top-of-the-barrier ballistic nanotransistor model [26,27] to include the phonon scattering mechanism [28] in SiNR FETs. Fig. 1 shows the schematic diagram of the proposed SiNR FET and the simplified quasi-ballistic transport model. This paper describes the development of the SiNR FET models from material level to device level. Section "**Model implementation**" describes the modelling procedures employed in this work. In Section "**Performance analysis and discussion**", the impacts of length scaling and phonon scattering mechanisms to the device performance of SiNR FETs are discussed. In the final section, the conclusion and future work recommendation are described.

Model implementation

This section describes the material-level and device-level modelling procedures employed in this study, where the overall flowchart is depicted in Fig. 2.

NNTB model for electronic properties

At the material-level modelling, the electronic properties of N_A-ASiNRs (where N_A is the nanoribbon width) were computed using the NNTB model as shown in Ref. [29]. For instance, the atomic arrangement in Fig. 3(a) is denoted as 10-ASiNR owing to the number of atoms within the unit cells. The Hamiltonian matrices of SiNRs can be computed by using

$$h(k) = \beta' e^{-ika} + \alpha + \beta e^{+ika}, \tag{1}$$

based on the derivation from the time-independent Schrödinger equation [30] where α is the unit-cell matrix which describes the hopping energies within the unit cells as shown in blue dotted box in Fig. 3(a) and the β is the interaction matrix which describes the interactions among the neighbouring unit cells. β' is the transverse matrix of β and $a = 0.382nm$ is the lattice constant of silicene [31]. To ensure the accuracy of the NNTB model, the 10-ASiNR band structure is benchmarked with the first-principle calculation results from Ding *et al.* [14], as shown in Fig. 3 (b).

Referring to Fig. 3(b), the NNTB band structure fits almost perfectly around the valence band maximum and conduction band minimum regions. The bandgap is also extracted from the band structure. Because the main objective of this work is to use the electronic properties for FET

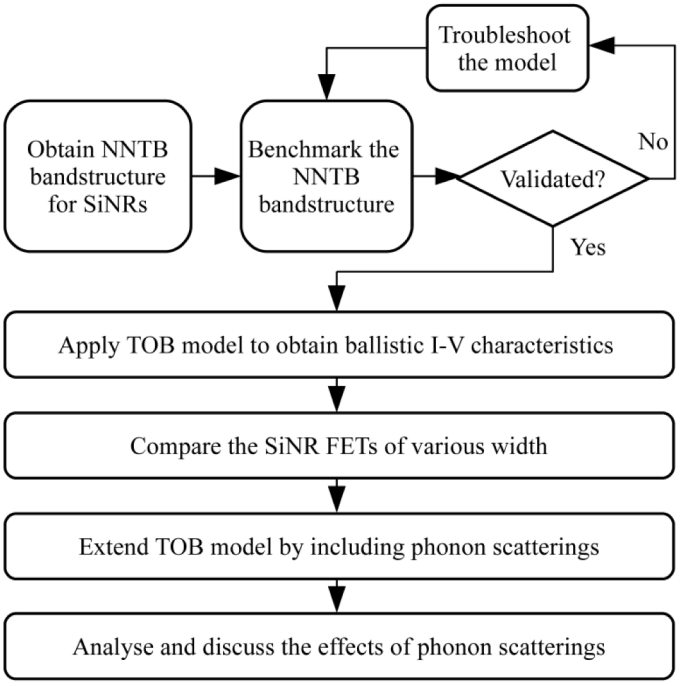


Fig. 2. Overall flowchart of this work.

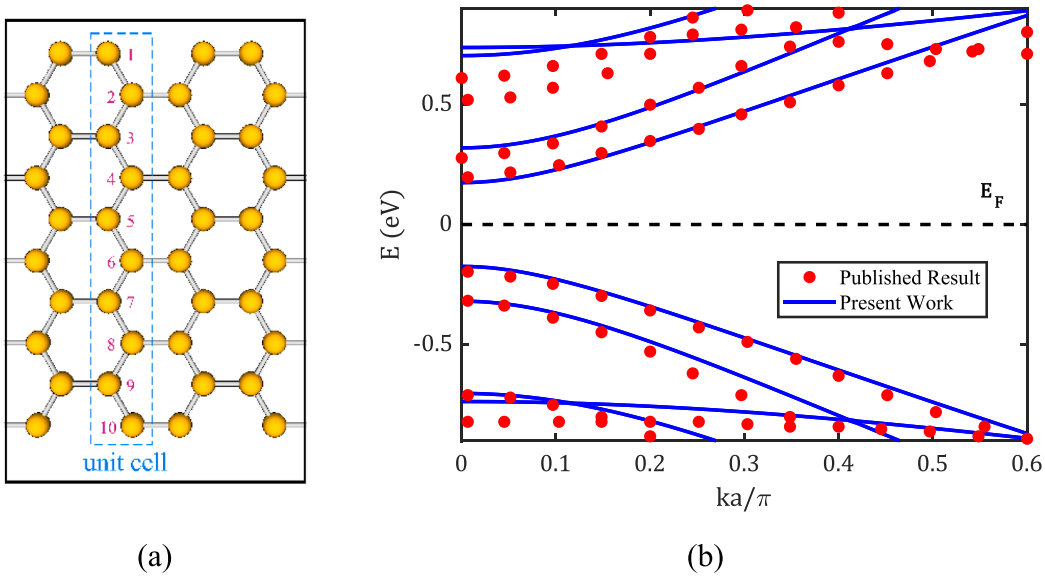


Fig. 3. (a) Schematic diagram of the atomic structure for a 10-ASiNR and (b) benchmark of band structure for the pristine 10-ASiNR. In (b), blue solid lines show the band structure of present work and red dots show the band structure from the first-principle calculations [14]. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

Table 1
The device parameters of ballistic SiNR FETs.

Parameters	Values
Band structures	NNTB
Oxide material	SiO_2
Oxide thickness, t_{OX}	$1.5nm$
S/D metals	Ideal
Temperature, T	$300K$

applications, the less fit regions of the NNTB band structure can be neglected. The band structures, that are accurate within the energy range of $E = 3k_BT \approx 0.08\ eV$, are sufficient to produce decent I-V characteristics [32]. In this study, only the ASiNRs from the $N_A = 3p+1$ family were selected because this particular width family produces the larger bandgap compared to $N_A = 3p$ and $N_A = 3p+2$ families.

Ballistic ToB transistor model for I-V characteristics

Having the NNTB band structures verified, the results from material-level modelling are then employed in the ballistic top-of-the-barrier (ToB) nanotransistor model [27]. Similar modelling procedures were described in our previous work [26]. In this work, the gate and drain control parameters are initially set as $\alpha_G = 1$ and $\alpha_D = 0$, respectively, to obtain the perfect room temperature ($T = 300K$) subthreshold swing $SS = 60mV/dec$ [15]. The device parameters of the SiNR FETs are summarised in Table 1. The I-V characteristics of 7-ASiNR FET under ballistic transport produced by the ballistic ToB nanotransistor model are shown in Fig. 4. Subsequently, the on-to-off current ($I_{on/off}$) ratio is extracted graphically from the transfer characteristics in Fig. 4(a).

Following that, the widths N_A of the SiNR FETs are varied. Fig. 5 shows the impact of width scaling to the bandgap of SiNRs and $I_{on/off}$ ratio of the ballistic SiNR FETs. The results show that only the 7-ASiNR effectively produces bandgap value within the range $0.4eV \leq E_g \leq 3.0eV$, such that it is optimum for nanoelectronic digital switching applications [33]. In addition, the 7-ASiNR FET produces $I_{on/off}$ ratio of 3.32×10^5, the highest ratio achieved among the selected widths within $N_A = 3p+1$ SiNRs family. Similar results were also observed by the study on graphene nanoribbon (GNR) FETs by Wong *et al.* [34]. Therefore, the modelling procedures hereafter will only focus on 7-ASiNR FETs.

Incorporating phonon scattering effects

In order to examine the impact of scattering effects on SiNR FETs with respect to channel length scaling, the ideal gate and drain control parameters are modified accordingly [35] for the channel lengths L of $10nm$, $8nm$ and $6nm$, respectively. By adapting the gate and drain control parameters for the length scaling from Hosseini *et al.*, the resulting transfer characteristics are plotted as shown in Fig. 6. It is clearly shown that the device performance metrics are degraded as the channel length becomes shorter. This performance degradations, owing to short gate length, have also been shown by other studies involving low-dimensional transistors [36–38]. These performance metrics will be further discussed in the latter section.

Furthermore, the ballistic ToB nanotransistor model is extended by including the non-ballistic phonon scattering effects [28], schematically shown in Fig. 1(b). The transmission coefficients $T_D(E)$ and $T_S(E)$, expressed as

$$T_S(E) = \frac{L_{eff}(0)}{L_{eff}(0) + L}, \tag{2}$$

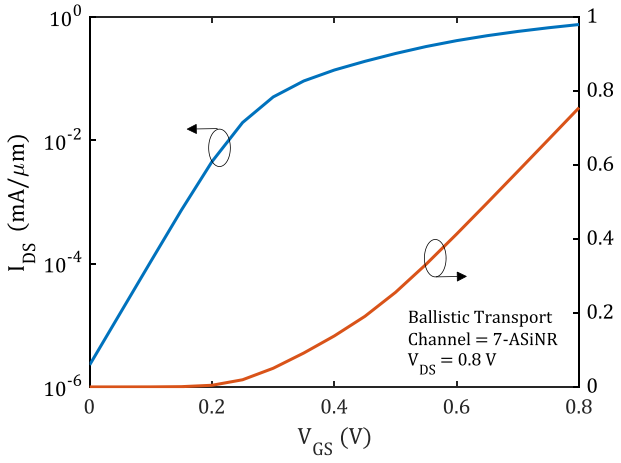
and

$$T_S(E) = \frac{L_{eff}(V_{DS})}{L_{eff}(V_{DS}) + L}, \tag{3}$$

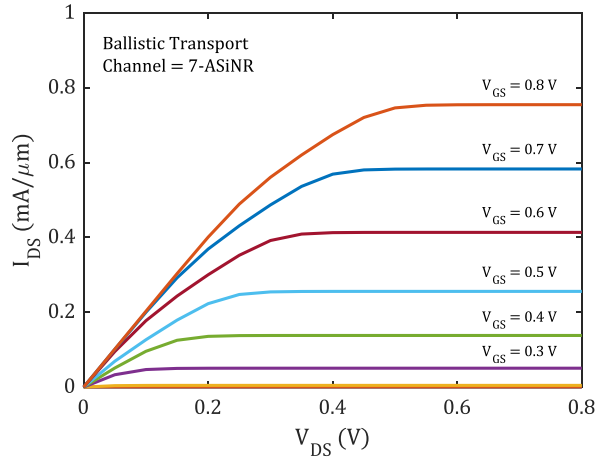
for drain and source terminals [39], respectively, can be introduced to the Landauer-Büttiker ballistic current transport equation such that

$$I_{DS}(V_{GS}, V_{DS}) = \frac{q}{2}\int_{-\infty}^{+\infty} |v(E)\,|D(E)\big[T_S(E)f_S(E_S) - T_D(E)f_D(E_D)\big]\,dE. \tag{4}$$

The effective phonon scattering mean free path (MFP) [28] in Eqns. (2) and (3) is given as



(a) transfer characteristics



(b) output characteristics

Fig. 4. I-V characteristics of 7-ASiNR FET under ideal ballistic transport at room temperature ($T = 300K$). Gate voltage, V_{GS} in (b) at the top is $0.8V$ with $0.1V$ step for each subsequent lines.

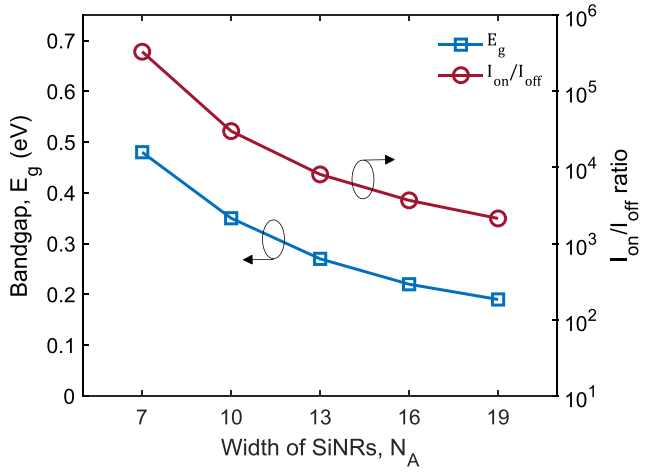


Fig. 5. Bandgaps and I_{on}/I_{off} ratio versus the width N_A of SiNRs at room temperature ($T = 300K$).

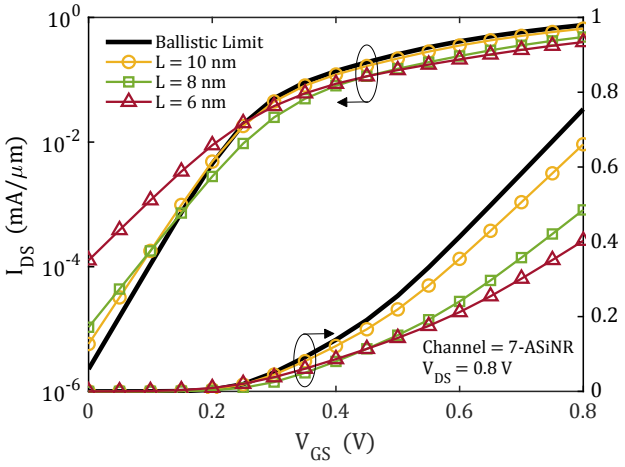


Fig. 6. Transfer characteristics of 7-ASiNR FETs with channel length scaling at room temperature ($T = 300K$).

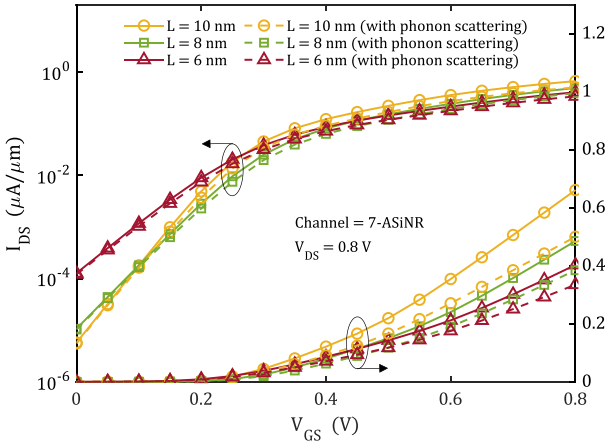


Fig. 7. Transfer characteristics of 7-ASiNR FETs with channel length scaling at room temperature ($T = 300K$): without phonon scattering effects (solid lines) and with phonon scattering effects (dashed lines).

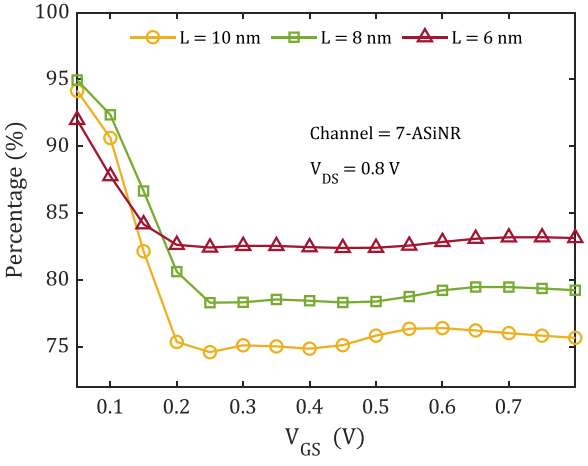


Fig. 8. Percentage of the I_{DS} for 7-SiNR FETs at room temperature ($T = 300K$) with phonon scattering effects, with respect to the I_{DS} for 7-SiNR FETs without phonon scattering effects.

Table 2
Device performance metrics for 7-SiNR FETs of various channel lengths, with and without phonon scattering effects.

	Without phonon scattering effects			With phonon scattering effects		
$L(nm)$	$I_{on/off}$ ratio	SS (mV/dec)	DIBL (mV/V)	$I_{on/off}$ ratio	SS (mV/dec)	DIBL (mV/V)
10	1.15×10^5	66.9	39.8	9.04×10^4	67.9	39.9
8	4.54×10^4	81.6	75.9	3.74×10^4	82.4	75.9
6	3.17×10^3	103.0	233.5	2.78×10^3	105.4	233.6

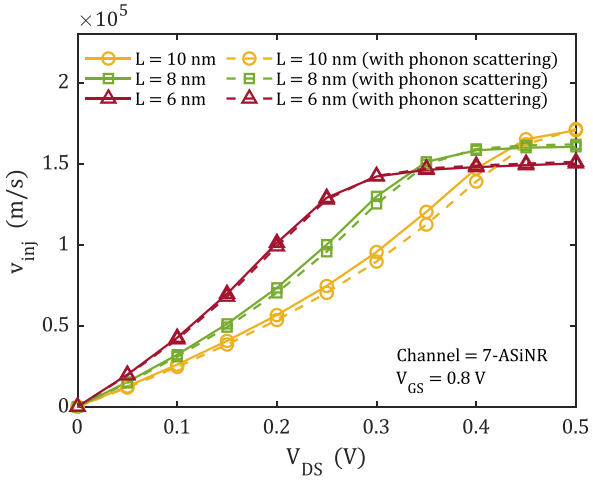


Fig. 9. Average carrier injection velocity v_{inj} at the top-of-the-barrier as a function of drain voltage V_{DS} at room temperature ($T = 300K$).

$$\frac{1}{L_{eff}(V_x)}=\frac{1}{L_{ap}}\left\{1-\frac{1}{1+\exp\left[\frac{E_F-U_{SCF}+qV_x}{k_BT}\right]}\right\}+\frac{1}{L_{op}}\left\{1-\frac{1}{1+\exp\left[\frac{(E_F-U_{SCF}-\hbar\omega_{op}+qV_x)}{k_BT}\right]}\right\}, \tag{5}$$

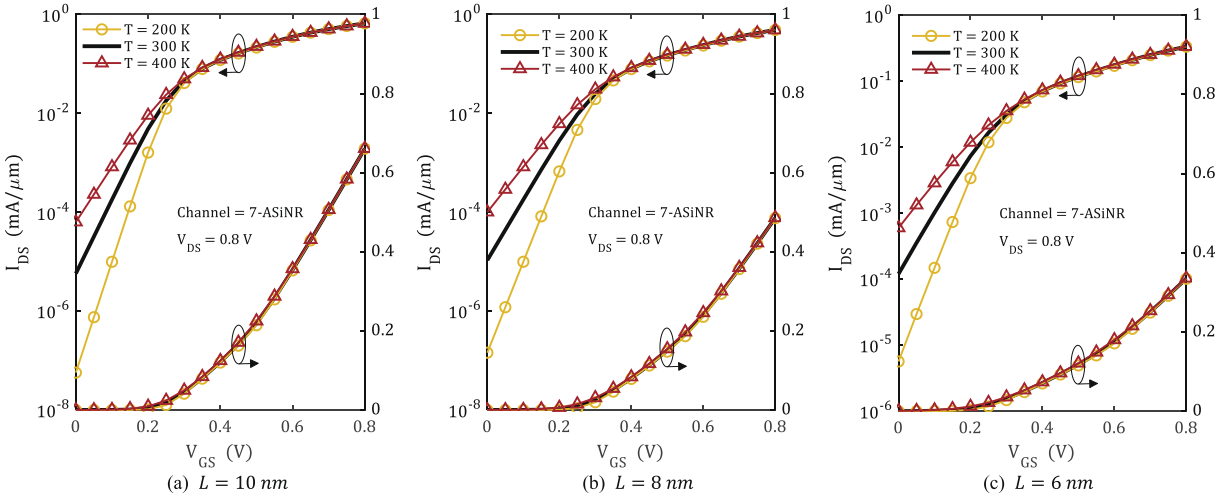
where $\hbar\omega_{op}\approx0.16\,eV$ is the optical phonon energy and V_x is substituted by $V_x = 0V$ and $V_x = V_{DS}$ for the transmission coefficients for source and drain, respectively. The length quantities to incorporate the phonon scattering effects in the ballistic ToB nanotransistor model include the channel length L, the acoustic phonon scattering MFP, $L_{ap} = 178nm$, and optical phonon scattering MFP, $L_{ap} = 29nm$ adapted from Ref. [40]. By applying Eqn. (4), the impact of phonon scattering to the I-V characteristics of 7-ASiNR FETs can be plotted, as shown in Fig. 7.

Performance analysis and discussion

By using the transfer characteristics in Fig. 7, we examine the impact of phonon scattering effects, by dividing the drain currents with phonon scattering effects by the drain current without phonon scattering effects, to obtain the respective drain current percentage. The resulting percentage is plotted in Fig. 8. It is clearly shown that the phonon scattering effects are not obvious at low V_{GS}, owing to the fact that there are not much mobile electrons when the channel potential barrier is high. As V_{GS} increases, the drain current percentage for all channel lengths decreases, indicating the influence of phonon scattering effects to the 7-ASiNR FETs. In general, Fig. 8 clearly shows that the phonon scattering effects are more dominant when the channel length is shorter, where the drain currents are reduced by approximately 17% for $L = 6nm$, 21% for $L = 8nm$, and 25% for $L = 10nm$ at high V_{GS} compared to the drain current of 7-ASiNR FETs without phonon scattering effects.

The device performance metrics of 7-ASiNR FETs of various lengths are also extracted from Fig. 7 and tabulated in Table 2. In this section, two additional parameters are extracted, namely the subthreshold swing (SS) and drain-induced barrier lowering (DIBL) [41]. This comparison clearly shows that the phonon scattering mechanisms have more impact on the $I_{on/off}$ ratio for all lengths of 7-ASiNR FETs, where the $I_{on/off}$ ratio is reduced by 12.3% for $L = 6nm$, 17.6% for $L = 8nm$, and 21.4% for $L = 10nm$. On the other hand, the phonon scattering mechanisms have more impact on the SS compared to DIBL. Nevertheless, the influence of phonon scattering mechanisms to both of these parameters are not as significant as the $I_{on/off}$ ratio. However, these relationships should be further explored by considering different FET device structures or material properties [42] to obtain further information.

For further insights, the carrier injection velocity v_{inj} for 7-SiNR FETs is calculated using $v_{inj} = I_{DS}/Q_{ToB}$, where Q_{ToB} is the charge density at the top-of-the-barrier [27]. Fig. 9 shows the resulting carrier injection velocity plot for 7-SiNR FETs of different channel lengths. In addition, the effects of temperature towards the transfer characteristics of 7-ASiNR FETs with phonon scattering effects are also computed, as shown in Fig. 10. The effects of temperature are not obvious in the linear scale transfer characteristic plots because the drain currents beyond the subthreshold region remain almost the same for all temperature. It is shown the higher temperature could degrade the performance of the 7-



(a) $L = 10\ nm$ (b) $L = 8\ nm$ (c) $L = 6\ nm$

Fig. 10. Transfer characteristics of 7-ASiNR FETs with channel length scaling and phonon scattering effects at various temperature.

ASiNR FETs especially in the subthreshold operating region, regardless of the channel lengths. Therefore, heat management [43] in 7-ASiNR FETs is also important towards their device performance.

Conclusion

In this paper, we have investigated the impact of width scaling, length scaling and non-ballistic phonon scattering effects on the SiNRs-based FETs by employing NNTB and ToB models at the material-level and device-level simulations, respectively. After systematic analysis on the width scaling, 7-ASiNR is identified as the decent choice for the channel material due to its high $I_{on/off}$ ratio. Following that, the impact of width scaling and phonon scattering are examined by extending the existing ballistic ToB nanotransistor model. In summary, the performance analysis in this study shows that the width and length scalings are among the crucial factors in designing nanoribbons-based FETs owing to their unique properties. This work can be extended by including additional non-ballistic effects such as tunnelling and leakage currents to provide further insights on this prospective 2D material for future nanoelectronic applications.

CRediT authorship contribution statement

Mu Wen Chuan: Methodology, Writing - review & editing, Writing - original draft. **Munawar Agus Riyadi:** Methodology, Funding acquisition, Formal analysis. **Afiq Hamzah:** Conceptualization, Writing - review & editing. **Nurul Ezaila Alias:** Resources. **Suhana Mohamed Sultan:** Project administration. **Cheng Siong Lim:** Software. **Michael Loong Peng Tan:** Funding acquisition, Supervision, Writing - review & editing.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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