Device performance of silicene nanoribbon field-effect transistor under ballistic transport

Mu Wen Chuan
School of Electrical Engineering
Universiti Teknologi Malaysia
81310 Johor Bahru, Malaysia
muwen94@gmail.com

Kien Liong Wong
School of Electrical Engineering
Universiti Teknologi Malaysia
81310 Johor Bahru, Malaysia
liong19931225@gmail.com

Afiq Hamzah
School of Electrical Engineering
Universiti Teknologi Malaysia
81310 Johor Bahru, Malaysia
mafiq@fke.utm.my

Shahrizal Rusli
School of Electrical Engineering
Universiti Teknologi Malaysia
81310 Johor Bahru, Malaysia
shahrizal@fke.utm.my

Nurul Ezaila Alias
School of Electrical Engineering
Universiti Teknologi Malaysia
81310 Johor Bahru, Malaysia
ezaila@utm.my

Cheng Siong Lim
School of Electrical Engineering
Universiti Teknologi Malaysia
81310 Johor Bahru, Malaysia
lcsiong@utm.my

Michael Loong Peng Tan*
School of Electrical Engineering
Universiti Teknologi Malaysia
81310 Johor Bahru, Malaysia
michael@utm.my

Abstract—Ballistic device performance of monolayer silicene nanoribbon (SiNR) field-effect transistors (FETs) is investigated in this paper. The electronic band structure of SiNR is calculated within the nearest neighbour tight-binding approximation. The top of the barrier ballistic transistor model is employed to compute the current-voltage characteristics of SiNR FETs. This theoretical model shows that the SiNR FET can achieve on-to-off current ratio up to 10^5, subthreshold swing of 65.12 mV/dec, and drain-induced barrier lowering of 44.44mV/V. The relationship between the drain current and the oxide thickness is also discussed. The findings show that silicene is suitable for future nanoelectronic applications.

Keywords— device modelling, silicene, ballistic transport, field-effect transistor, 2D material

I. Introduction

Two-dimensional materials have become an emerging "More than Moore" research topic as Moore's Law is approaching the fundamental limits [1]. Silicene is a monolayer of silicon (Si) atoms arranged in graphene-like (commonly known as honeycomb) lattice structure [2, 3]. Unlike other 2D materials, silicene is envisaged to be compatible with the Si fabrication technology in the semiconductor industry [4]. Moreover, silicene is one of the emerging research material for miniaturisation of transistors in the International Roadmap for Devices and Systems (IRDS) [5]. These suggest that investigation on silicene-based devices is important to certain extent in the nanoelectronic applications.

Although the fabrication of free-standing silicene has yet to be discovered [6], researchers have confirmed its existence through various theoretical calculations such as density functional theory (DFT) [7] and first-principles calculations [8]. Similar to electronic properties of graphene nanoribbons, the armchair SiNRs (ASiNRs) has larger finite bandgap than the zigzag SiNRs [9]. Hence, ASiNR is chosen as the channel material for the field-effect transistor in this paper. ASiNR with the nanoribbon width of 6 (denoted as 6-ASiNR hereafter) is chosen in this work to benchmark the results with published results from Ref. [10]. In Section II, the model of electronic band structure and transistor is described. The ballistic performance of SiNR FET is shown and discussed in Section III. Finally the conclusion is drawn in Section IV.

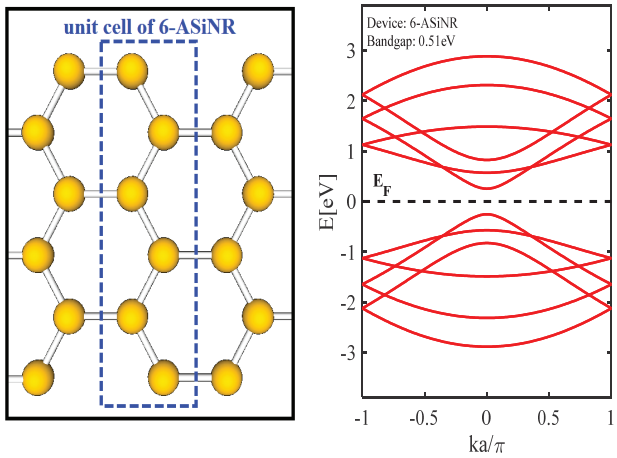
II. Model Implementation

A. Electronic band structure of silicene nanoribbons

The electronic band structure of 6-ASiNR is computed using the nearest neighbour tight-binding approach with the hopping integral between Si atoms, t_{Si-Si} of $-1.03\ eV$ [11] and Fermi energy level, E_F of $0\ eV$. In this work, 6-ASiNR is assumed to be in perfect planar honeycomb lattice structure. The Hamiltonian matrix of 6-ASiNR is computed based on [12]:

$$h(k) = \beta' e^{-ika} + \alpha + \beta e^{+ika}\,, \qquad (1)$$

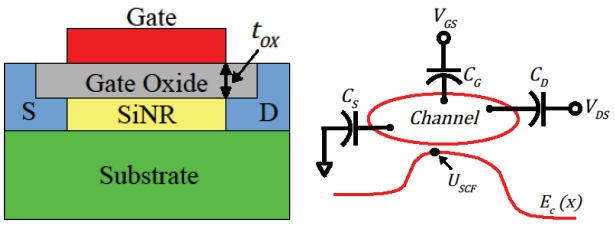
which is derived from the time-independent Schrödinger equation where α-matrix describes the interactions of atoms within the unit cells as shown in blue dotted box in **Fig. 1(a)** and the β-matrix describes the interactions among the unit cells. β' is the transverse matrix of β and a is the lattice constant of silicene where $a = 0.382\ nm$ [13]. The solution



(a) (b)

Fig. 1. (a) Schematic diagram of the 6-ASiNR. (b) Band structure of 6-ASiNR.

978-1-7281-5968-3/20/$31.00 ©2020 IEEE



(a) (b)

Fig. 2. (a) Structural model of the SiNR FET where t_{OX} is the oxide thickness. (b) Schematic diagram of the ballistic transistor model where C_D, C_S and C_G are the drain, source and gate capacitances respectively, V_{GS} is the gate voltage, V_{DS} is the drain voltage, $E_C(x)$ is the conduction band and U_{SCF} is self-consistent potential at the top of the barrier .

for eigenvalue problem [14]: $det\left|\left[h\left(\vec{k}\right)\right] - EI\right| = 0$ is employed to obtain energy eigenstates in order to plot the band structure of 6-ASiNR as depicted in **Fig. 1(b)**.

B. Device structure and model of transistor

Fig. 2(a) illustrates the structure of the SiNR FET. Silicon dioxide (SiO_2) with t_{OX} of 3 nm is used as the gate oxide. The current-voltage characteristics is evaluated by employing the 10 nm ballistic top-of-the barrier (ToB) transistor model [15] as depicted in **Fig. 2(b)**. The ToB transistor model has been widely used to predict the theoretical upper limit performance of various nanotransistors [16], while ignoring the scattering effects and off-state tunnelling leakage current [10].

The drain current is calculated numerically using the Landauer-Büttiker ballistic current transport equation [15]:

$$I_{DS} = \frac{q}{2}\int_{-\infty}^{+\infty} |v(E)|D(E)[f_S(E_S) - f_D(E_D)]\,dE\,, \qquad (2)$$

where $f_S(E_S)$ and $f_D(E_D)$ are source and drain Fermi functions respectively, q is the electric charge constant, $v(E)$ is the average carrier velocity and $D(E)$ is the density of states. The default values of capacitive couplings ($C_G/C_\Sigma = 0.870$ and $C_D/C_\Sigma = 0.033$) [15] is used in the present work, where C_Σ is the parallel combination of C_D, C_S and C_G. **Fig. 3** shows the numerical simulation flow chart for the ToB transistor model. In present work, MATLAB is used to perform calculations (by running modified Fettoy source code [17] from nanohub.org) and plot graphs.

III. Results and Discussions

The drain voltage, V_{DS} and gate voltage, V_{GS} are both swept from 0 V to 1 V. The transfer (I_{DS}-V_{GS}) characteristics curve as plotted in **Fig. 4(a)** is obtained by sweeping V_{GS} at a few fixed V_{DS}. On the other hand, the output (I_{DS}-V_{DS}) characteristics curve as plotted in **Fig. 4(b)** is obtained by sweeping V_{DS} at a few fixed V_{GS}. From the output and transfer characteristics curves, the device performance metrics of the 6-ASiNR FET are extracted, namely on-to-off current ratio (I_{ON}/I_{OFF}), subthreshold swing (SS), threshold voltage (V_T), and drain-induced barrier lowering ($DIBL$). I_{ON}/I_{OFF} and V_T are extracted from the characteristics curves, whereas SS [18] and $DIBL$ [19] are calculated using:

$$SS = \frac{\Delta V_{GS}}{\Delta log\, I_{DS}}, \qquad (3)$$

$$DIBL = \frac{\Delta V_T}{V_{DD} - 0.1}, \qquad (4)$$

where V_{DD} is the maximum V_{DS}. The computed device performance metrics are and tabulated in **TABLE I.** .

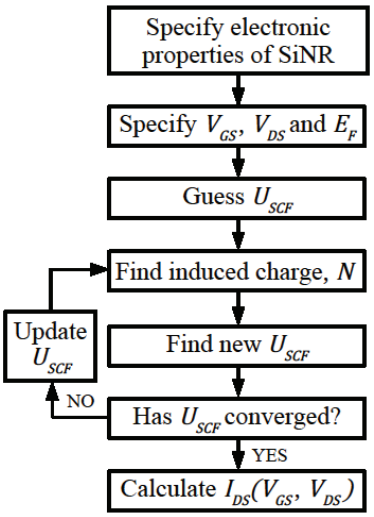
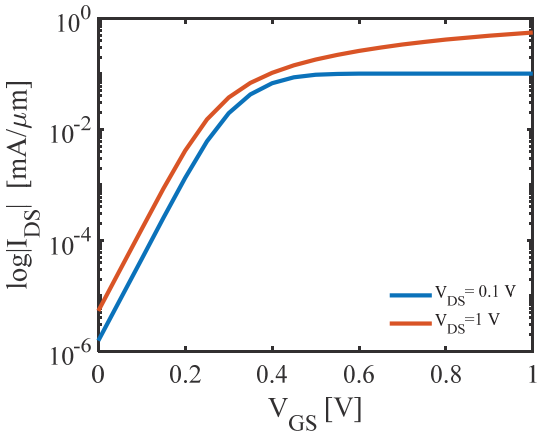
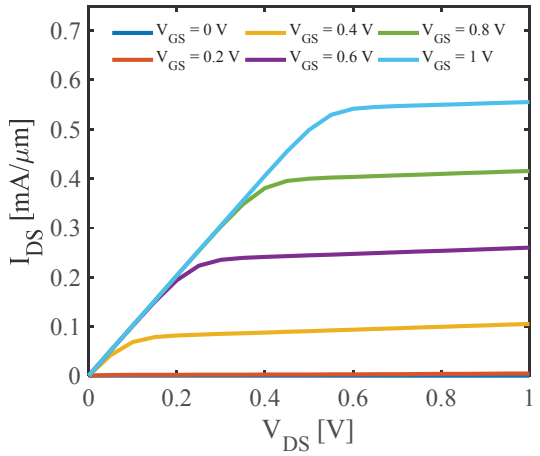


Fig. 3. Flow chart for the ToB transistor model simulation [20].



(a) I_{DS}-V_{GS} in semi logarithmic scale



(b) I_{DS}-V_{DS} in linear scale

Fig. 4. I-V characteristics of SiNR FET with gate oxide (SiO_2) of t_{OX} = 3 nm and 6-ASiNR as the conducting channel at room temperature.

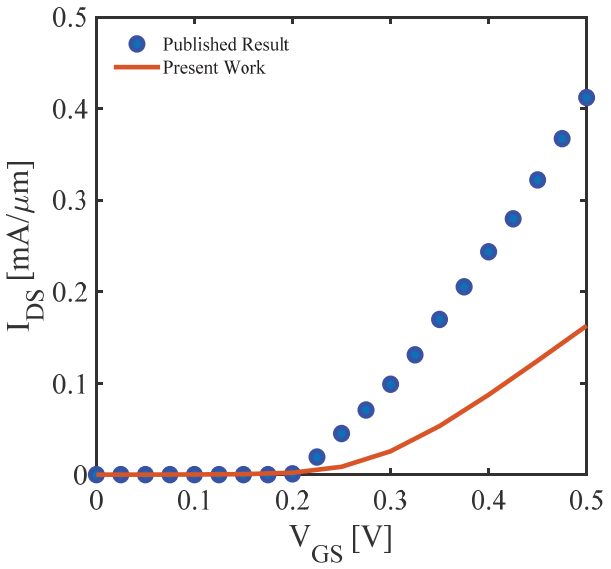


Fig. 5. Benchmark of the I_{DS}-V_{GS} characteristic curves (in linear scale) for 6-ASiNR FET with gate oxide (SiO_2) of $t_{OX} = 3\ nm$ at room temperature between the present work (solid line) and published results from Ref. [10] (dotted line).

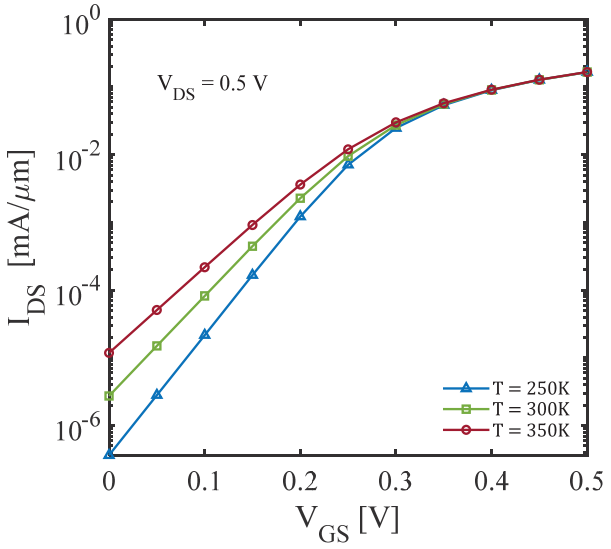


Fig. 6. Comparisons of the I_{DS} - V_{GS} characteristic curves (in semilogarithmic scale) of 6-ASiNR FET with gate oxide (SiO_2) thickness of 3.0 nm at $V_{DS} = 0.5\ V$ for $T = 250\ K$, $T = 300\ K$ (room temperature) and $T = 350\ K$.

TABLE I. DEVICE PERFORMANCE METRICS OF 6-ASINR FET UNDER BALLISTIC TRANSPORT AT ROOM TEMPERATURE

Device Metrics	Value
Oxide thickness (SiO_2), t_{OX}	3 nm
On-to-off current ratio (I_{ON}/I_{OFF})	~10^5
Threshold voltage, V_T (V)	0.25
Subthreshold swing, SS (mV/dec)	65.12
Drain-induced barrier lowering, $DIBL$ (mV/V)	44.44

Within the ballistic transport regime, the presented 6-ASiNR FET model has achieved close to ideal SS value ($60\ mV/dec$) and $DIBL$ of $44.44\ mV/V$ using the default capacitive coupling values. **Fig. 5** compares the I_{DS} - V_{GS} characteristic curves of 6-ASiNR FET from published results by Kaneko *et al.* [10] and present work. Both curves are computed within the ballistic transport region with SiO_2 ($t_{OX} = 3\ nm$) as the gate oxide at room temperature ($T = 300\ K$). It is found that the slope of I_{DS}-V_{GS} characteristic curve of present work is lower than that obtained by Kaneko *et al.*. This difference is possibly caused by the zero capacitive coupling assumptions in their work, while the present work uses the default non-zero capacitive coupling values set by Rahman *et al.* [15]. In addition to this difference, Kaneko *et al.* used effective mass assumption method where we use the NNTB to compute the electronic properties of 6-ASiNR. Despite the slight difference, similar trends of V_T and I_{DS}-V_{GS} characteristic curve are successfully computed in the present work, with lower on-current by benchmarking with the published result.

To gain more insights from the 6-ASiNR FET, I-V characteristic simulation is done at a lower temperature ($T = 250\ K$) and a higher temperature ($T = 350\ K$) as depicted in **Fig. 6**. The SS of the FET increases as the temperature of the 6-ASiNR channel increases. This phenomenon is also observed in conventional silicon FETs [21]. The relationship between oxide thicknesses and the transfer characteristic of 6-ASiNR FET is also investigated and plotted in **Fig. 7**. The transistor can achieve higher current with lower gate voltage when the oxide thickness is reduced. As the gate oxide is thinner, the FET can achieve higher I_{ON} at the same applied V_{GS}. This clearly shows that reduction in oxide thickness can improve the performance of the transistor. This finding is also observed in the published silicene FET simulation work using the non-equilibrium Green's function formalism [22]. However, the leakage current and oxide breakdown are neglected in this model. Hence, a more detailed model is required to cover the effects of non-ideal factors to the performance of the FETs.

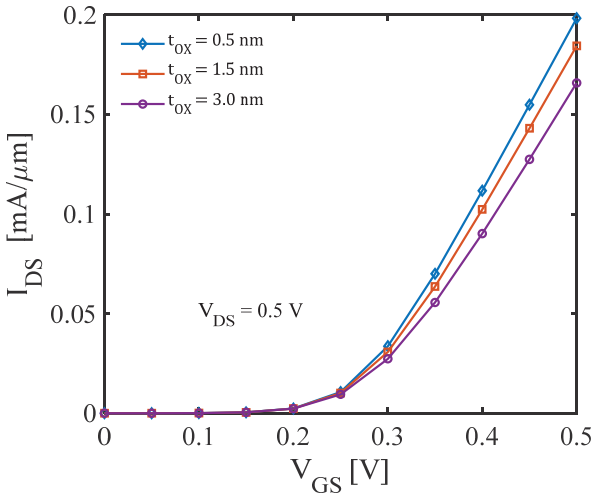


Fig. 7. Comparisons of the I_{DS} - V_{GS} characteristic curves (in linear scale) of 6-ASiNR FET for gate oxide (SiO_2) thicknesses of 0.5 nm, 1.5 nm and 3.0 nm at $V_{DS} = 0.5\ V$ and room temperature.

IV. Conclusion

This work presents the modelling and simulation of 6-ASiNR FETs within the ballistic transport regime. NNTB model is used to compute the band structure while the ToB model is used to simulate the I-V characteristics of the 6-ASiNR FETs. The theoretical transfer and output characteristics of 6-ASiNR FET shows that ASiNRs is suitable for future nanoelectronic applications. The trend of the relationship between temperature and *SS* of the 6-ASiNR FET model is verified with conventional FET. Moreover, it is also that oxide thickness is an important device parameter in the design of transistors. This work can be further extended by replacing the pristine ASiNR channel with bandgap engineered silicene nanosheets such as doped or defected silicene.

Acknowledgement

The authors acknowledge the Research Management Centre (RMC) at Universiti Teknologi Malaysia (UTM) for providing excellent support and conducive research environment. Mu Wen expresses his appreciation for the award of the UTM PhD Zamalah Scholarship from the School of Graduate Studies UTM. Michael Tan would like to acknowledge the financial support from the Fundamental Research Grant Scheme (FRGS) (Vote no.: R.J130000.7851.5F043) that enabled this research to proceed smoothly.

References

[1] M. Chhowalla, D. Jena, H. Zhang, Two-dimensional semiconductors for transistors, Nature Reviews Materials, 1 (2016) 16052.

[2] L. Lew Yan Voon, J. Zhu, U. Schwingenschlögl, Silicene: Recent theoretical advances, Applied Physics Reviews, 3 (2016) 040802.

[3] M.W. Chuan, K.L. Wong, A. Hamzah, S. Rusli, N.E. Alias, C.S. Lim, M.L.P. Tan, 2D Honeycomb Silicon: A Review on Theoretical Advances for Silicene Field-Effect Transistors, Current Nanoscience, In Press (2020).

[4] L. Tao, E. Cinquanta, D. Chiappe, C. Grazianetti, M. Fanciulli, M. Dubey, A. Molle, D. Akinwande, Silicene field-effect transistors operating at room temperature, Nature nanotechnology, 10 (2015) 227.

[5] IEEE, 'International Roadmap for Devices and Systems', 2018. [Online]. https://irds.ieee.org/images/files/pdf/2017/2017IRDS_ERM.pdf [Accessed: 14 February 2020]

[6] H. Oughaddou, H. Enriquez, M.R. Tchalala, H. Yildirim, A.J. Mayne, A. Bendounan, G. Dujardin, M.A. Ali, A. Kara, Silicene, a promising new 2D material, Prog. Surf. Sci., 90 (2015) 46-83.

[7] K. Takeda, K. Shiraishi, Theoretical possibility of stage corrugation in Si and Ge analogs of graphite, Physical Review B, 50 (1994) 14916.

[8] S. Cahangirov, M. Topsakal, E. Aktürk, H. Şahin, S. Ciraci, Two-and one-dimensional honeycomb structures of silicon and germanium, Phys. Rev. Lett., 102 (2009) 236804.

[9] Y. Ding, J. Ni, Electronic structures of silicon nanoribbons, Appl. Phys. Lett., 95 (2009) 083115.

[10] S. Kaneko, H. Tsuchiya, Y. Kamakura, N. Mori, M. Ogawa, Theoretical performance estimation of silicene, germanene, and graphene nanoribbon field-effect transistors under ballistic transport, Applied Physics Express, 7 (2014) 035102.

[11] N.J. Roome, J.D. Carey, Beyond graphene: stable elemental monolayers of silicene and germanene, ACS applied materials & interfaces, 6 (2014) 7743-7750.

[12] M.W. Chuan, K.L. Wong, A. Hamzah, M.A. Riyadi, N.E. Alias, M.L.P. Tan, Electronic properties of silicene nanoribbons using tight-binding approach, in: 2019 International Symposium on Electronics and Smart Devices (ISESD), IEEE, 2019, pp. 1-4.

[13] L. Lew Yan Voon, E. Sandberg, R. Aga, A. Farajian, Hydrogen compounds of group-IV nanosheets, Appl. Phys. Lett., 97 (2010) 163114.

[14] M.W. Chuan, K.L. Wong, A. Hamzah, S. Rusli, N.E. Alias, C.S. Lim, M.L.P. Tan, Electronic properties and carrier transport properties of low-dimensional aluminium doped silicene nanostructure, Physica E: Low-dimensional Systems and Nanostructures, 116 (2020) 113731.

[15] A. Rahman, J. Guo, S. Datta, M.S. Lundstrom, Theory of ballistic nanotransistors, IEEE Trans. Electron Devices, 50 (2003) 1853-1864.

[16] M.W. Chuan, K.L. Wong, A. Hamzah, S. Rusli, N.E. Alias, C.S. Lim, M.L.P. Tan, A review of the top of the barrier nanotransistor models for semiconductor nanomaterials, Superlattices Microstruct., (2020) 106429.

[17] A. Rahman, J. Wang, J. Guo, M.S. Hasan, Y. Liu, A. Matsudaira, S.S. Ahmed, S. Datta, M. Lundstrom, FETToy, in, 2011.

[18] A. Nazari, R. Faez, H. Shamloo, Modeling comparison of graphene nanoribbon field effect transistors with single vacancy defect, Superlattices Microstruct., 97 (2016) 28-45.

[19] M. Lundstrom, J.-H. Rhew, A Landauer approach to nanoscale MOSFETs, Journal of Computational Electronics, 1 (2002) 481-489.

[20] D. Supriyo, Lessons From Nanoelectronics: A New Perspective On Transport -Part A: Basic Concepts, World Scientific, 2017.

[21] J. Zhang, J. Trommer, W.M. Weber, P.-E. Gaillardon, G. De Micheli, On temperature dependency of steep subthreshold slope in dual-independent-gate FinFET, IEEE Journal of the Electron Devices Society, 3 (2015) 452-456.

[22] N. Patel, S. Choudhary, Current saturation and kink effect in zero-bandgap double-gate silicene field-effect transistors, Superlattices Microstruct., 110 (2017) 155-161.