Electrical characterization of n-type cylindrical gate all around nanowire junctionless transistor with SiO2 and high-k dielectrics

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Abstract*— In this work, the electrical characteristics of n-type cylindrical gate all around (GAA) nanowire junctionless transistors (NWJLT) of different gate oxides are investigated and analyzed. Silicon dioxide (SiO_2) and two high-k dielectrics which are silicon nitride (Si_3N_4) and hafnium dioxide (HfO_2) were used in this study. GAANWJLT of different gate lengths (L_G) and nanowire diameter (d_{NW}) were simulated, compared and analyzed to obtain the most optimum device. SDE and Sdevice tools of Sentaurus TCAD were used to simulate and extract the electrical properties of the proposed devices. It was found that GAANWJLT with high-k dielectrics significantly exhibits better electrical properties than with SiO_2 due to increase in internal fringe capacitance of the gate dielectric layer. SCEs were considerably improved as the gate-to-channel capacitance reduced. It was found that, for L_G of 7 nm and d_{NW} of 6 nm GAANWJLT, device with HfO_2 exhibits better electrical properties with more than 2-fold elevated in I_{ON}/I_{OFF} ratio and about 15% improvement in SS than the conventional device with SiO_2. It proves that GAANWJLT with HfO_2 exhibits the most optimum electrical characteristics among the three devices, hence the best alternative to improve SCEs as well as to increase the switching speed of the transistor devices.

Keywords—junctionless transistor, nanowire, gate capacitance, high-k, dielectric constant

I. INTRODUCTION

Short channel effects (SCEs) are the main concerns in CMOS technology scaling below 10nm [1]. Junctionless field effect transistor (JLFET) is consider the most optimum solution to overcome the SCEs due to the absence of the metallurgical junctions and less thermal budget [2]. High leakage current and SCEs such as Drain Induced Barrier Lowering (DIBL), velocity saturation, hot carrier etc. are remarkably reducing the electrical performance of JLFET. JLFET is a thin highly doped semiconductor device in which the gate electrode controls the flow of current from source to drain [3]. The channel of the device has the same doping concentration that can be fully depleted to turn off the device.

Gate oxide controls the flow of electrons in the channel. The electrical properties of the gate oxide are critical to the realization of the conductive channel region below the gate [4]. Silicon dioxide (SiO_2) has been used as gate dielectric material in many JLFET researches. As the size of transistor keep decreasing in order to follow the Moore's law, thickness of SiO_2 has gradually decreased so as to increase the gate capacitance as well as the drive current to increase the device performance. As the oxide thickness (t_{ox}) reduce below 2 nm, leakage currents (I_{OFF}) significantly increase due to the tunnelling of electrons. This results in high power consumption and poor device reliability. To increase gate capacitance without the associated leakage effects, high-*k* material is an alternative to replace the SiO_2 [5]. In this work, three GAANWJLTs of different gate lengths (L_G) and nanowire diameter (d_{NW}) were designed and simulated using SDE tools of Sentaurus TCAD. The first device with SiO_2 as a gate dielectric layer, the second device with Si_3N_4 as a gate dielectric layer and the third device with HfO_2 as a gate dielectric layer. Electrical characteristic of each device were extracted using the Sdevice tools of the Sentaurus TCAD. The electrical characteristics of the 3 devices were compared and analyzed to obtain the most optimized device.

II. PREVIOUS WORK

Previously, many scholars have contributed tremendously on the NWJLT device by using different methods. Their work indicated that to overcome the SCEs, NWJLT is the utmost alternative to speed up the switching of the devices. The conduction of current in NWJLT is a bulk phenomenon which normally conducts during the on-state when bias is applied across source and drain. The gate voltage induces depletion region in the channel to turn off the current [6]. Heavily doped junctionless transistor uses the idea of tunneling by narrowing the barrier between source and channel of the device to switch the device ON and OFF [7]. Leakage current (I_{OFF}) can be significantly reduced due to the small cross-section of bulk device that ensured full depletion of electrons in the channel junction. The on-state current can be increase in NJT device

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due to the high doping concentration (N_D) used in the design to allow for high current flow in the on-state. DIBL and subthreshold slope were also improved [8]. HfO_2 demonstrated an improved I_{ON}, I_{OFF}, DIBL and subthreshold slope when used as gate oxide due to the high gate capacitance, small d_{NW} and high N_D [9].

High-k dielectric used as a spacer in double gate junctionless transistor, can improved the OFF-state current by more than one order of magnitude thus enhanced the scaling of the device [10]. Even though, the ON-state current can be slightly affected by increasing dielectric constant (k) of the spacer, but marginally decreases with spacer width. Subthreshold Slope and DIBL decreases with increasing spacer dielectric constant of a spacer (k_{sp}) for SiO_2, Al_2O_3 and HfO_2 due to the enhanced fringing electric fields through the spacer deplete the silicon beyond the gate edges for high-k spacer in the subthreshold region. SiO_2 gate oxide has the lowest value of SS and DIBL for all spacer dielectrics considered [10].

The gate capacitance (C_{gg}) of junctionless transistor depends on the N_D, fin width (W_{fin}) and fin height (H_{fin}) [11] as in Eq. (1) and (2). C_{gg} of NJT is lower because the channel is buried in the center of the nanowire and the series relation between the gate oxide capacitance (C_{ox}) and the depletion capacitance decreases the overall C_{gg} [12]. The minimum gate capacitance ($C_{gg\ min}$) can be calculated using the equation in [11].

$$C_{gg.min} = \frac{C_{ox} C_{si.min}}{C_{ox} + C_{si.min}} \quad (1)$$

Where C_{ox} is the gate oxide capacitance and $C_{si,min}$ is the minimum silicon capacitance. $C_{si,min}$ can be computed using:

$$C_{si.min} = \frac{\varepsilon_{si}}{d_{max}} \quad (2)$$

d_{max} is the maximum depletion region depth.

Junctionless double gate tunnel device improved gate control over the channel and provides ideal subthreshold swing and better I_{ON}/I_{OFF} current ratio. Using SiO_2 as gate oxide material leads to high leakage current and direct tunneling of electrons. Therefore, replacing SiO_2 with a highk material such as HfO_2, Al_2O_3, ZrO_2 improve SCEs, leakage current, high density and low energy consumption [13].

III. SIMULATION SETUP

GAANWJLT devices of different gate oxide materials, L_G and d_{NW} were designed and simulated using SDE tools of Sentaurus TCAD. The electrical characteristics of the devices were extracted using Sdevice tools of TCAD for gate voltage of 1V and the drain to source voltage at linear region, V_{DS} of 0.05V. The metal gate work function (ϕ_m) of 4.8 eV was used in all the devices as shown in table 1. High uniform channel doping concentration of 10^{19} cm^{-3} was used from source to drain. The L_G is 10 nm. Philips unified mobility and Lombardi mobility models were used to consider field and doping dependent mobility degradation. The dominant generation and recombination process in silicon and other indirect energy band gap materials was Shockley–Read–Hall (SRH).

Fig. 1 shows the uniform doping concentration of GAANWJLT from source to drain across the channel. the High gate work function was use to achieve a suitable subthreshold voltage value. Metal was used as a gate material to reduce the gate resistance as well as diminish the height of energy barrier.

Table 1 Device Parameters and Dimensions

Parameter	SiO_2	Si_3N_4	HfO_2
Structure	n-type cylindrical	n-type cylindrical	n-type cylindrical
N_D	$10^{19}cm^{-3}$	$10^{17}cm^{-3}$	$10^{17}cm^{-3}$
Nanowire diameter (dNW)	6-10nm	6-10nm	6-10nm
Oxide thickness (t_{ox})	1nm	1nm	1nm
Gate workfunction (ϕ_m)	4.8eV	4.8eV	4.8eV
Gate length (L_G)	7-50nm	7-50nm	7-50nm
Length of S/D (LSD)	10nm	10nm	10nm
Length of S/D contact (LSDC)	10nm	10nm	10nm

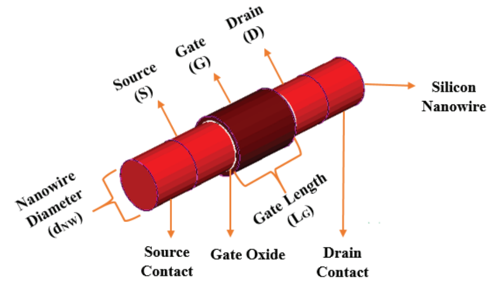

Fig.1 3D cross-sectional view of GAANWJLT

IV. RESULTS AND DISCUSSION

Due to the high doping concentration in the channel and small nanowire diameter of d_{NW} = 6nm of the devices, full depletion of the heavily doped channel was achieved resulting in low leakage current for L_G = 7 nm, d_{NW} = 6 nm and t_{ox} = 1 nm as shown in Fig. 2.

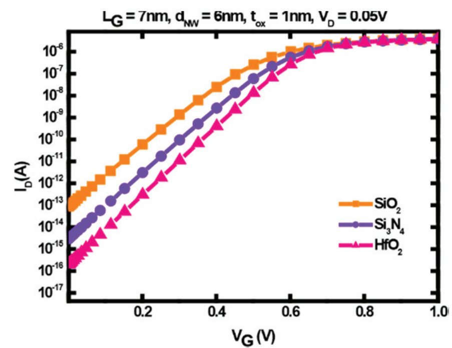

Fig.2 I-V characteristics of GAANWJLT for three different gate oxides.

Low leakage current was experienced in all the three devices for short L_G. The leakage became high when the L_G increases. GAANWJLT with HfO_2 exhibits most optimized leakage current of 2.37 x 10^{-16}A compared to SiO_2 and Si_3N_4 having 3.57 x 10^{-14}A and 2.28 x 10^{-15}A respectively for L_G of 7nm and d_{NW} of 6nm. The highest leakage current demonstrated by GAANWJLT with SiO_2 was due to the high tunnelling of electrons in the device when the t_{ox} was reduced to 1nm.

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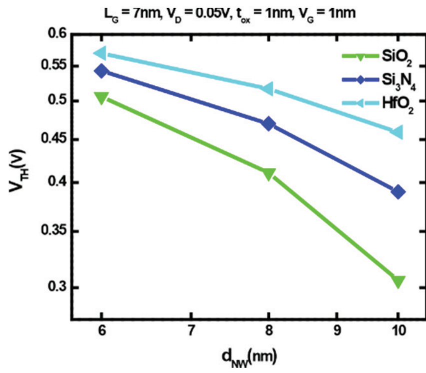

Fig.3 Impact of d_{NW} variation on V_{TH} for the three different gate oxides at V_D of 0.05 V.

Oxide thickness (t_{ox}) of high-k dielectrics has a great influence on the threshold voltage. Effect of high tunneling current can be eliminated if the thickness of the dielectrics is large [14]. Fig. 3 shows the variation of d_{NW} against the threshold voltage for L_G of 7 nm. V_{TH} of SiO_2 is 0.506 V while Si_3N_4 is 0.543 V. V_{TH} decreases with an increase in d_{NW}.

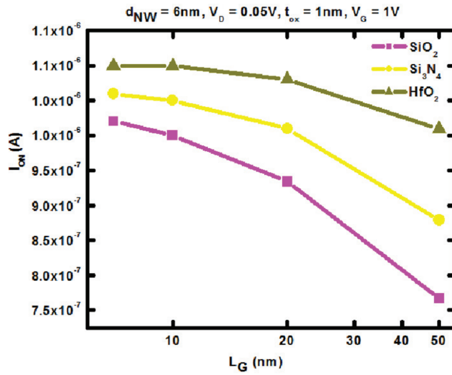

Fig. 4 I_{ON} against L_G for the three different gate oxides at constant d_{NW} of 6 nm.

High-ON state current was observed in all the three devices due heavy doping concentration used in the devices. GAANWJLT with HfO_2 exhibits the most optimum I_{ON} among the three devices because when HfO_2 make contact with n-type material, the gate capacitance of the device will improve and the leakage current will have decreased allowing a large ON-state current to flow. For L_G of 10nm, the I_{ON} for HfO_2 and SiO_2 are 1.10 x 10^{-6}A and 1.00 x 10^{-6}A respectively. I_{ON} decreases as the L_G increases at constant diameter as shown in Fig.4 due decrease in the mobility of electrons in the device.

Fig. 5 shows the impact of variation of L_G on the DIBL for d_{NW} of 6nm. It was observed that for small L_G of 7nm, all the three devices demonstrated small DIBL. The rate decreases further as the L_G increases. GAANWJLT with HfO_2 device has the lowest DIBL of 11.47 mV/V than GAANWJLT with SiO_2 which has 54.74 mV/V. Fig. 4 displays that GAANWJLT with HfO_2 has a limited value when the L_G exceeded 33nm. Beyond 33nm, the DIBL tends to increase instead of to decrease further.

It is known that the oxide thickness of high-k dielectrics demonstrated higher fringing field effect from the gate to source and drain region causes the gate to have less control of the channel, hence reduced the subthreshold slope [15].

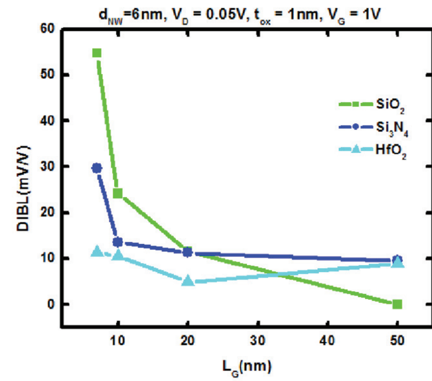

Fig. 5 Impact of variation L_G on DIBL at d_{NW} of 6nm at V_D of 0.05V.

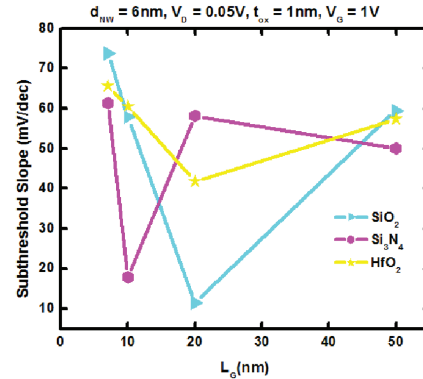

Fig. 6 Impact of L_G variation on Subthreshold Slope for constant d_{NW} of 6nm at V_D of 0.05V for the three different gate oxides.

Fig. 6 shows the impact of variation of L_G on the Subthreshold slope (SS). The SS trend for GAANWJLT with SiO_2 seems different with the other 2 devices. For L_G of 7 nm, the SS for Si_3N_4 and HfO_2 are significantly reduced to 61.34 mV/dec and 62.7 mV/dec, respectively, which are slightly higher than that of the theoretical limit, 60 mV/dec. Meanwhile the SS of SiO_2 was found to be 73.82 mV/dec. Fig. 6 proves that all the three devices reached their limits as the L_G increases. SS of GAANWJLT with Si_3N_4 was observed to be 17.85mV/dec for L_G of 10nm. As L_G increases to 20nm, the SS increases to 58.17 mV/dec and decreases again to 50.10 mV/dec when L_G increases further to 50 nm. Similarly, the minimum SS of GAANWJLT with SiO_2 and HfO_2 occurs when L_G is 20 nm as 11.49 mV/dec and 41.8 mV/dec respectively. However, the values instead of to decrease further, it increases to 59.49 mV/dec and 57.44 mV/dec respectively.

Nanowire diameter has a great effect on the SCEs such as on DIBL and subthreshold slope. It can be shown in Fig. 7 that small d_{NW} enhanced SCEs compared to the larger d_{NW}. For d_{NW} of 8 nm, GAANWJLT with HfO_2 demonstrated the lowest DIBL and SS of 30.53 mV/V and 64.19 mV/dec for L_G of 7 nm. Similarly, the SCEs becomes worse when the d_{NW} was increased further. Using high-k as gate dielectric slightly increased the surface electrostatic potential in the channel region near source region [14]. This leads to the high injection of carriers from source to channel, hence improving the performance of the device. In Fig. 8, the two high-k materials show higher ON-state-to-OFF-state current ratio than the SiO_2 gate oxide device. GAANWJLT with HfO_2 significantly improved I_{ON}/I_{OFF} up to 4.64 x 10^9 while GAANWJLT with SiO_2 has 2.86 x 10^7 for L_G of 7 nm.

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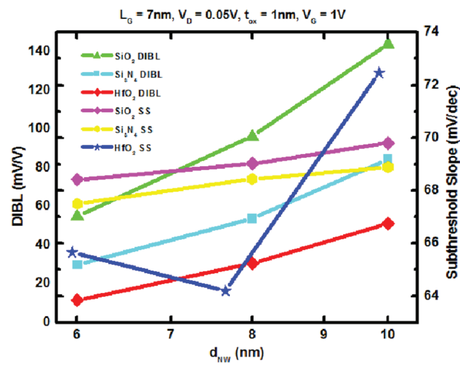

Fig. 7 Effects of d_{NW} variation on DIBL and Subthreshold slope for L_G of 7nm for the three gate oxides.

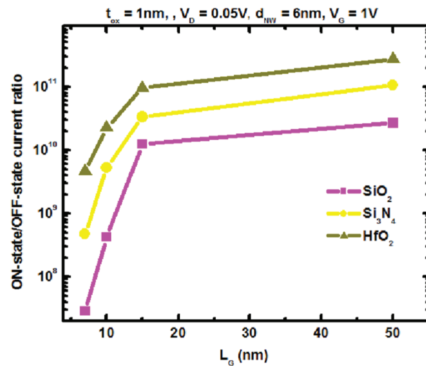

Fig. 8 ON-state-to-OFF-state current ratio for different L_G with constant d_{NW} of 6nm of the three different gate oxides.

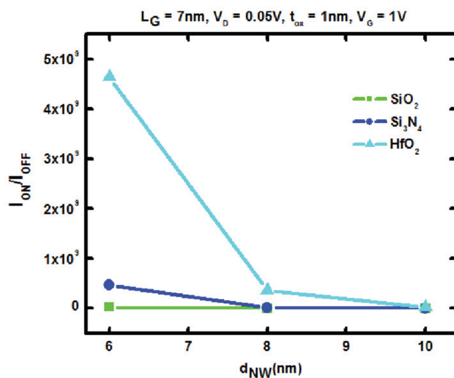

Fig. 9 Impact of d_{NW} variation on ON-state-to-OFF-state current ratio for L_G of 7 nm of the three different gate oxides.

Similar, the switching speed of the 3 devices decrease when d_{NW} increases to 10 nm. I_{ON}/I_{OFF} decreases with an increase in d_{NW} as shown in Fig. 9. For d_{NW} of 8 nm, GAANWJLT with HfO_2 exhibits most optimal I_{ON}/I_{OFF} of 3.7 x 10^9 than GAANWJLT with SiO_2 which has 2.867 x 10^5.

V. CONCLUSION

In this study, GAANWJLT device SiO_2 dielectric layer and two others GAANWJLTs with high-k dielectrics for different L_G and d_{NW} were successfully designed and simulated. GAANWJLT with Si_3N_4 and HfO_2 are the high-k dielectric used in this study. Electrical characteristics of all the devices were compared and analysed. The simulation results show that GAANWJLT with high-k dielectric exhibits the most optimal electrical characteristics than the conventional SiO_2. V_{TH}, DIBL, SS and I_{OFF} were significantly improved by using high-k dielectrics than using SiO_2 gate oxide. The I_{ON} and the I_{ON}/I_{OFF} ratio were considerably increased due to the increases in internal fringe capacitance of the gate oxide. This leads to the faster switching speed of the device.

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REFERENCES

[1] L.-C. Chen et al., "The physical analysis on electrical junction of junctionless FET," AIP Advances, vol. 7, no. 2, p. 025301, 2017.

[2] S. Sahay and M. J. Kumar, "Nanotube junctionless FET: Proposal, design, and investigation," IEEE Transactions on Electron Devices, vol. 64, no. 4, pp. 1851-1856, 2017.

[3] E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, "Theory of the junctionless nanowire FET," IEEE Transactions on Electron Devices, vol. 58, no. 9, pp. 2903-2910, 2011.

[4] M. A. Riyadi, I. D. Sukawati, and T. Prakoso, "Influence of Gate Material and Process on Junctionless FET Subthreshold Performance," International Journal of Electrical & Computer Engineering (2088-8708), vol. 6, no. 2, 2016.

[5] S. Sahay and M. J. Kumar, "Insight into lateral band-to-bandtunneling in nanowire junctionless FETs," IEEE Transactions on Electron Devices, vol. 63, no. 10, pp. 4138-4142, 2016.

[6] S. Das and S. Kundu, "A Review on Junctionless Transistor-A Prospective sub-10nm Logic Device," Advanced Research in Electrical and Electronic Engineering, vol. 1, no. 3, pp. 98-102, 2014.

[7] B. Ghosh, P. Bal, and P. Mondal, "A junctionless tunnel field effect transistor with low subthreshold slope," Journal of Computational Electronics, vol. 12, no. 3, pp. 428-436, 2013.

[8] J.-P. Colinge et al., "Junctionless nanowire transistor (JNT): Properties and design guidelines," Solid-State Electronics, vol. 65, pp. 33-37, 2011.

[9] A. Al Sayem, Y. Arafat, and M. M. Rahman, "Effect of high kdielectric as gate oxide on short channel effects of junction-less transistor," in 2013 2nd International Conference on Advances in Electrical Engineering (ICAEE), 2013, pp. 115-118: IEEE.

[10] R. K. Baruah and R. P. Paily, "Impact of high-k spacer on device performance of a junctionles transistor," Journal of Computational Electronics, vol. 12, no. 1, pp. 14-19, 2013.

[11] G. Mariniello, R. T. Doria, M. de Souza, M. A. Pavanello, and R. D. Trevisoli, "Analysis of gate capacitance of n-type junctionless transistors using three-dimensional device simulations," in 2012 8th International Caribbean Conference on Devices, Circuits and Systems (ICCDCS), 2012, pp. 1-4: IEEE.

[12] J.-P. Colinge et al., "A simulation comparison between junctionless and inversion-mode MuGFETs," ECS Transactions, vol. 35, no. 5, pp. 63-72, 2011.

[13] A. Ali, D. Seo, and I. H. Cho, "Investigation of Junction-less Tunneling Field Effect Transistor (JL-TFET) with Floating Gate," JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, vol. 17, no. 1, pp. 156-161, 2017.

[14] L. Fairouz, R. Djamil, G. Kamel, and Z. Mourad, "Channel Length Effect on Subthreshold Characteristics of Junctionless Trial Material Cylindrical Surrounding-Gate MOSFETs with High-k Gate Dielectrics," 2019.

[15] S. Mah, I. Ahmad, P. J. Ker, and N. F. ZA, "High-k Dielectric Thickness and Halo Implant on Threshold Voltage Control," Journal of Telecommunication, Electronic and Computer Engineering (JTEC), vol. 10, no. 2-6, pp. 1-5, 2018.

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