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Reliability Analysis Of Gate-All-Around Floating Gate (GAA-FG) With Variable Oxide Thickness For Flash Memory Cell

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Abstract

In this work, a concept of tunnel barrier engineering using Variable Oxide Thickness (VARIOT) of low-k/high-k stack is implemented in Gate-All-Around Floating Gate (GAA-FG) memory cell to reduce P/E operational voltage, improve the efficiency of data retention after 10 years and endurance after 10^4 of P/E cycles. This work begins with the VARIOT optimization of five high-k dielectric materials which are ZrO_2, HfO_2, La_2O_3, Y_2O_3 and Al_2O_3 in which these high-k dielectrics can be embedded onto low-k dielectric layer which is SiO_2. The impact of the proposed structure on the device characteristic is analyzed through simulated transient performances of the GAA-FG memory cell with optimized parameters are accessed to offset the trade-off between P/E characteristics and the device reliability including data retention and endurance.

(Keywords: High-k, P/E, Retention, Endurance, Flash memory)

Introduction

3-D floating gate flash NAND technology has been extensively manufactured in which offers bigger data storage [1]. One of it is vertical stack of GAA-FG structure. The GAA-FG has been downscaled for better P/E process and transient performance [2]. However, there have been some reports suggest that the device scaling faced severe challenges due to the reliability concerns and practical physical limitations such as capacitive coupling of FGs along the string line of conventional-FG (C-FG) 3-D NAND which affected the P/E operational voltage and speed degradations [3]. Thus, the floating gate potential is reduced by the same factor the C-FG cell needs higher P/E voltages to yield wide memory window [1]. To overcome this limitation, the tunnel barrier engineering (TBE) is incorporated in GAA-FG memory cell for high tunneling current which led to the faster P/E operation. VARIOT stack technology has high field sensitivity than single SiO_2 layer resulted in low P/E voltage, shorter P/E operation time and less leakage in long-term retention time [4]. Although the effect of incorporating the high-k dielectric material into the tunnel oxide layer is proven better; serious attention has been paid to the optimization of high-k dielectric materials based on their characteristics and suitability [5]. An attempt has been made to reduce P/E voltages by using triangular GAA structure [6]. To offset the P/E and reliability characteristics, a validation study is conducted between fabricated triangular GAA-FG [6] and cylindrical GAA-FG [3] memory cell to compare the transfer characteristic and transient performances of both GAA-FG memory cell. Therefore, in this paper, an optimization work has been done to determine the best stacking layer between low-k/high-k, which focused on the memory performances of the cylindrical GAA-FG memory cell. Also, the device and transient performances of GAA-FG memory cell are investigated by examining the tunneling current, P/E operation and device reliability included data retention and endurance.

Simulation Details

The simulation of GAA-FG memory cell is carried out by using 3-D ATLAS Simulator. By implementing the engineered tunnel stack of SiO_2 embedded with high-k materials of ZrO_2, HfO_2, La_2O_3, Y_2O_3 and Al_2O_3 to the GAA-FG memory cell, the device and transient performances are accessed. The simulation flow work is divided into two parts; 1) VARIOT optimization and 2) variability test of the low-k SiO_2 tunnel layer. The purpose of VARIOT optimization is to find the best combination of low-k/high-k stack and extract the Fowler-Nordheim (F-N) coefficients. Table 1 lists the dielectric parameters need to be defined in the Technology Computer Aided-Design (TCAD) Silvaco ATLAS for VARIOT optimization work. Then, to determine flash memory constraints. The memory constraints are needed to a domain down-selection in determining the optimum EOT and low-k SiO_2 tunnel layer. Then, the best low-k/high-k combination is determined based on the gate voltage during program, read-disturb and retention conditions as given in Table 2. After these two things are clarified, the simulation of 3-D of GAA-FG

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device structure was conducted for simplicity only to study the electrical behavior of the asymmetric VARIOT stacks of different high-k dielectric materials. For fair comparison of P/E efficiency and reliability characteristics (data retention and data endurance), the simulation of GAA-FG with the best stacking layer which is SiO_2/La_2O_3 tunnel barrier is performed and plotted. The structure of GAA-FG with SiO_2/La_2O_3 tunnel stack is shown in Fig.1 meanwhile its device parameters are stated in Table 3. From the table, the physical thickness of the low-k and high-k oxide thickness can be calculated using Eq. (1).

$$EOT = T_{ox} + (3.9/\varepsilon_{hk})T_{hk} \quad (1)$$

As for P/E process, low operational voltage is applied (10/-12V) to compare the operational speed and memory window of the P/E characteristics. Then, data retention simulation is performed by applying gate stress 3V/-3V for program/erase state for 10^4 times then the data is extrapolated by using Power's Law model until 10 years. Meanwhile, the data endurance is done by simulation of the GAA-FG memory cell device up to 10^4 of P/E cycles. Finally, a comparative analysis is made between GAA-FG cell with SiO_2/La_2O_3 tunnel barrier and single barrier, SiO_2 for the device and transient performances.

Results and Discussion

For the VARIOT optimization result, any value of T_{ox} that can endure V_g>3.6V during read-disturb and V_g>|-1.5V| during retention are extracted. Based on the dashed-lines, two permissible ranges of T_{ox} that satisfies both constraints (read-disturb and retention) are found and combined with Vg-T_{ox} of program constraint, the minimum EOT for each VARIOT combinations are determined. Under the retention constraint, all the VARIOT combinations under study have satisfied the retention constraint EOT=4nm as shown in Fig. 2(a). However, under a more restrictive constraint of the read-disturb (refer Fig. 2(b), only SiO_2/La_2O_3 able to retain its minimum EOT at 4nm and as the rest are at 5nm (SiO_2/Al_2O_3), 6nm ($SiO_2/HfO_2$and SiO_2/ZrO_2) and 8nm (SiO_2/Y_2O_3). Referring to their minimum EOT, it was found that the combination of SiO2/La2O3 and SiO_2/Al_2O_3 have the thinnest T_{ox} = 1nm. However, SiO_2/La_2O_3 has the upper hand due to its lowest EOT. Therefore, the F-N coefficients are extracted by plotting the F-N plot (J_g/E^2 versus 1/E).

Further investigation on the memory performance, a set of simulation to analyze the data retention and endurability of the proposed device structure have been done. Fig. 3 shows the comparison of P/E characteristics for GAA-FG with SiO_2/La_2O_3 tunnel stack and experimental data of GAA-FG cell for P/E operational time of 10ms. It shows that GAA-FG with SiO_2/La_2O_3 tunnel stack has wider memory window. It shows that engineered tunnel stack gives significant impact in improving the P/E efficiency and more electrons can be stored in that memory cell. Retention characteristic of GAA-FG cell is shown in Fig. 4 under gate stress (3/-3V). Engineered tunnel stack (SiO_2/La_2O_3) achieved larger V_{th} shift compared to single stack, SiO_2. Wider memory window can be obtained after 10 years of extrapolation although SiO_2/La_2O_3 tunnel stack steeper threshold shift compared to single layer, SiO_2. In addition, the endurance of the GAA-FG cell is shown in Fig. 5 where it is performed by applying constant P/E cycle, which indicated by the plotting of V_{th} shift versus P/E cycles. In the figure both stacks show obvious degradation after 10^3 cycles. It is a sign that stress still affected in both stacks as there is an obvious shift after 10^3 of P/E cycles.

Conclusion

In summary, this paper presents the optimized low-k/high-k stacking layer which focused on the memory performances of the cylindrical GAA-FG memory cell. The characterization of GAA-FG with engineered tunnel stack (SiO_2/La_2O_3). As compared to the GAA-FG without tunnel barrier engineering (TBE), the proposed device exhibits faster P/E operational speed which required lower operational voltage to yield wider threshold voltage shift. In addition, the retention and endurance of GAA-FG with SiO_2/La_2O_3 tunnel stack shows 5% and 16% of data loss indicating that SiO_2/La_2O_3 tunnel barrier has become a promising candidate to improve P/E efficiency and device reliability.

Acknowledgments

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Table 1: Dielectric parameters need in the simulation for different materials

Dielectric Parameters	HfO_2	ZrO_2	Al_2O_3	La_2O_3	Y_2O_3	SiO_2
Barrier Height, Φ_B(eV)	1.5	1.4	2.8	2.3	1.6	3.2
Dielectric Constant, ϵ_r	19	25	9.6	27	25	3.9
Electron Affinity, χ(eV)	2.7	2.8	1.3	1.9	2.4	1.0
Band Gap, E_G (eV)	6.0	5.8	8.8	6.0	6.0	9.0
Effective Mass, $m*/m_0$	0.2	0.2	0.3	0.25	0.25	0.5

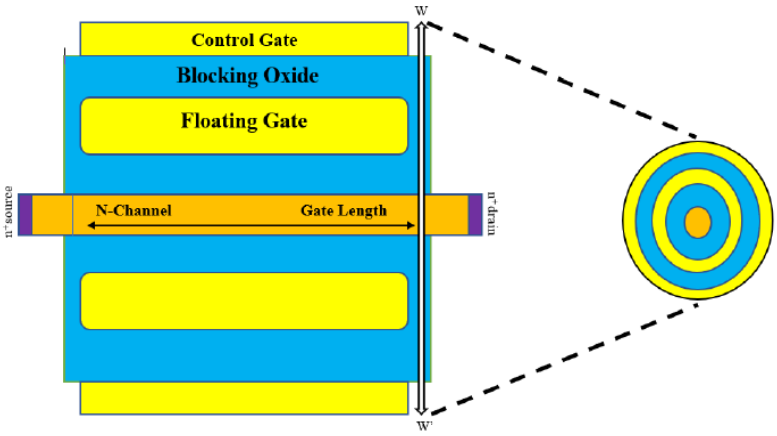

Fig. 1. Cross-section of 3-D GAA-FG with SiO_2/La_2O_3 tunnel stack. The physical thickness for tunnel stack is 22nm where SiO_2 layer is 1nm.

Table 2: Flash Memory Constraints

Flash Memory Constraints	Dimension
Tolerable read-disturb current density (A/cm^2)	< ~ 4 x 10^{-11} at around 3.6V
Tolerable retention current density(A/cm^2)	< 10^{-16} at around -1.5V
Tolerable programming current density(A/cm^2)	3 x 10^{-2}
Endurance	> 10^4 P/E cycles

Table 3: GAA-FG parameters used in the simulation

Device Parameter[3]		**Dimension**
Area width, A_w (cm^2)		1.2 x 10^{-12}
Area gate, A_{Gate} (cm^2)		1.55 x 10^{-10}
Gate Length, L_G (nm)		400
Blocking Oxide, T_{IPD} (nm)		20
FG thickness, T_{FG} (nm)		25
Body Doping (cm^{-2})		1 x 10^{19}
S/D Doping (cm^{-2})		1 x 10^{19}
Oxide Charges, Q_{ox} (cm^{-2})		-3.6 x 10^{12}
Optimized Parameter		**Dimension**
Tunnel Oxide, T_{tun} (nm)	The low-k oxide layer, T_{ox}	1
	The high-k oxide layer, T_{hk}	21

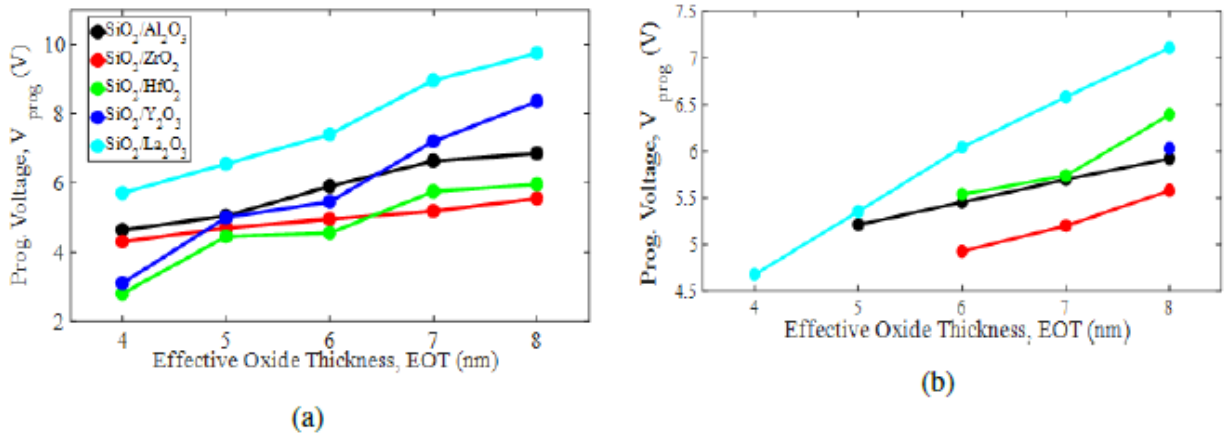

Fig. 2. Program Voltage, Vprog for each EOT of all VARIOT stack (a) Retention constraint > |-1.5V| (b) Read Disturb Constraint > 3.6V

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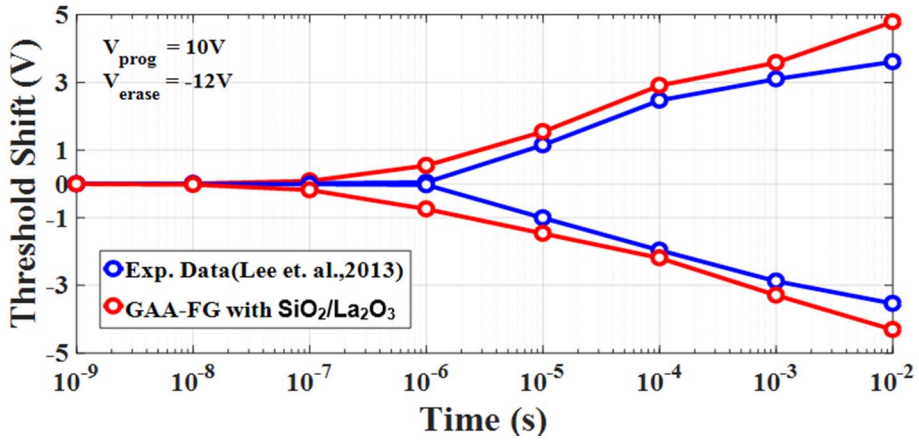

Fig. 3. Threshold voltage shift of GAA-FG for 10/-12V operational voltage. Engineered tunnel stack reduced the P/E operational speed for a fixed P/E voltage and time. As shown in the figure, the FG is charged earlier at ~10^{-6} s for SiO_2/La_2O_3 stack and led a wider memory window than experimental data

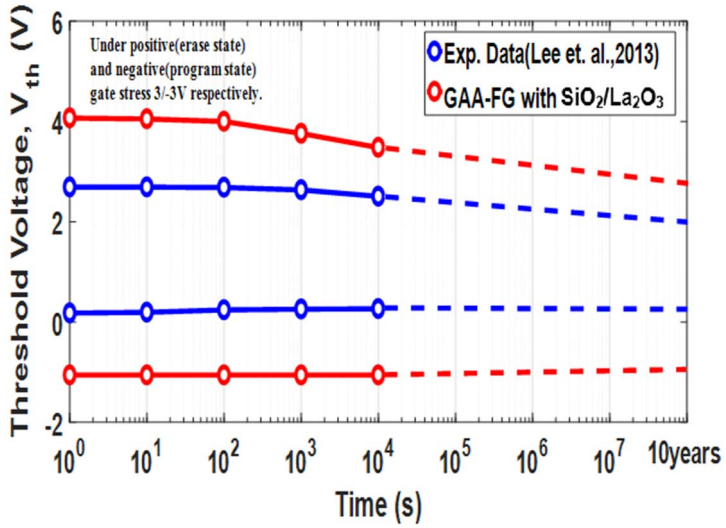

Fig. 4. 10 years approximation of data retention under positive (erase state) and negative(program state) gate stress 3/-3V. For a given P/E operational time, engineered tunnel stack shows steeper slope and wider memory window compared to experimental data.

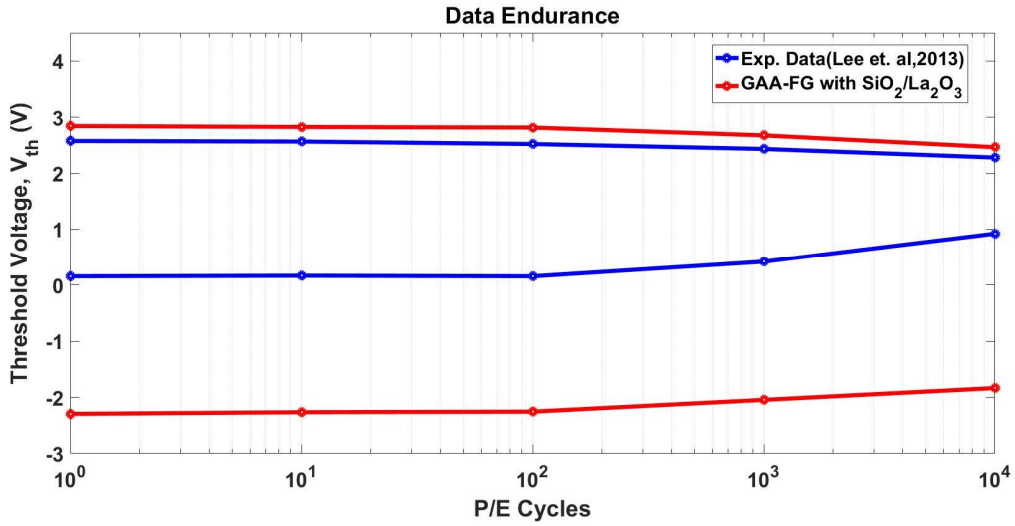

Fig. 5. Comparison of data endurance after 10^4 of P/E cycles between GAA-FG with SiO_2/La_2O_3 and single stack, SiO_2. Wider threshold shift can be observed for SiO_2/La_2O_3 stack resulting to a better endurance (16% data loss) compared to the single stack (46% data loss).

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