HARDWARE ACCELERATOR IMPLEMENTATION OF COLOUR CORRECTION ALGORITHM

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DEDICATION

This project report is dedicated to all the people such as my parents, my other family members, my friends and whoever that taught me to never give up and always believe in myself.

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ABSTRACT

Colour correction algorithm plays an essential part in processing the colour information. Researches on various statistical methods in colour correction algorithms keep growing in order to obtain higher accuracy and reproducibility for the intended usage. Among those, Polynomial Colour Correction is one of the common applications in practice. Nevertheless, the intensive computation and inconvenience of implementing complex algorithm using Hardware Description Language have significant impact on the timing performance especially for those urgent life-threatening diagnosis application. Through this project, a hardware accelerator is proposed to improve the timing performance of the repetitive nature in the Polynomial algorithm while maintaining its accuracy with a minimal degradation. But before designing the hardware accelerator, there is a need to investigate on the compute intensive part of the baseline algorithm. High Level Synthesis tool is used to maximize the design space exploration and effectively minimize the design time. The proposed work has included several optimization techniques such as loop unrolling, pipelining and array partitioning to further exploit the parallelism of the colour correction algorithm. Analysis on latency, total execution time, resource utilization, maximum operating frequency and accuracy with respect to software baseline is conducted to evaluate the outcome of the hardware design. At the end of the project, it is identified that the combination of all the three approaches is able to achieve the highest timing speedup of 22.05 times but at a cost of hardware resources. On the other point of view, it provides several solutions for designs with different usage and targets to achieve based on the performance and hardware cost trade-off.

ABSTRAK

Algoritma pembetulan warna memainkan peranan yang vital dalam pemprosesan maklumat warna. Penyelidikan mengenai pelbagai kaedah statistik dalam algoritma pembetulan warna terus bertambah untuk mendapatkan ketepatan dan reproduksiti yang lebih tinggi untuk pelbagai penggunaan yang berlainan tujuan. Antaranya, algoritma Pembetulan Warna Polynomial adalah salah satu aplikasi yang biasa dalam amalan. Walau bagaimanapun, pengiraan intensif dan ketidakselarasan melaksanakan algoritma kompleks menggunakan Bahasa Keterangan Perkakasan mempunyai kesan yang ketara terhadap prestasi masa terutama bagi aplikasi diagnosis yang mengancam nyawa. Melalui projek ini, pemecut perkakasan telah dicadangkan untuk meningkatkan prestasi masa sifat berulang-ulang dalam algoritma Polynomial sambil mengekalkan ketepatannya dengan kemerosotan yang minimum. Tetapi, sebelum mereka bentuk pemecut perkakasan ini, keperluan untuk menyiasat bahagian pengiraan intensif algoritma garis dasar sepatutnya dipraktik. Alat Sintesis Aras Tinggi juga digunakan untuk memaksimumkan penerokaan ruang reka bentuk dan mengurangkan masa reka bentuk secara berkesan. Kerja yang dicadangkan ini telah merangkumi beberapa teknik pengoptimuman seperti gelung pembongkaran, pipelining dan pembahagian susun atur untuk mengeksploitasi paralelisme algoritma pembetulan warna dengan lebih lanjut. Analisis mengenai latensi, jumlah masa pelaksanaan, penggunaan sumber, frekuensi operasi maksimum dan ketepatan berkenaan dengan algoritma garis dasar dijalankan untuk menilai prestasi hasil reka bentuk perkakasan. Di peringkat akhir projek, ia dikenalpasti bahawa gabungan ketiga-tiga pendekatan tersebut dapat mencapai pemecutan masa yang paling tinggi sebanyak 22.05 kali tetapi dengan pengorbanan kos sumber perkakasan. Pada pandangan yang lain, projek ini telah menyediakan beberapa penyelesaian bagi reka bentuk yang berbeza penggunaan dan sasaran berdasarkan prestasi dan kos perkakasan yang diingini.

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3D	-	3-Dimensional
CPU	-	Central Processing Unit
CUDA	-	Compute Unified Device Architecture
DMA	-	Direct Memory Access
DUT	-	Device Under Test
FF	-	Flip-flops
FPGA	-	Field Programmable Gate Arrays
fps	-	frames per second
G	-	Giga
GPU	-	General Processing Unit
GW	-	Gray World
HDL	-	Hardware Description Language
HDR	-	High Dynamic Range
HLS	-	High-Level Synthesis
Hz	-	Hertz
IP	-	Intellectual Property
K	-	Kilo
LCC	-	Linear Colour Correction
LUT	-	Look-up Table
M	-	Mega
m	-	milli
MAE	-	Mean Absolute Error
MSGW	-	Multi-Scale Gray World
MSR	-	Multi Scale Retinex
MSRCR	-	Multi Scale Retinex with Colour Restoration
MSRCR+AL	-	MSRCR with Autolevels
n	-	nano

NCD	-	Normalized Colour Difference
PCC	-	Polynomial Colour Correction
pgLUT	-	Polynomial Regression with Modified Gamma LUT
PSNR	-	Peak Signal to Noise Ratio
RAM	-	Random Access Memory
RGB	-	Red, Green, Blue
RTL	-	register-Transfer Level
s	-	seconds
SFG	-	Signal Flow Graph
sRGB	-	standard Red, Green, Blue
SSIM	-	Structural Similarity Index
SSR	-	Single Scale Retinex

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CHAPTER 1

INTRODUCTION

1.1 Research Background

In the recent decades, digital computers and image processing techniques have been growing tremendously and becoming more and more stable. Digital images are frequently used in electronic display, transmission and printing compared to the analogue images [1]. As a result, various pronounced advantages of digital images have been introduced, which are processing flexibility, transmission reliability, ease of reproduction, storage and retrieval facility as well as the compatibility with digital computers and networks [1]. Digital images have transformed from gray-scale to colours made of red, green and blue (RGB) combination.

Images with desired colour are normally used in biomedical diagnosis, virtual reality application, computer games, visual quality inspection and others [2]. Factors like light source conditions, image acquisition device and angle of the image being taken [3] might cause nonlinear contrast and brightness changes [4] and thus affect the quality of the image. Unfavourable phenomenon like overexposed or underexposed, cooler or hotter image colour, shadows and highlights are features to be eliminated during the image processing stage as they will affect the visual of users and the accuracy of a diagnosis especially in medical field. Not only this, the colour images produced by digital cameras are usually device-dependent, where images are captured in a colour space designated according to the properties of a particular imaging device. Hence, when the captured images are to be rendered or displayed on other devices, the colour of the images may differ from the originally captured images [5]. The differences here is due to the technology limitation on the devices which creates different colour gamut across the devices and thus limiting the colour to be reproduced by the devices.

In order to acquire the best fit image quality by using the image processing techniques, various algorithms have been presented by the researchers. Every algorithm introduces diverse distinct features as well as the limitations when transforming the device-dependent colour space to device-independent colour space like the standard RGB (sRGB) colour space. In this study, the focus is on polynomial colour correction (PCC), which is commonly used in practice. Linear colour correction (LCC) can produce desirable colour value approximation to the sRGB format with the linear changes in scene radiance or exposure. However, it may induce remarkable mapping errors for some surfaces. In order to reduce this mapping error, PCC is introduced by adding few simple extensions to the linear approximation [6].

In the recent years, where image size keeps on increasing with the name of better resolution, there is a need to maintain or minimize the processing time with those large data sets as well as having low power consumption. Normal Central Processing Unit (CPU) has reached its bottleneck with the speedup technique of limited clock scaling. Therefore, Field Programmable Gate Arrays (FPGA), which is capable to execute tremendous amount of operations in parallel with lower energy cost, is gaining significant interest among the designers [7]. In addition, FPGA can be further exploited by implementing heterogeneous system which integrates both processing unit and hardware accelerator on one board. Using this approach, intensive computational operations can be executed by the hardware accelerator while maintaining the complex algorithm in the CPU. But, designing sophisticated application on FPGA using Hardware Description Language (HDL) requires complex coding. Thus, High-Lvel Synthesis (HLS) tool can be utilized for a more efficient design-space exploration and shorter design time as it can directly map the C/C++ algorithm into a digital circuit and offer various optimization compiler directives [7].

1.2 Problem Statements

A variety of colour correction techniques have been developed by researchers, either in software or hardware. Often, the new algorithms introduced have improved accuracy, performance as well as intelligence. However, some gaps are still able to be observed from the previous work.

First of all, a compute intensive algorithm can lead to high execution time. Normally, an algorithm can be considered as compute intensive when it involves complex operations, large dataset from an image or both happens at the same time. As mentioned in [8], it is very difficult to realize real-time image processing with the huge image dataset or the complex operations on a serial processor. Also, from [3], the high number of iterations set for the algorithm will multiply the execution time. But, if the iteration number is too low, the result is not accurate. In some cases, the computation is done pixel by pixel and with the intended number of iterations, hence the execution time will be boosted significantly. Another unavoidable fact is that resolution of current images is very high which already achieves around 4 Kilo (K) by 4K of pixels. Therefore, compute intensive part of an algorithm must be identified before designing solutions to the problem.

Besides that, it has also been identified that complex algorithm implementation using HDL results in longer design time and less flexibility, especially when sudden design change is required. Cacciotti *et al.* revealed that designing hardware accelerator for sophisticated applications is not a minor work and complex in terms of HDL coding [7]. It involves a certain level of hardware and software architecture knowledge in order to properly integrate and interface the hardware and software algorithms such as the planning of interface signals, data transmission sequence, control signals and much more. The accuracy of the design depends heavily on the hardware-software interaction. Furthermore, [9] has stated that it is easier if instantiating the floating-point intellectual property (IP) instead of designing from scratch. All these examples have indirectly shown that hardware implementation in HDL has become very challenging and complex before designer can further optimize the design for parallelism in hardware. Hence, by using HLS which is compatible with C / C++ language, designer can explore the design space more easily, more efficiently and faster without the concern of difficult conversion of C, C++, Python or other software programming languages to HDL.

1.3 Objectives

The aim of this research is to design hardware accelerator for PCC algorithm. In order to achieve the target, objectives below are identified:

1. To identify compute intensive part in the software colour correction algorithm.
2. To explore the design space of PCC hardware accelerator using Vivado HLS especially in performance optimization.
3. To analyze performance of hardware accelerator in terms of latency, total execution time and resource utilization while targeting for minimal degradation in accuracy.

1.4 Research Scope

In this project, scopes are drafted so that the project is realistic in execution and completed within the given time frame. Firstly, the PCC software algorithm is simulated in MATLAB and the output parameters are captured as the reference for hardware accelerator. Next, the algorithm is implemented and run on Vivado HLS in C language using different optimization techniques. The output results from hardware accelerator is then be measured and analyzed in terms of latency, total execution time, resource utilization and accuracy. Accuracy of the hardware accelerator is compared with the output from its software code, which is the MATLAB design.

1.5 Chapter Organization

This report consists of five chapters discussing the work done in this project. Chapter 2 contains the literature review of the previous work on multiple colour correction algorithms and the hardware implementation or performance enhancement made on the existing software algorithms. Limitations of the existing techniques as well as the summary of the possible improvement are included in this chapter too. Chapter 3 subsequently discusses the flow of the project, software algorithm's operations and methodology of the proposed hardware implementation with different optimization techniques. Following that is Chapter 4 which includes the detailed evaluation and discussion on the results acquired in both software and hardware algorithms according to the objectives listed. Lastly, a brief conclusion on the project as well as future work recommendations are presented in Chapter 5.

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