OPTIMIZATION OF PROCESS PARAMETERS FOR LOWER LEAKAGE CURRENT IN 10 NM FINFET USING TAGUCHI METHOD

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A project report submitted in partial fulfilment of the
requirements for the award of the degree of
Master of Engineering (Computer & Microelectronic Systems)

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JULY 2020

DEDICATION

This project report is dedicated to my father, who taught me that the best kind of knowledge to have is that which is learned for its own sake. It is also dedicated to my mother, who taught me that even the largest task can be accomplished if it is done one step at a time.

ACKNOWLEDGEMENT

I would like to thank to God for giving me the strength, patience and ability to go through all the trials and challenges to complete this final year project successfully. This project would not have been possible without the support of many people. No one walks alone on the journey of life. I would like to take this opportunity to express my gratitude to the people who have been instrumental in the successful completion of this project.

First and foremost, I would like to express my sincere appreciation to my supervisor, Dr Zaharah binti Johari for giving me this golden opportunity on doing and completing this project with all her guidance and knowledge. This project would have never been accomplished without her constant assistance and dedicated involvement. Thank you very much for her enthusiasm and understanding during these two semesters.

Apart from that, I would like to show my biggest gratitude to my beloved family for their unconditional support and encouragement throughout this process. Their love and moral support are the main factors that make me keep going on. Next, I would like to forward my thanks to the faculty; School of Computer and Microelectronic Engineering of Universiti Teknologi Malaysia (UTM), that gave me chance, opportunities and support to gain knowledge in this field.

Furthermore, I would like to highlight my appreciation to my friends, Goh Chien Nam and Muhammad Faidzal Bin Mohamad Rasol, who inspired, encouraged and fully supported me in every trial that came to my way. They had given me constructive and valuable advices throughout the accomplishment of this project.

Once again, thank you very much for their endless support and motivation throughout this project.

ABSTRACT

The scaling of conventional transistor according to Moore's Law is predicted to reach its limitation in the future. The conventional transistor using silicon material particularly at nanoscale channel has experienced the short channel effect (SCE), which leads to increase in the leakage current. Therefore, alternative device structure and advanced material are needed to overcome the SCE and reduce the leakage current (I_{LEAK}) with regards to the transistor performance. In this project, a method to control the leakage current in ultranarrow 10 nm FinFET using High-K dielectric material is proposed. The device's fabrication and electrical characterization are then executed using TCAD Sentaurus from Synopsys. Optimization of the process parameters using L9 Taguchi method and finally prediction of the best combination of process parameters in order to obtain the minimum leakage current (I_{LEAK}) in the 10 nm FinFET. There are four process parameters were varied, which are the fins dimension (fin height and width), channel concentration and oxide thickness. Smaller-the-Better (STB) Signal – to –noise ratio (SNR) and the Analysis of Variance (ANOVA) is used to study the performance characteristic and finally obtain the best combination of process parameters in order for the device to perform at its best performance, that will later benchmarked with predicted data from International Technology Roadmap for Semiconductors (ITRS) and previous published results. The optimization is expected to result in the attainment of the lower leakage current value in order to increase the speed performance of the device.

ABSTRAK

Pengukuran transistor konvensional mengikut Undang-undang Moore diramalkan akan mencapai batasannya pada masa akan datang. Transistor konvensional menggunakan bahan silikon terutamanya pada saluran nanoscale telah mengalami kesan saluran pendek, yang menyebabkan kebocoran arus meningkat. Oleh itu, struktur peranti alternatif dan bahan canggih diperlukan untuk mengatasi kesan saluran pendek dan mengurangkan kebocoran arus. Dalam projek ini, kaedah untuk mengawal kebocoran arus elektrik dalam 10 nm FinFET ialah menggunakan bahan High-K dielektrik. Fabrikasi dan pencirian elektrik telah dijalankan menggunakan TCAD Sentaurus dari Synopsys. Kaedah L9 Taguchi digunakan untuk mengoptimumkan parameter proses dan akhirnya meramalkan kombinasi parameter proses yang terbaik untuk mendapatkan kebocoran arus yang paling minimum dalam *FinFET* 10 nm. Empat parameter proses yang diubah, iaitu dimensi sirip (kelebaran dan ketinggian), kepekatan saluran dan ketebalan oksida. ***Smaller-the-Better (STB) Signal – to –noise** ratio (SNR)* dan *Analysis of Variance (ANOVA)* digunakan untuk mengkaji ciri prestasi dan akhirnya meramalkan gabungan parameter proses terbaik untuk mendapatkan prestasi terbaik peranti yang akan kemudian ditandai dengan data yang diramalkan dari Peta Jalan Teknologi Antarabangsa untuk Semikonduktor dan juga karya terbitan sebelumnya. Pengoptimuman dijangka akan menghasilkan pencapaian nilai kebocoran arus yang rendah untuk meningkatkan prestasi kelajuan peranti.

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LIST OF ABBREVIATIONS

TCAD	-	Technology Computer-Aided Design
MOSFET	-	Metal-Oxide Semiconductor Field-Effect Transistor
FinFET	-	Fin-Field Effect Transistor
CMOS	-	Complementary Metal Oxide Semiconductor
SCE	-	Short Channel Effects
DIBL	-	Drain-Induced Barrier Lowering
MugFET	-	Multigate FinFET
SNR	-	Signal-to-Noise Ratio
EOT	-	Equivalent Oxide Thickness
IC	-	Integrated Circuit
ANOVA	-	Analysis of Variance
ITRS	-	International Technology Roadmap for Semiconductors
HK/MG	-	High-K/Metal Gate
S/D	-	Source/Drain
L9	-	Level 9
L11	-	Level 11
DF	-	Degree of Freedom
SS	-	Sum of Squares
WF	-	Work Function
Si	-	Silicon
SiO_2	-	Silicon dioxide
HfO_2	-	Hafnium oxide
Si_3N_4	-	Silicon nitride
Al_2O_3	-	Aluminium oxide
AlN	-	Aluminium nitride
SiGe	-	Silicon Germanium
TiN	-	Titanium Nitride
C_{gate}	-	Gate Capacitance

LIST OF SYMBOLS

nm	-	nanometer
V_{dd}	-	Drain to drain voltage
I_{LEAK}	-	Leakage current
L_{eff}	-	Effective channel length
W_{eff}	-	Effective width
η_{STB}	-	SNR (Smaller-the-Better)
n	-	Number of tests
y_i	-	Experimental value of the leakage current
Σ	-	Sum of leakage current of the experiment

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CHAPTER 1

INTRODUCTION

1.1 Problem Background

The guiding principle that is used for CMOS scaling for the past few decades is Moore's Law [1]. The research and development to improve the performance of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is growing at an unprecedented rate since MOSFET is the most vital device in the field of electronic, communication and radio frequency application. One of the crucial methods to improve the performance of the MOSFET is by designing it into smaller dimension, which also means to downscale the size of the device [2]. Intel's state-of-art has doubled its transistor density in the recent years, from 45-nm having 3.3 million transistors per square millimeter to 10 nm having 100.8 million transistors per square millimeter [3].

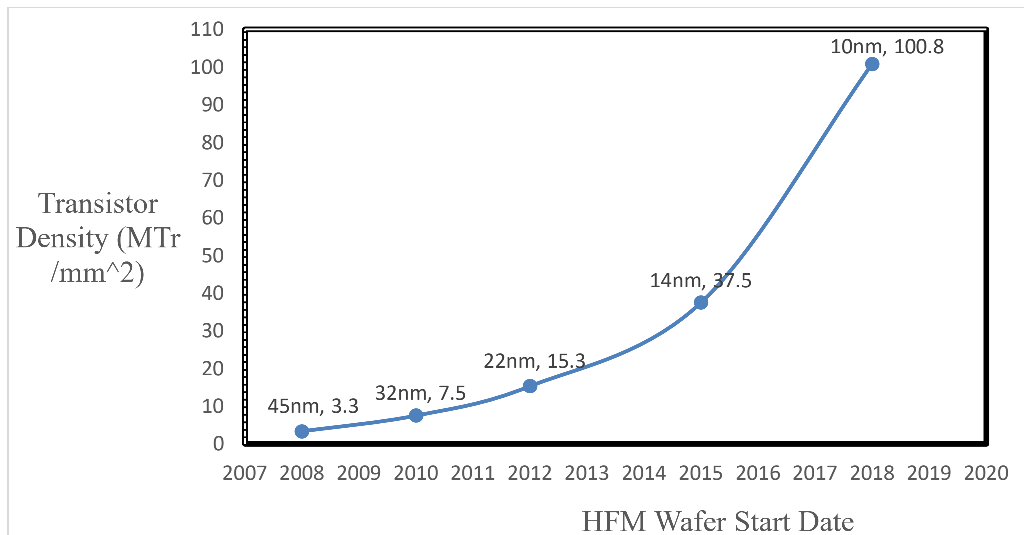

Figure 1.1: State-of-art for Intel's Transistors Density [3]

The gate controllability of the channel potential decreases as the MOSFET is shrinking down. This is due to the drain having an increase of longitudinal field, which causes the short channel effects to become worse [2]. Besides that, as the device dimension decreases, this also means that the equivalent oxide thickness (EOT) reduces, thus increases the leakage current, which makes the fabrication process of SiO_2 not able to carry out. Higher leakage current increases current densities and encourages higher power dissipation [4]. In fact, leakage current (I_{LEAK}) has been identified as one of the main sources of leakage to the total power consumption of CMOS devices [5]. Both the SCE and high leakage current have become the crucial problems to MOSFET. Thus, having an extra gate is one of the attractive alternative ways in order to have increment of gate control over the channel [6].

For future scaling of CMOS technologies, Multigate MOSFETs (MuGFETs) have been considered as one of the attractive and promising candidates. This is because a better drive current had been shown by MuGFETs at a fixed value of V_{dd} [7]. FinFETs are one of the examples of MuGFETs, where the multigated architecture of FinFET having additional discrete fin sizing, which brings an advantage to the design [7] [8]. Crucially, Intel mentioned that 10 nm FinFET shows the capability in terms of higher speed performance and better energy efficiencies compared to the predecessors [3]. Meanwhile, the problem of gate leakage current can be solved by introducing the combination of high-k gate dielectric layer to replace the conventional SiO_2 [9]. This could potentially reduce the leakage current flowing through the gate dielectric layer and improve the reliability of the device.

In fact, in the advancement of CMOS technologies, both the Moore's Law and ITRS played a very significant role. Since the very first edition of the ITRS roadmap in the beginning of 90's, Moore's Law and ITRS have been the compliment to each other. The initial forecast of Gordon Moore is on the number of transistors that can be integrated into the microchip for the coming ten years, which is from 1965 to 1975, but it can be seen for the next three decades, the trend remain unchanged [10]. Meanwhile, ITRS, on the other hand, is an ambitious and reliable document, which is widely used as a guiding reference for the research of the advanced semiconductor device and manufacturing purposes that gives direction for the next generation of

devices. One of the vital sections which included in ITRS is finding and developing new device structures to replace the current conventional MOSFETs for a better performance. One of the suggestions provided in ITRS is using FinFET as the device to boost the performance without neglecting the short channel effects [11].

1.2 Problem Statement

Scaling down the size of MOSFET is the main trend to achieve the target set by Moore's Law. In the current trend, the performance of MOSFET can be improved easily by scaling down its size. Over the past decades, many researchers have tried to enhance the scaling technology and have been successfully changed the physical dimensions of MOSFETs from larger to a smaller dimension [12]. However, the reduction of the channel length of the transistor has reached the limit in current technology. As the channel length are scaled to nanometer, the undesirable effects which are named short channel effects (SCEs) occur and become more problematic. The SCEs is defined as the channel length, L_{ch} of a MOSFET becomes the same order of magnitude as the depletion widths associated with the drain and source, in other words, device downscaling has caused the drain area and source to be much closer to each other, thus resulting in short channel effects [13]. In this situation, the behaviour of the MOSFET is out of expected, and this undesired effect has created a huge impact in terms on the reliability, modelling and the performance.

Over the past few decades, silicon dioxide (SiO_2) has been used as the gate dielectric material. The continually scaling down of CMOS causes the continuous reduction of the equivalent oxide thickness (EOT) until as low as 1nm, which makes the fabrication of SiO_2 having difficulty to be achieved since this thickness would cause higher gate leakage current, and consequently causing increased of current densities and encourages high power dissipation [4]. In fact, one of the main causes of the current leakage is because of the ultra-thin gate which contribute much to the total static power dissipation of the CMOS device.

1.3 Objectives

The main aim of this project is to simulate and optimize the process parameters for lowering leakage current in a 10 nm FinFET by replacing the conventional SiO_2 and polysilicon layers respectively with high-k dielectric materials, using L9 Taguchi Method.

Below are the objectives, which needed to be achieved to realize the aim of the project:

i. To simulate a 10 nm FinFET with the deposition of high-k material (Hafnium Oxide) using TCAD Sentaurus from Synopsys.

ii. To optimize the process parameters using L9 Taguchi Method in order to obtain a lower leakage current (I_{LEAK}).

iii. To perform a statistical analysis and predict the best process parameters combination of the 10 nm FinFET device using Analysis of Variance (ANOVA) while benchmarking with predicted data from ITRS and previous published results.

1.4 Project Scope

i. 10 nm FinFET is developed and simulated as the device structure with this gate length shows reduced SCE and leakage current with a higher drive current, thus lowering the leakage current.

ii. The device's process will be executed using TCAD Sentaurus from Synopsys. TCAD Sentaurus software is used throughout this whole project to organize, design and run simulations.

iii. Optimization of the 10 nm FinFET using Hafnium Oxide (HfO_2) as the dielectric layer to replace the conventional silicon dioxide for lower leakage

current. Hafnium oxide appears to be one of the most attractive type of high k-dielectric materials and the demand for high-k dielectric materials in integrated circuits (IC) has becoming more and more imminent in the development of electronic devices towards miniaturization. Besides, the thickness of the gate oxide using HfO_2 would then be optimized throughout the simulation process.

iv. L9 Taguchi Method is used for the optimization of the process parameters. The advantages of Taguchi method over the other methods are that numerous factors can be simultaneously optimized, and more quantitative information can be extracted from fewer experimental trials.

1.5 Chapter Organization

This report is separated into five chapters covering different aspects of this research. The overview of the work is described as follows:

Chapter 1: This chapter contains the introduction of this research project and brief discussion on background, problem statement, aim, objectives and project scope of this research project.

Chapter 2: This chapter covers the literature review of the project. It contains the concept of this project and on previous work done by various researchers. This chapter also discusses about the optimization process using L9 Taguchi method by various researchers.

Chapter 3: This chapter defines the methodology or procedure used in the project. Flow charts are also included for better description. Besides, this chapter explains the procedure to model and simulate the design. Performance parameters used to compare and analyse the 10 nm FinFET using Taguchi method and ANOVA also been discussed.

Chapter 4: This chapter contains the results for this project. The simulation results obtained are also discussed and the best setting of parameters is then chosen based on the statistical analysis on the performance of the device.

Chapter 5: The chapter contains the summary or conclusion of the research project and findings. Apart from that, this chapter also included the directions and suggestions of future works for improvement of current work.

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