DESIGN AND CHARACTERIZATION OF 8×1 PHOTON COUNTING ARRAY IN 0.13 µm CMOS TECHNOLOGY AT 1 GHz

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DEDICATION

This project is dedicated to my beloved family, lecturers and friends for guidance, encouragement and inspiration throughout my journey of education.

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ABSTRACT

A single-photon avalanche diode (SPAD) is widely used as low-intensity ionizing radiation sensor at high speed detection rate application. The SPAD function when applied reverse bias voltage higher than the breakdown voltage of the device known as Geiger-mode. SPAD operates when the detected photon carrier activates a large avalanche current flow in a short period of time due to the impact of ionization. This avalanche effect occurs when the electrons or holes accelerated to high kinetic energies through a large potential gradient. This project focuses on the design and simulation of 8×1 passively quenched Single Photon Avalanche Diode (SPAD) array applying 0.13 µm CMOS technology. In term of fabricating the device, difference shape and size will have different current, voltage and count rate performances. Mentor Graphics TCAD is used to predict the performance of suggested SPAD array prior fabrication process. A SPAD is required to have high photo detection rates, high output signal in response to photons and faster counting speed. The drive for this project is to improve the counting rate of the model at low voltage and study the effect of quenching circuit integrated with SPAD. As the increasing demand of high-speed photon sensor, this design introduces a high-speed photon detection with quenching circuit applicable for several application as such biomedical, astronomy, fluorescence decay etc. In this project, Single Photon Avalanche Diode (SPAD) simulation model is utilized into 8×1 photon counting array circuit using 0.13 µm CMOS technology, to implement parallel detection and serial output of 8×1 photon counting array in 1 GHz counting rate and to characterize 8×1 array with non-time correlated timing. The 8×1 SPAD array designed using 0.13 µm CMOS technology via Mentor Graphics TCAD tool. The design is formed by integrating a single pixel SPAD from previous research into 8×1 array circuit and will provide an operation of parallel in serial out (PISO) result. In the single pixelate design, consist of the photon avalanche diode (SPAD), a passively quenching circuit and pulse discriminator circuit (PDC). The simulated dead time result from the schematic design for the 8×1 passive quenched SPAD array is observed with the result as 1 GHz operating frequency with the transistor size length 0.13 µm and width 0.35 µm. The result from physical designed layout is compared to the schematic design to ensure both designs provide the similar output.

ABSTRAK

Single diode avalanche avalanche (SPAD) digunakan secare meluas sebagai sensor radiasi pengion intensiti rendah dalam aplikasi kadar pengesanan berkelajuan tinggi. *SPAD* berfungsi apabila diterapkan dengan voltan berkecenderungan terbalik yang lebih tinggi daripada voltan pecahan peranti, Fungsi ini dikenali sebagai *Geiger-mode*. *SPAD* beroperasi apabila foton yang dikesan mengaktifkan aliran arus deras yang besar dalam tempoh masa yang singkat disebabkan oleh kesan ionasi. Projek ini memberi tumpuan kepada reka bentuk dan simulasi 8 × 1 pelindap pasif *Single Photon Avalanche Diode (SPAD)* yang menggunakan teknologi 0.13 µm *CMOS*. Dalam segi fabrikasi peranti tersebut, perbezaan dalam bentuk dan ukuran boleh menberikan perbezaan dalam segi arus elektrik, voltan dan kadar kiraan. Penggunaan alat *Mentor Graphics TCAD* adalah untuk meramalkan prestasi proses fabrikasi susunan *SPAD* yang teleh dicadangkan. *SPAD* diperlukan untuk ciri-ciri kadar pengesanan foto yang tinggi, tindak balas cepat terhadap isyarat keluaran foton dan pengiraan yang kelajuan tinggi. Pemacu untuk projek ini adalah untuk meningkatkan kadar pengiraan model pada voltan rendah dan mengkaji kesan litar pelindap bersepadu dengan *SPAD.* Peningkatan dalam permintaan sensor foton berkelajuan tinggi menyebabkan reka bentuk ini diperkenalkan untuk pengesanan foton berkelajuan tinggi dengan litar pelindapan kejutan yang digunakan untuk beberapa aplikasi seperti bioperubatan, astronomi, peluruhan pendarfluor dan lain-lain. Dalam projek ini, model simulasi *Single Photon Avalanche Diode (SPAD)* dimanfaatkan dalam jalaran 8×1 dengan menggunakan teknologi *CMOS* 0.13 µm untuk litar mengira foton, melaksanakan pengiraan foton dalam kadar pengiraan 1 GHz menggunakan pengesanan selari dan pengeluaran bersiri jalaran 8×1 dan menonjolkan jalaran 8×1 dengan ciri-ciri masa yang tidak berkorelasi. Reka bentuk *SPAD* 8×1 akan direka menggunakan teknologi *CMOS* 0.13 µm melalui alat *Mentor Graphics TCAD tool*. Reka bentuk ini direka dengan mengintegrasikan SPAD piksel tunggal dari penyelidikan terdahulu ke litar jalaran 8×1 dan akan mengeluarkan hasil beroperasi *parallel in serial out (PISO).* Dalam reka bentuk piksel tunggal, terdiri daripada diod foton tunggal *(SPAD)*, litar pasang pelindap pasif dan litar diskriminasi nadi (PDC). Keputusan *Dead Time* yang disimulasikan dari reka bentuk skematik dengan susunan SPAD jalaran 8×1 diperhatikan dengan hasilnya sebagai operasi 1 GHz dengan menggunakan transistor ukuran panjangan 0.13 µm and lebaran 0.35 µm. Hasil daripada susun atur yang dirancang secara fizikal dibandingkan dengan reka bentuk skematik untuk memastikan kedua-dua reka bentuk memberikan hasil yang serupa.

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LIST OF ABBREVIATIONS

SPAD	-	Single Photo Avalanche Diode
CMOS	-	Complementary Metal Oxide Semiconductor
PISO	-	Parallel-In Serial-Out
PDS	-	Pulse Discriminator Circuit
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
TCAD	-	Technology Computer-Aided Design
PEX	-	Parasitic Extraction
MCP	-	Multichannel Plates
PMT	-	Photomultiplier Tubes
ADC	-	Analogue to Digital Converter
DRC	-	Design Rule Check
LVS	-	Layout Versus Schematic
MSB	-	Most Significant Bit
LSB	-	Lowest Significant Bit

LIST OF SYMBOLS

Ω	-	Resistance
V	-	Voltage
A	-	Current
W	-	Watt
Hz	-	Hertz
C	-	Capacitance
t_d	-	Dead time
t_q	-	Quenching time
t_r	-	Recovery time

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CHAPTER 1

INTRODUCTION

1.1 Introduction

Single-photon avalanche diodes (SPADs) is known as one of the photodetectors for single-photon counting and timing applications. These photodetectors are used to detect photons in different intensity and time-dependent waveform of optical signals by counting photons in high speed detection rate [1]. These detectors are applicable for several applications as such biomedical, astronomy, fluorescence decay etc [2]**.** When compare SPADs to other existing photon sensing devices such as the photomultiplier tubes (PMTs) as well as the multichannel plates (MCPs) which are highly responsive to magnetic field. SPADs are much more favourable due to its characteristics of small size, able to integrate into large arrays and unaffected by the magnetic fields [1]. SPADs also have highly sensitive in detecting light at a high detecting rate in low light environment [3]**.**

SPADs sensors are needed to detect the incoming photons at fast pace and generate accurate and readable data for the circuit to process the signal. SPADs are p-n junction that operates in Geiger mode, where the operation of the diode is due to the applied reverse bias voltage to the diode is higher than the breakdown voltage [2][3]**.** When detect photon, generated carrier will trigger avalanche current due to the impact ionization. Although SPADs are good in term of their characteristics, incompatible to integrate into electronic and hard to fabricate single pixel into arrays are the major drawback [4]**.** Using Mentor Graphic TCAD tools to create a similar arrays SPADs model can determine the expected result before fabricating the device, which then can save the cost and time for fabrication.

1.2 Problem Statements

As stated earlier, the process taken to fabricate SPADs is quite hard [4]**.** To ease the understanding of the outcome of the SPADs design, Mentor Graphic TCAD tools can be used to design and simulate SPADs model and determine the result for the quenching circuit as stated in previous studies. Besides, another reason for using Mentor Graphic TCAD tools to simulate the SPADs model is because of avalanche process cannot be modelled using the SPICE tools. The SPADs model can be designed using TCAD tool and the layout can be verified together with the functionality with the schematic design using low voltage 0.13 um CMOS technology.

As a photon detector, the high-speed detection rate is needed to detect incoming photons [5]**.** Based on previous research [6]**,** fast self-quenching or recovery time is needed to reduce the dead time, as dead time of the diode will affect the SPADs performance. Long dead time will hinder the SPADs execution for the counting rate. Other than that, using different types of counter will also affect the reading of the outcome. In this project high-speed adder will be implemented to improve the performance of the SPADs model.

1.3 Objectives

This project focus on design and simulation of 8×1 passively quenched Single Photon Avalanche Diode (SPAD) array using 0.13 µm CMOS technology. The drive for this project is to improve the counting rate of the model at low voltage and study the effect of quenching circuit integrated with SPAD. The design of this SPAD model was done using Mentor Graphics tools. The objectives of this project include as stated:

i. To utilize Single Photon Avalanche Diode (SPAD) simulation model to 8×1 photon counting array circuit using 0.13 µm CMOS technology.
ii. To implement parallel detection and serial output of 8×1 photon counting array in 1 GHz counting rate.
iii. To characterize 8×1 array with uncorrelated timing.

1.4 Scope of Work

The design of the 8×1 SPAD array with parallel in serial out PISO will be designed using 0.13 µm CMOS technology via Mentor Graphics TCAD tool. The design is formed by integrating a single pixel SPAD [2] from previous research into 8×1 array circuit and will provide an operation of parallel in serial out (PISO) result. In the single pixelate design, consist of the photon avalanche diode (SPAD), a passively quenching circuit and pulse discriminator circuit (PDC). A 4-bit asynchronous counter is used to accumulate the digitized signal and pass the signal to the 8-bit parallel-in serial-out model to shift and load the signal data. The simulated dead time result from the schematic design for the 8×1 passive quenched SPAD array is observed with the result as 1 GHz operating frequency. The result from physical designed layout is compared to the schematic design to ensure both designs provide the similar output.

1.5 Project Chapter Outlines

There are 5 chapters to be discussed in this report. For Chapter 1, it describes on introduction of this project background, the problem statement, the objectives and project work scopes of this project.

Moving on to Chapter 2, this chapter present on the literature review on single photon avalanche diodes (SPADs). This part covered some of the shift register that includes parallel-in serial-out (PISO), parallel-in parallel-out (PIPO), serial-in serial-out (SISO) and serial-in parallel-out (SIPO) implementations.

Chapter 3 discusses on the workflow of this project. Flow charts and circuits are included to give better explanation on the project. It explains the method to model and simulate the design, from a single pixel to 8×1 arrays SPAD model.

Next, Chapter 4 describes the result and the design obtained after simulating the functionality of the photon counting circuit and analysing the obtained outcome from the simulations.

Lastly in Chapter 5 where this chapter provided a conclusion on the summarized results and findings of this project. This chapter also provided the suggestions of future works that can be implement to this current project.

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