DESIGN OF A LAN INTERFACING MODULE FOR A SOFTCORE PROCESSOR – AMIR CPU

LIM HUI TENG

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DEDICATION

This project report is dedicated to my supervisor, who lead me along the way of completing this project report. Fruitful of knowledge and experience in his expertise has been shared to me which has been helping me a lot during the completion of hardware implementation, programming and paper work. It is also dedicated to my family, who encouraged me when I was upset with the undesired project result. A lot of moral values has shared by them which has motivated me to never give up on the way of getting the best output. Lastly, this project report is dedicated to my course mates, who always shared with me useful resources and knowledge that has broaden my mindset along the project on-going.

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ABSTRACT

An AMIR CPU is a novel 32-bit softcore processor developed from the improvement of the weakness of existing Intel x86 and ARM architectures which has its own local I/O memory and easier ISA (Instruction Set Architecture) compared to RISC (Reduced Instruction Set Computer) and CISC (Complex Instruction Set Computer). The motivation of this project is to design a LAN interfacing module which is compatible with the features having by the softcore AMIR CPU. This is because the new AMIR CPU is not supported by HDL coding style but need to use its instruction set architecture to generate the machine code before can be implemented onto the FPGA. Besides this, this project is to study the capability of AMIR CPU to support the functionality of Ethernet communication as for now the development of this softcore processor is still in progress. However due to the reason of using a ready-to-use Ethernet LAN controller, it is found out that the relative researches or resources are less whereby most of the research is based on C-based microcontroller that comes along with the ready-to-use Ethernet library. Therefore, the objectives this project are:
(1) To build a SPI module on DE0 FPGA board in order to build up the same communication interface with the ENC28J60
(2) To send an Ethernet packet from DE0 to PC through the Ethernet communication with data transmission rate of 10MB/s using HDL coding style
(3) To process the input data and send to PC through Ethernet by using AMIR instruction set architecture after the first two objectives are achieved.
The scopes of the project are discussed in the section later. The project is aimed for contributing to develop the new feature (LAN) that able to work along with the new processor – AMIR CPU and to study the methodology of establishing LAN that is different from the existing research.

ABSTRAK

CPU AMIR adalah pemproses softcore 32-bit baru yang dibangunkan dari peningkatan kelemahan seni bina Intel x86 dan ARM yang ada yang mempunyai memori I / O tempatan sendiri dan ISA yang lebih mudah (Instruction Set Architecture) berbanding dengan RISC (Reduced Instruction Set Computer)) dan CISC (Komputer Set Instruksi Kompleks). Motivasi projek ini adalah untuk merancang modul antara muka LAN yang sesuai dengan ciri-ciri yang dimiliki oleh CPU AMIR softcore. Ini kerana CPU AMIR baru tidak disokong oleh gaya pengkodan HDL tetapi perlu menggunakan arsitektur set instruksinya untuk menghasilkan kod mesin sebelum dapat diterapkan ke FPGA. Selain itu, projek ini adalah untuk mengkaji kemampuan CPU AMIR untuk menyokong fungsi komunikasi Ethernet kerana untuk saat ini pengembangan pemproses softcore ini masih berjalan. Namun kerana alasan menggunakan pengawal LAN Ethernet yang siap digunakan, didapati bahawa penyelidikan atau sumber daya relatif kurang di mana sebahagian besar penyelidikan berdasarkan mikrokontroler berasaskan C yang disertakan bersama dengan siap sedia gunakan perpustakaan Ethernet. Oleh itu, objektif projek ini adalah:

(1) Untuk membina modul SPI pada papan DEP FPGA untuk membina antara muka komunikasi yang sama dengan ENC28J60

(2) Untuk mengirim paket Ethernet dari DE0 ke PC melalui komunikasi Ethernet dengan kecepatan pengiriman data 10MB / s menggunakan gaya pengkodan HDL

(3) Untuk memproses data input dan mengirim ke PC melalui Ethernet dengan menggunakan arsitektur set instruksi AMIR setelah dua tujuan pertama tercapai.

Skop projek dibincangkan di bahagian kemudian. Projek ini bertujuan untuk menyumbang untuk mengembangkan fitur baru (LAN) yang dapat bekerja bersama dengan pemproses baru - CPU AMIR dan mempelajari metodologi penubuhan LAN yang berbeza dengan penyelidikan yang ada.

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LIST OF ABBREVIATIONS

FYP	-	Final Year Project
I/O	-	Input/Output
ISA	-	Instruction Set Architecture
RISC	-	Reduced Instruction Set Computer
CISC	-	Complex Instruction Set Computer
FPGA	-	Field Programmable Gate Arrays
LAN	-	Local Area Network
RMII	-	Reduced Media-Independent Interface
PC	-	Personal Computer
IoT	-	Internet of Things
ID	-	Identification
LAN	-	Local Area Network
MAN	-	Metropolitan Area Network
WAN	-	Wide Area Network
LE	-	Logic Element
FPU	-	Floating Point Unit
ASIC	-	Application-Specific Integrated Circuit
TCP	-	Transmission Control Protocol
IP	-	Internet Protocol
SPI	-	Serial Peripheral Interface
IEEE	-	Institute of Electrical and Electronics Engineers
LED	-	Light Emitting Diode
TX	-	Transmit
RX	-	Receive
UART	-	Universal Asynchronous Receiver-Transmitter
TTL	-	Transistor-Transistor Logic
MOSI	-	Master Data Out, Slave Data Input
MISO	-	Master Data In, Slave Data Out
NSS	-	Slaved Enabled Signal
CS	-	Chip Select

I2C	-	Inter-Integrated Circuit
JTAG	-	Joint Test Action Group
LCD	-	Liquid Crystal Display

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CHAPTER 1

INTRODUCTION

1.1 Introduction to Ethernet

Ethernet can be defined as a subset of the Local Area Network whereby it allows the interconnection between multiple devices by communicating in a same protocol. Furthermore, an Ethernet also able to provide the description on the method of a network device can transmit the required data and in which format or protocol so that the receiver device is able to recognize the Ethernet packet or segment sent out by transmitter.

Apart from this, Ethernet is still a popular technology used for network construction because of its cheap instalment price compared to the available technologies. Besides this, the Ethernet development is kept on improving in which the 10Mbps of throughput in early year has folded its performance throughout the years. It can now support 100Mbps or even the latest version is able to operate at a throughput of up to 400Gbps.

The advantages of using Ethernet is make sure the intended speed achievement is fulfilled while maintain a reliable data transferring quality. Moreover, low cost of installation compared to other emerging technology. On the other hand, because the Ethernet communication is depending on the RJ245 connectors whereby when there are many devices are involved in the particular network, it may be an issue for debugging and troubleshooting the root cause of the malfunction.

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1.2 Introduction to AMIR CPU

AMIR CPU is a novel 32-bit softcore processor developed from the improvement of the weakness of existing Intel x86 and ARM architectures which has its own local I/O memory and easier ISA compared to RISC and CISC. The processor is established in schematic which requires little learning curve period among a wide range of users even for an occasional user.

There are always some brainstormed ideas and motivations that leading to the establishment of a new processor architecture starting with a softcore implementation. The reason of selecting 32-bit as the data size of processor is due to its wide range coverage in the applications of embedded systems, for example IoT-based embedded application and broadband equipment. Apart from this, the AMIR CPU is designed for education purpose at its first intention. In order to learn and understand a processor architecture well, ISA and assembly language both are the important elements. Therefore, AMIR CPU is created with a simpler ISA that making the learning of assembly language easier throughout the process of understanding the architecture.

Reconfigurability is one of the key features introduced by AMIR CPU. It allows additional functionality to be added easily into the design for softcore CPU according to different requirement at different stage. As an instance, LAN module is a new functionality and component that can be added into the design as LAN is an useful component on achieving fast transmission between devices. Moreover, with the reconfigurability feature of FPGA, it allows the user to integrate any newly designed softcore processor.

1.3 Problem Statement

The new AMIR CPU is not supported by HDL coding style as for now but need to use its own instruction set architecture to generate the machine code before can be integrated onto the FPGA for further use. Besides this, the capability of AMIR CPU to support the functionality of Ethernet communication is not yet explored before thus

there are less resources can support on designing the LAN module directly using AMIR instruction set. Furthermore, due to the reason of using a ready-to-use Ethernet LAN controller, it is found out that the relative researches or resources are less whereby most of the research is based on C-based microcontroller that comes along with the ready-to-use Ethernet library. There were few researches discussing on interfacing the FPGA to the SPI-based Ethernet controller even in using HDL coding style.

1.4 Research Goal

The goal of this research is to develop a SPI interface that is compatible with the Ethernet LAN controller used in this project as DE0 FPGA board is not supporting the SPI interface. Moreover, the research is to explore the methodology on sending Ethernet packet with info encapsulated inside towards another device from DE0 board. Research goal is to design the module based on the AMIR CPU instruction set architecture with a prior prerequisite whereby the Ethernet communication can work properly when using HDL coding style.

1.4.1 Research Objectives

The objectives of the research are:

(a) To build a SPI module on DE0 FPGA board in order to build up the same communication interface with the ENC28J60

(b) To send an Ethernet packet from DE0 to PC through the Ethernet communication with data transmission rate of 10MB/s using HDL coding style

(c) To process the input data and send to PC through Ethernet by using AMIR.

1.5 Project Scopes

The proposed system will be built on a DE0 FPGA board with interfacing to a standalone Ethernet LAN controller, ENC28J60 that can only support up to 25MHz of clock rate. Besides that, this project will cover the SPI interfacing since the DE0 board is not equipped with ready-to-use SPI pins. Furthermore, the RJ245 connector used is Cat5e type which can support up to 1000 MB/s of data transmission rate, however in this project, is only aimed for supporting 10MB/s due to the slow operating system. Moreover, although this project is designed in full-duplex mode of Ethernet communication, but it is only expected to send out an Ethernet packet from FPGA to PC because UDP protocol is used which is no handshake or acknowledgement is expected.

1.6 Summary

This chapter has introduced some basic background regarding the type of networks and the newly developed CPU. In this chapter, it also includes the problem statement, research goal, research objectives and project scope that would like to be focused throughout the research. Lastly, in this report will consist of five main chapters, which are Chapter 1 Introduction, Chapter 2 Literature Review which will exploring the key components in this project and related works, Chapter 3 Research Methodology which will discuss the steps for making the proposed system to be functioned, Chapter 4 Result and Discussion that discussing the system result throughout the project and lastly Chapter 5 Conclusion and Future Work which will conclude the work has done in the current project and the recommendations for the system improvement in future.

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