ELECTROCARDIOGRAM QRS DETECTION HARDWARE ACCELERATOR FOR ASIC IMPLEMENTATION

LIM ZHI QING

UNIVERSITI TEKNOLOGI MALAYSIA

LIM ZHI QING

A project report submitted in partial fulfilment of the
requirements for the award of the degree of
Master of Engineering (Computer and Microelectronic Systems)

School of Electrical Engineering
Faculty of Engineering
Universiti Teknologi Malaysia

JULY 2020

DEDICATION

This project report is dedicated to my parents and friends who taught me to never give up and always believe in myself.

ACKNOWLEDGEMENT

I would like to express my sincere gratitude to my thesis supervisor, Dr Suhaila binti Issak, for encouragement, guidance and supporting ideas which she shared during the execution of this project. Her suggestions and instructions have served a major contribution towards the completion of this project. I would like to thank my project supervisor for allocating her valuable time coming all the way from Johor to Penang to discuss on the project with me. Also, I feel so grateful to her for spending time to have video call with me from time to time to help resolving my confusion. I am also indebted to my company, Intel Microelectronics for funding my master study. Last but not least, my sincere appreciation also extends to my colleagues, manager and others who have giving me their useful advice, encouragement and moral support throughout this project.

ABSTRACT

Electrocardiogram (ECG) analysis is an important tool to detect the heart pulse rate and rhythm. QRS complex plays a vital role in such analysis. This work presents ECG QRS detection based on Pan-Tompkins algorithm using 90nm ASIC design architecture. Among plenty of QRS detection algorithm, Pan-Tompkins algorithm is chosen to detect QRS complex in ECG signal due to its simplicity and accuracy in detecting QRS complex. The algorithm is modified to use together with adaptive threshold for R-peak detection. The input of ASIC design is Hardware Description Language (HDL) code. Nevertheless, compute intensive algorithm and complexity in building Hardware Description Language can degrade timing performance of design which can lead to life-threatening impact to patient. Through this project, a hardware accelerator of QRS complex detector is designed with Register Transfer Level (RTL) optimization technique to improve the timing performance. Before RTL code is developed, the algorithm is modelled in MATLAB to confirm its functionality. To maximize design space exploration and minimize design time due to HDL complexity on building an algorithm, VIVADO HLS tool is introduced in this project. Loop unrolling and loop pipelining technique are used to optimize hardware code in VIVADO HLS. Analysis on design latency, resource utilization, accuracy and total execution time with respect to software baseline is conducted. At the end of the project, total double speedup is achieved, and 144455 cycles are reduced after optimization is done in hardware code. However, number of FF is increased by 30% from original number while the number of LUT is increased by 17% from the original number. On ASIC design analysis, total area and power consumption are found to be 1.686mm^2 and 9.78mW respectively. From Synopsys Prime Time result, the setup time and hold time of the design are met.

ABSTRAK

Analisis Elektrokardiogram (ECG) adalah alat yang penting untuk mengesan degupan dan irama jantung. Kompleks QRS memainkan peranan penting dalam analisis tersebut. Kerja ini mencadangkan pengesanan ECG QRS berdasarkan algoritma *Pan-Tompkins* dengan penggunaan teknologi ASIC 90nm. Di antara banyak algoritma pengesanan QRS, algoritma *Pan-Tompkins* dipilih untuk mengesan kompleks QRS dalan isyarat ECG kerana kesederhanaan dan ketepatannya dalam pengesanan kompleks QRS. Algoritma ini diubah untuk digunakan bersama dengan *adaptive threshold* untuk pengesanan puncak-R dalam ECG. Input untuk ASIC ini adalah *Hardware Description Language* (HDL). Walau bagaimanapun, pengiraan intensif dan kerumitan dalam membina HDL dapat menurunkan prestasi masa yang boleh membawa kesan yang mengancam nyawa kepada pesakit. Melalui projek ini, pemecut perkakasan pengesan kompleks QRS telah dirancang dengan teknik pengoptimuman *Register Transfer Level* (RTL) untuk meningkatkan prestasi masa. Sebelum kod RTl dibinakan, algoritma telah dimodelkan dalam MATLAB untuk mengesahkan fungsinya. Untuk memaksimumkan penerokaan ruang reka bentuk dan meminimumkan masa reka bentuk kerana kerumitan HDL dalam pembinaan algoritma, Alat VIVADO HLS diperkenalkan dalam projek ini. Teknik gelung pembongkaran dan pipelining telah diguna untuk mengoptimumkan kod perkakasan dalam VIVADO HLS. Analisis mengenai latensi reka bentuk, penggunaan sumber, ketepatan dan jumlah masa pelaksanaan berkenaan dengan algoritma garis dasar dijalankan. Pada akhir projek ini, jumlah peningkatan berganda dicapai, dan 144455 kitaran dikurangkan setelah pengoptimuman dilakukan dalam kod perkakasan. Walau bagaimanapun, bilangan FF meningkat sebanyak 30% dari nombor asal sementara bilangan LUT meningkat sebanyak 17% dari nombor asal. Pada analisis reka bentuk ASIC, jumlah kawasan dan penggunaan kuasa masing-masing didapati 1.686mm2 dan 9.78mW. Dari hasil Synopsys Prime Time, *setup time* dan *hold time* reka bentuk dipenuhi.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

ECG	-	Electrocardiogram
VLSI	-	Very Large-Scale Integration
CVD	-	Cardiovascular Disease
HDL	-	Hardware Description Language
WT	-	Wavelet Transform
EMD	-	Empirical Mode Decomposition
HDL	-	Hardware Description Language
SA	-	Sinoatrial
DSP	-	Digital Signal Processing
HRV	-	Heart Rate Variability
HPF	-	High Pass Filter
LPF	-	Low Pass Filter
HLS	-	High Level Synthesis
RTL	-	Register Transfer Level
FF	-	Flip-Flop
LUT	-	Lookup Table
STA	-	Static Timing Analysis
PNR	-	Place and Route
ICC	-	IC Compiler
DC	-	Design Compiler
PT	-	Prime Time
STA	-	Static Timing Analysis
CTS	-	Clock Tree Synthesis

CHAPTER 1

INTRODUCTION

1.1 Background

Human heart consists of a four-chambered muscular organ, the upper two chambers is called atria and lower two chambers is called ventricles. Human heart is an organ that pumps blood throughout the whole body via the circulatory system. When the function or structure of the heart is get affected and not able to work well, this condition is called cardiovascular disease (CVD). Diagnosis of cardiovascular disease is highly dependent on the Electrocardiogram (ECG) signal analysis. ECG is a signal of heart muscle that provides information of electrical activity of the heart. Most cardiac abnormalities can be determined by using Electrocardiogram (ECG) and heart rate analysis. The main task of ECG signal analysis is to detect the heartbeat rhythm whether the heart beating is too fast, irregular or steady. However, ECG signal is contaminated by artefact such as power-line noise, motion artefact, instrumentation noise and EMG noise. All the noise will affect the originality of the ECG signal, therefore digital pre-processing techniques is crucial to enhance the ECG signal condition. The development of an efficient algorithms is important to analyse ECG signal.

Over the years, cardiovascular disease (CVD) has become a threat to human life. The increasing rate of CVD mortality has raised public concern to the diagnosis of CVD prediction. Irregular heartbeat cannot be ignored as it is one of the main factors that lead to severe CVD (1). According to the Star reporting (2), Ischaemic heart disease keep leading the main cause of death for the 14^{th} year in Malaysia. Ischaemic heart disease is one of the cardiovascular diseases when arteries of the heart cannot supply enough oxygen to the heart. Department of Statistics Malaysia (DOSM) revealed that there are on average 50 persons of people died in Malaysia because of

Ischaemic heart diseases every day. Tachycardia-bradycardia syndrome is one the heart rhythm disorder in which the heartbeat signal is too fast or too slow. Tachycardia and bradycardia may cause no symptoms, but it can lead to serious complications if it is left untreated. Thus, it is of the utmost important to detect heart problem at the early stage by frequently monitoring our heart activity through the usage of portable heart monitoring device.

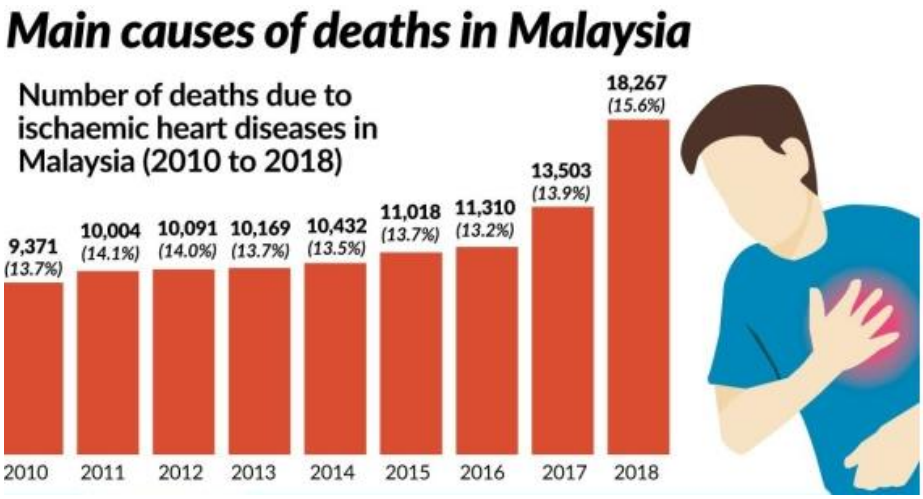

Figure 1.1 Number of deaths due to ischaemic heart diseases in Malaysia [2]

ECG has been utilized for a long time as a diagnostic tool in hospital. Gone are the days when ECG data is needed to interpret by a team of cardiologists. Nowadays, the market continues to evolve with new ECG monitoring device for healthcare facilities or for patients own carrying to monitor their heart rhythms every day. There are many ECG monitoring devices have been developed with current architecture of microcontroller, but it may not be the best in high speed performance. In addition, ECG data acquisition hardware must be robust enough to provide high accuracy in detection of irregular heartbeat so that there will no false alarm is being generated.

1.2 Problem Statements

In ECG processing, all the extensive analysis requires the information of QRS position as a basic. There are many approaches to QRS detection have been proposed.

Some QRS complex detection algorithm such as wavelet transform (WT), Hilbert transform and empirical mode decomposition (EMD) can achieve high accuracy but they are complex (3) and time-consuming (4). Another algorithm in detecting R-peak is called derivative-based algorithms. Derivative-based algorithm is simple to use and often used in real-time analysis but they are sensitive to noise (4–7) Thus, the chosen ECG signal processing algorithm must be noise-resistance, accurate and efficient in QRS complex detection.

In addition, there are various platforms available now for ECG signal processing such as microprocessor, microcontroller, Personal Computer (PC), mobile phone and digital signal processor. However, they have their own drawbacks in ECG signal processing. For example, microprocessor-based system is limited in performance by clock rate and sequential nature of their internal design. Sequential nature is the fetch-decode-execute cycle in microcontroller which is a time-consuming process in handling instruction (8). Other than that, PC is not suitable to be built as medical device due to its large sizing, the drawing of high power and its expensive price to build as medical device. In addition, mobile phone is also used as one of the platforms to implement ECG signal analysis. However, according to (9,10), electromagnetic interference from mobile phone can influence ECG signal recording. Alternatively, QRS detection is targeted to implement into VLSI design (FPGA or ASIC platform) in this project due to its low power consumption, smaller area and high operating speed of circuit.

The design running in VLSI platform is generally created using Hardware Description Language (HDL) such as Verilog, System Verilog and VHDL. The design nowadays getting more challenging and complex HDL coding is required to build the design. This will result to a longer design time and less flexibility when a sudden change is needed in a design. In (11) and (12), High Level Synthesis (HLS) is used to overcome the long testing time and to create effective RTL architectures by applying directives provided by HLS tool. Also, in (13), the authors illustrated both traditional way (RTL modelling) and modern way (HLS modelling) to design HDL block. At the end of the project, they found that HLS did a better optimization in term of performance and efficiency as compare to RTL modelling. Thus, by using High

Level Synthesis (HLS) which is compatible with C/C ++ language, designer is able to create, synthesize the code and translate the complex algorithms into register-transfer level (RTL) logic with less testing and debugging time on HDL code.

Most Digital Signal Processing (DSP) algorithms behave sequential in nature, simply use the algorithm into hardware design will often give disappointing results. Algorithms have to be transformed parallelism so that it can be applied effectively (14). To have an efficient design, we should refrain from using a compute intensive algorithm which can lead to high execution time. Algorithm is required to transform such that parallelism can be effectively applied. The performance of an operation can be accelerated by replicating hardware resources to perform the steps in parallel. Hence, compute intensive of an algorithm must be analysed and identified to exploit the inherent parallelism. The design of accelerators to involve parallelism should be enough but not more to avoid increase cost and power unnecessarily.

1.3 Objectives

Based on the design problem as mentioned previously, the objectives proposed for this study are:

i. To implement a suitable QRS complex detector by using high level synthesis (HLS) tool with its algorithm verified with Matlab.
ii. To identify and improve the compute intensive part of QRS complex detection algorithm in Vivado HLS.
iii. To analyse the performance of QRS complex detector in Vivado HLS and Synopsys for ASIC implementation.

1.4 Project Scope

In this study, several scopes have been outlined. Firstly, to detect ECG QRS complex, an algorithm must choose wisely. In this project, Pan and Tompkins algorithm is chosen due to its simplicity, efficiency and higher accuracy in detecting

R-peak (15,16). Pan and Tompkins is a most cited and widely used algorithm in many researches(17). The modelling and verification of the chosen algorithm will be done in PC by using Matlab software. Matlab is a powerful tool with the integration of computation, visualization, and programming where the problems and solutions are expressed in familiar mathematical notation. The equation provided by the Pan and Tompkins algorithm will be verified and output waveform will be plotted to measure its accuracy in detecting ECG QRS complex.

Next, QRS detection algorithm is implemented and run on Vivado HLS using C language with different optimization techniques. The result from Vivado HLS will then be analysed in terms of latency, total execution time and resource utilization. The output result from Vivado HLS is also compared with Matlab result to ensure its accuracy.

For ASIC implementation, a 90nm CMOS library is used to build ASIC layout. Design Compiler is used to translate RTL from Vivado HLS into netlist. IC Compiler is utilized to build the design layout. Prime Time is the tool in Synopsys for Static Timing Analysis (STA). At the end of the design, delay, area and power usage are extracted from Synopsys tool to analyse the result.

Lastly, the input ECG data is taken from online Physiobank database. Physiobank is a collection of physiological databases available on online website, it is often used by many researchers for development and evaluation of algorithms. Among more than 50 databases, MIT-BIH Normal Sinus Rhythm Database is chosen to be used for analysis and processing.

1.5 Thesis Outline

The aim of this project outline is to achieve project completing with planning, organizing and controlling with a desired time. This project is planned systematically according to the Gantt Chart in Table 1.1 and Table 1.2. Table 1.1 is the Gantt chart planning for Project I while Table 1.2 is the Gantt chart planning for Project II. FYP1

focus on problem formulation, literature review and algorithm modelling using Matlab. FYP2 focus on High Level Synthesis using Vivado HLS, code optimization, VLSI implementation using Synopsys and result discussion and analysis.

Table 1.1 Gantt Chart for Master Project I

Tasks	Sept 2019			Oct 2019				Nov 2019				Dec 2019		
	W2	W3	W4	W1	W2	W3	W4	W1	W2	W3	W4	W1	W2	W3
Problem formulation and literature review														
Understanding algorithm related to work														
Implementation of algorithm on MATLAB														
FYP 1 presentation														
Report Writing														

Table 1.2 Gantt Chart for Master Project II

Tasks	March 2020			April 2020				May 2020				June 2020			
	W1	W2	W3	W1	W2	W3	W4	W1	W2	W3	W4	W1	W2	W3	W4
VIVADO Tool Learning and Understanding															
Implementation of QRS detection algorithm in VIVADO HLS															
Perform RTL optimization technique in QRS algorithm code in VIVADO HLS															

Tasks	March 2020			April 2020				May 2020				June 2020			
	W1	W2	W3	W1	W2	W3	W4	W1	W2	W3	W4	W1	W2	W3	W4
Performance Analysis of RTL code in VIVADO															
Synopsys Tool Learning and Understanding															
Transfer RTL code from VIVADO into Layout design in Synopsys Tool															
Result Extraction and Performance Analysis in Synopsys															
Thesis Writing															

REFERENCES

1. Hanås S, Tidholm A, Holst BS. Ambulatory electrocardiogram recordings in cats with primary asymptomatic hypertrophic cardiomyopathy. J Feline Med Surg. 2017;19(2):158–64.
2. Star T. Heart attack leading cause of death | The Star Online [Internet]. 2019 [cited 2019 Nov 21]. p. 1. Available from: https://www.thestar.com.my/news/nation/2019/10/31/heart-attack-leading-cause-of-death
3. Desai V. Electrocardiogram (ECG/EKG) using FPGA. San Jose State University; 2012.
4. Yang D, Zhang Y. A Real-time QRS Detector Based on Low-pass Differentiator and Hilbert Transform. In: MATEC Web of Conferences. EDP Sciences; 2018. p. 2–4.
5. Benitez DS, Gaydecki PA, Zaidi A, Fitzpatrick AP. New QRS detection algorithm based on the Hilbert transform. In: Computers in Cardiology. IEEE; 2000. p. 379–82.
6. Subramanian B. ECG signal classification and parameter estimation using multiwavelet transform. Biomed Res. 2017;28(7):3187–93.
7. Bae TW, Kwon KK. Efficient real-time R and QRS detection method using a pair of derivative filters and max filter for portable ECG device. Appl Sci. 2019 Oct 1;9(19):4128.
8. Reg Zatrepalek HI. Using FPGAs to solve tough DSP design challenges [Internet]. EE times. 2012. p. 1–4. Available from: https://www.eetimes.com/using-fpgas-to-solve-tough-dsp-design-challenges/#
9. Buczkowski T, Janusek D, Zavala-Fernandez H, Skrok M, Kania M, Liebert A. Influence of Mobile Phones on the Quality of ECG Signal Acquired by Medical Devices. Meas Sci Rev. 2013;13(5).
10. Jones A. Cell Phones Cause Electromagnetic Interference With Implantable Cardioverter Defibrillators [Internet]. HCT America. 2015. Available from: https://hctamerica.com/technology-news/cell-phones-cause-electromagnetic-interference-with-icds/

11. Ramzan OKNAKGC. Design and Evaluation of Vivado HLS-Based Compressive Sensing for ECG Signal Analysis. IEEE 16th Int Conf Dependable, Auton Secur Comp, 16th Int Conf Pervasive Intell Comp, 4th Int Conf Big Data Intell Comp, 3rd Cyber Sci Tech Cong. 2018;457–61.
12. Tsoutsouras V, Koliogeorgi K, Xydis S, Soudris D. An Exploration Framework for Efficient High-Level Synthesis of Support Vector Machines: Case Study on ECG Arrhythmia Detection for Xilinx Zynq SoC. J Signal Process Syst. 2017 Aug 1;88(2):127–47.
13. Tsiktsiris D, Ziouzios D, Dasygenis M. A High-Level Synthesis Implementation and Evaluation of an Image Processing Accelerator. Technologies. 2018 Dec 23;7(1):4.
14. Khalil-Hani DM. Design of Digital Systems II: RTL System Verilog and High-Level Synthesis. 2019. 1–199 p.
15. Kher R, Vala D, Pawar T, Thakar VK. Implementation of derivative based QRS complex detection methods. In Institute of Electrical and Electronics Engineers (IEEE); 2010. p. 927–31.
16. Nahiyan KMT, Al-Amin A. Acceptable ECG trace selection based on Pan-Tompkins algorithm. In: 2016 5th International Conference on Informatics, Electronics and Vision, ICIEV 2016. Institute of Electrical and Electronics Engineers Inc.; 2016. p. 731–6.
17. Tompkins WJ. A Real-Time QRS Detection Algorithm. Vol. 32, IEEE TRANSACTIONS ON BIOMEDICAL ENGINEERING. 1985.
18. Rabbani H, Parsa Mahjoob M, Farahabadi E, Farahabadi A. R peak detection in electrocardiogram signal based on an optimal combination of wavelet transform, Hilbert transform, and adaptive thresholding. J Med Signals Sens. 2011 May 1;1(2):91–8.
19. Shufni SA, Mashor MY. ECG signals classification based on discrete wavelet transform, time domain and frequency domain features. In: 2015 2nd International Conference on Biomedical Engineering, ICoBE. Institute of Electrical and Electronics Engineers Inc.; 2015. p. 2.
20. Vastarouchas C, Kapoulea S, Psychalinos C. ECG signal acquisition for the Pan-Tompkins algorithm using current-mirror filters. In: 2016 IEEE International Conference on Electronics, Circuits and Systems, ICECS 2016.

Institute of Electrical and Electronics Engineers Inc.; 2017. p. 317–20.

21. Mundhe P, Pathrikar AK. An Overview of Implementation of Efficient QRS Complex Detector with FPGA. Int J Adv Res Comput Commun Eng. 2013;2(10):4041–3.
22. Resources PL. A Beginners Guide to Normal Heart Function, Sinus Rhythm & Common Cardiac Arrhythmias [Internet]. Cardiology Teaching Package. 2015. p. 1–3. Available from: https://www.nottingham.ac.uk/nursing/practice/resources/cardiology/function/normal_duration.php
23. Vijjaya V, Rao KK, Sahrudai P. Identification of sudden cardiac arrest using the Pan-Tompkins algorithm. In: Proceedings - 2012 14th International Conference on Modelling and Simulation, UKSim 2012. 2012. p. 97–100.
24. Sornmo LPL. Electrocardiogram (ECG) Signal Processing. John Wiley & Sons, Inc. 2006;1–14.
25. Rosu MC, Hamed Y. Methods for Denoising the ECG Signal in Wearable Systems. In: Proceedings of the 2015 7th International Conference on Electronics, Computers and Artificial Intelligence. Institute of Electrical and Electronics Engineers Inc.; 2015. p. 1–5.
26. Gacek A, Pedrycz W. ECG signal processing, classification and interpretation: A comprehensive framework of computational intelligence. ECG Signal Processing, Classification and Interpretation: A Comprehensive Framework of Computational Intelligence. Springer-Verlag London Ltd; 2014. 1–47 p.
27. bu Md. Numan-Al-Mobin, Sheikh Md. Rabiul Islam, Md. Rezwanul Haque MH. 16-Bit Embedded Microprocessor for Information System Using FPGA. Glob J Res Eng Electcical Electron Eng. 2011;11(7):39–43.
28. Hardman S, Steinberger-Wilckens R. Mobile phone infrastructure development: Lessons for the development of a hydrogen infrastructure. In: International Journal of Hydrogen Energy. Elsevier Ltd; 2014. p. 8185–93.
29. Buczkowski T, Janusek D, Zavala-Fernandez H, Skrok M, Kania M, Liebert A. Influence of mobile phones on the quality of ECG signal acquired by medical devices. Meas Sci Rev. 2013 Oct;13(5):231–6.
30. Bayasi N, Saleh H, Mohammad B, Ismail M. 65-nm ASIC implementation of QRS detector based on Pan and Tompkins algorithm. In: 2014 10th

International Conference on Innovations in Information Technology, IIT 2014. Institute of Electrical and Electronics Engineers Inc.; 2014. p. 84–7.

31. Jain SK, Bhaumik B. An energy efficient application specific integrated circuit for electrocardiogram feature detection and its potential for ambulatory cardiovascular disease detection. Healthc Technol Lett. 2016;3(1):77–84.
32. Li Q, Alemzadeh H, Kalbarczyk Z, Iyer RK. A fault-tolerant hardware architecture for robust wearable heart rate monitoring. In: Proceedings of the 2015 9th International Conference on Pervasive Computing Technologies for Healthcare, PervasiveHealth 2015. Institute of Electrical and Electronics Engineers Inc.; 2015. p. 185–92.
33. German-Sallo Z. Signal Processing using FPGA Structures. Procedia Technol. 2014;12:112–8.
34. Hashim MA, Wen Hau Y, Baktheri R. Efficient QRS complex detection algorithm implementation on soc-based embedded system. J Teknol. 2016;78(7–5):49–58.
35. Gutiérrez-Rivas R, García JJ, Marnane WP, Hernández Á. Novel Real-Time Low-Complexity QRS Complex Detector Based on Adaptive Thresholding. IEEE Sens J. 2015 Oct 1;15(10):6036–43.
36. Cacciotti M, Camus V, Schlachter J, Pezzotta A, Enz C. Hardware Acceleration of HDR-Image Tone Mapping on an FPGA-CPU Platform Through High-Level Synthesis. In: International System on Chip Conference. IEEE Computer Society; 2019. p. 158–62.
37. Ryan M V. FPGA Hardware Accelerators - Case Study on Design Methodologies and Trade-Offs. Rochester Institute of Technology Rochester; 2013.
38. Xilinx Inc. Increasing Local Memory Bandwidth [Internet]. Xilinnx Support Documentation. 2015 [cited 2020 Jul 8]. p. 1. Available from: https://www.xilinx.com/support/documentation/sw_manuals/xilinx2015_2/sdsoc_doc/topics/calling-coding-guidelines/concept_increasing_local_memory_bandwidth.html
39. Kher R, Gohel S. Digital Signal Processor (Tms320c6713) Based Abnormal Beat Detection from ECG Signals. Int J Appl Sci Res Rev. 2018;5(2):7.
40. Ragnarsson F. A portable ECG system for real-time arrhythmia classification.

Uppsala University; 2019.

41. Jain SK, Bhaumik B. An ultra low power ECG signal processor design for cardiovascular disease detection. In: Proceedings of the Annual International Conference of the IEEE Engineering in Medicine and Biology Society, EMBS. Institute of Electrical and Electronics Engineers Inc.; 2015. p. 857–60.
42. PhysioBank ATM [Internet]. [cited 2019 Dec 8]. Available from: https://archive.physionet.org/cgi-bin/atm/ATM
43. Hamilton PS, Tompkins WJ. Quantitative Investigation of QRS Detection Rules Using the MIT/BIH Arrhythmia Database. IEEE Trans Biomed Eng. 1986;BME-33(12):1157–65.
44. Johansson A, Johansson J. High-Level Synthesis for Efficient Design and Verification. Lund University; 2020.
45. Introduction to High-Level Synthesis with Vivado HLS [Internet]. XILINX. 2013 [cited 2020 May 22]. Available from: http://users.ece.utexas.edu/~gerstl/ee382v_f14/soc/vivado_hls/VivadoHLS_Overview.pdf
46. Lockhart D. Introduction to the ECE5745 ASIC Toolflow ECE5745 Tutorial 0 (Version 606ee8a) [Internet]. 2016 [cited 2020 May 30]. Available from: http://www.csl.cornell.edu/courses/ece5745/syndocs