A 2.5-GHz Optical Receiver Front-end in a 0.13 μm CMOS Process for Biosensor Application

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***Abstract*— This paper presents a low-noise and low-power transimpedance amplifier (TIA,) intended for use as an analog frontend for a very low biomedical signal detection. Different topologies are reviewed, and then the most appropriate structures are characterized. A common gate transimpedance amplifier has been designed in 0.13 μm CMOS process. Experimental results obtained show that the TIA connected to a Geiger mode photodiode with a total capacitance of 2 pF performed a bandwidth of 2.47 GHz with transimpedance gain of 53.8 and input referred current noise of 28.1 pA/(Hz)$^{1/2}$ by using regulated cascade topology. The core circuit of the poposed analog front-end receiver occupies a chip area of 900 μm^2 with power dissipation of 1.8 mW. These encouraging results have exhibited the potential of the circuit for use in the CMOS photon detector for biomedical sensing application.**

Keywords—transimpedance amplifier, low voltage, photodiode, common gate

I. INTRODUCTION

The application of high-speed optical receiver is essentially devoted as the analog front-end receiver have been developed and widely for the detection of low light level detection in astronomy, laser ranging, optical timedomain reflectometry (OTDR), single molecule detection, fluorescence decay, biomedical imaging and etc [1], [2]. An analog front-end optical receiver (AFRX) is commonly consisting of photodiode (PD) as the sensor, transimpedance amplifier and output buffer. The transimpedance amplifier (TIA) converts the photocurrent signal which is detected by the PD into a voltage. However, the performances of PD implemented in standard CMOS process which is drive out through the ouput buffer have low detection efficiency due to shallow PN junctions and premature breakdown [3-5]. Furthermore, detection bandwidth is limited by slow diffusion of photogenerated carriers in the charge neutral region [3].

In recent studies, the analog front-end optical receiver circuit which have been implemented by many researchers encounters many design challenges to attain high speed and low noise features [4, 6-8]. The noise, gain, and bandwidth (BW) of the TIA impact the overall speed and sensitivity of the AFRX directly. As the trend of CMOS IC technologies is to scale down voltage supply to achieve low power requirement, raising the difficulty to design a TIA with low noise, high gain and high BW [9, 10].

The AFRX have two major problems. First, the parasitic capacitance (pCAP) of the PD is large, usually a few pico Farads. This pCAP is the dominant capacitance to the input of the TIA. Large pCAP means the input pole is small, hence that the cutoff frequency due to input pole is small. The PD's pCAP effect significantly limited the BW of the entire system. Thus, this effect must be relaxed by designing the input impedance of the TIA to be as small as possible for the system to operate in gigahertz (GHz) frequency range. In addition, the photocurrent signal from PD usually is very weak, depending on the type of PD, the current magnitude can be as small as a few ten micro Ampere (μA), thus sensitive to noise [4, 11]. A large pCAP will introduce considerable large amount of input referred noise current (IRNC) to the input of the TIA [12]. This poses a risk of data loss as the input current signal of the TIA is subjected to noise. To ensure the input current signal to be amplified and converted to voltage signal accurately, the noise and gain performance of the TIA must be designed to be sufficiently robust to separate the weak current signal from the noise.

There are various TIA topologies and performance improvement techniques have been designed and characterized earlier by the other researchers. For TIA topology, the simplest one will be the single stage TIA which employs only one stage usually is a common gate (CG) or common source (CS). In earlier studies, some researchers proposed a single CG stage TIA with self-bias current source device implemented 0.18 μm CMOS process [13]. This TIA employed inductive shunt peaking technique to boost the BW. The circuit was tested with input signal of 1mA amplitude and the pulse frequency of 25 GHz for the pCAP of 0.15 pF. A BW range of 20 GHz with a TI gain of 44.5 dBΩ and a small input-referred current noise (IRCN) of 22 pA/(Hz)1/2 were obtained through post-layout simulation. These characterization performances indicate the possibility of designing TIA with low power, low noise, high gain and high BW in low voltage CMOS technology. However, a single stage TIA will not robust enough to meet all the design specifications. Thus, more stages will be added to it and resulted in multi-stage TIA topologies [12, 13]. In multi-stage topologies, more than one stage is employed in the amplifier. For industrial CMOS process, it usually incorporated three basic MOSFET amplifier configurations which are CG, CS and common drain (CD) configuration. A very comprehensive work of optical AFRX circuit with the integration of PD and TIA was demonstrated in 0.35 μm CMOS technology by M.Li et. al [4]. The TIA circuit employed regulated cascode (RGC) input stage, CS as gain stage and CD as the output stage. Inductive series peaking and feedback techniques adopted to enlarge the BW. The TIA was considered as an open-loop TIA as the feedback is added internally (feed 2nd stage output back to 2nd stage input instead of the final output back to the input stage). Despite the extremely weak current signal and substantially large pCAP of 0.71 pF, Li's TIA [4] demonstrated BW of

6.02 GHz with TI gain of 51 dBΩ and small IRCN of 21 pA/(Hz)1/2. As reported in this work, the TIA's BW degraded to 3.2 GHz with slightly drop in TI gain to around 48 dBΩ when voltage supply reduced to 2.5 V. This indicates that the TIA might not be feasible in a low voltage CMOS process. Besides, for the headroom (output voltage swing) critical application, TIA in differential form also had been demonstrated recently to achieve higher voltage signal swing. Other than various types of TIA topology, techniques such as feedback, inductive peaking and zero compensation also can be incorporated into the basic TIA topologies to further enhance the noise, gain and BW performance [9, 14, 15].

In this paper the design and characterization performances of AFRX consists of a geiger mode PD simulation model and TIA circuits will be discussed in the following sections by considering a 2.5 GHz BW with sufficiently large gain, good noise performance and low TIA input impedance. Section II explains the light detection implementation with a Geiger mode photodiode simulation model. The proposed common gate TIA circuits and the amplification improvement in detecting the signals from Geiger mode photodiode simulation model are described in Section III. The simulation performances of the basic common gate and regulated common gate TIA are analyzed in Section IV. Layout and optimized simulation measurements are also presented in Section IV. Finally, conclusions are given in Section V.

II. CMOS PHOTODETECTION SIMULATION MODEL

The main focuses of optical receiver analog front-end design are particularly considered the geiger mode PD and TIA, as shown in Fig. 1. The amplification stage followed the geiger mode photodiode must be well-designed to amplify the detected signal using a low voltage CMOS process device. Hence, low input impedance amplifier topology such as common gate (CG) transimpedance amplifier (TIA) is usually employed. A geiger mode PD detector is implemented by using single photon avalanche diode (SPAD) simulation model as shown in Fig. 2. The circuit is adopted from Dalla Mora [3] and redesigned in Siltera 130 nm CMOS process to generate the photon detector signal to predict the electronic behavior of the avalanche current ignition, quenching and recovery process with passive quenching circuit. In order to properly count for quenching and recovery times, some parasitic components must be considered, as in traditional SPAD model. C_{ac} is a junction capacitance while C_{cs} and C_{as} are the stray capacitances from anode and cathode to substrate (typically in the order of picofarad). The diode resistance R_{spad} is given by the sum of the space-charge resistance and the resistance of neutral regions crossed by the avalanche current. V is the breakdown voltage and the transistor control the avalanche triggering [11-13]. A pulse voltage is used to represent the arrival of photon. However, this SPAD simulation model is designed to initiate a photon signal to the SPAD and the performance of this circuit may vary from the fabricated SPAD. The breakdown voltage and the transistor control the avalanche triggering is indicated by "V" and the photon input is presented by the voltage pulses to represent the arrival of photon. The small photocurrents from the geiger mode PD need to be amplified as soon as possible to overcome the dark noise effect on the front end optical receiver circuit.

III. TRANSIMPEDANCE AMPLIFIER CIRCUIT DESIGN

The transimpedance amplifier(TIA) circuit design is important for the AFRX implementation which is reported in this paper. The circuit design must consider to improve the sensitivity and speed of the AFRX. The proposed TIA circuit based on regulated cascode configuration (RGC) and is adapted from Li et. al [4] has been implemented using a low voltage Siltera 0.13µm CMOS process. The RGC circuit diagram is shown in Fig. 3.

Consequently, the chosen RGC TIA was previously implemented using Austria Microsystem 0.35 µm CMOS process [4]. Therefore, the proposed circuit needs to be analysed and designed to meet the target BW of 2.5 GHz. The mathematical analysis of the TIA input stage is presented in the following context. From the equations derived, the trade-off and relationship between circuit components and parameters can be comprehended. The knowledge is applied to design the circuit to meet the target BW. The success of designing the circuit to reach 2.5 GHz BW proves that the RGC input stage is capable of meeting the BW requirement of optical AFRX using a geiger mode PD with pCAP of 2 pF, in a 0.13 µm CMOS process with the supply voltage of 1.2 V.

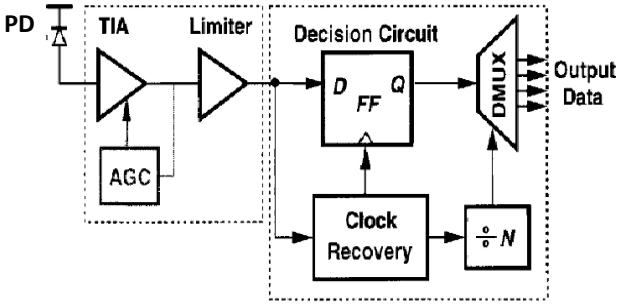


Fig. 1. The schematic of optical receiver analog front-end circuit

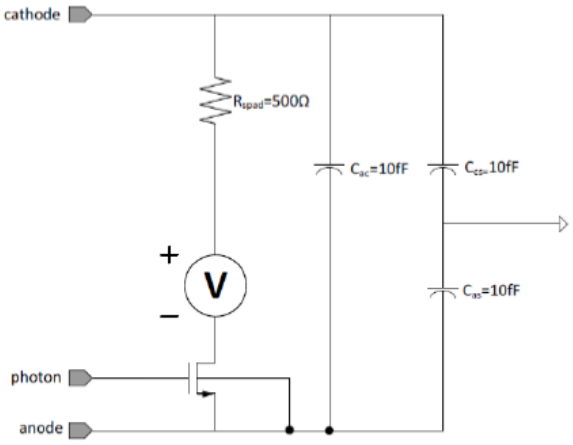


Fig. 2. Single photon avalanche diode simulation model

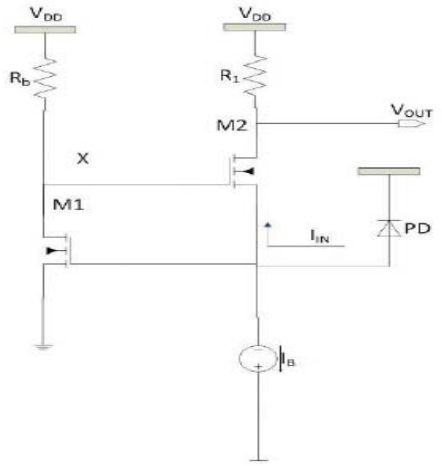


Fig. 3. Input stage of proposed RGC TIA

A. Small Signal Circuit Analysis

The small signal analysis is performed on both the low-frequency model and high-frequency model to derive the equation of TI gain (R_T), input impedance (R_{IN}) and transfer function (T_F). For the low frequency, the capacitance is considered as open circuit. Therefore, the small signal model (SSM) is drawn separately for M1 and M2, as shown in Fig. 4. Note that, the body effect is ignored to reduce the complexity of analysis. The R_T and R_{IN} can be derived from these SSMs.

Referring to Fig. 4, all current signal at the input node will flow through R_1. Therefore, TI gain is actually equal to R_1 as shown in (1).

$$R_T = \frac{v_{out}}{i_{in}} = R_1 \tag{1}$$

By applying Kirchoff's Current Law (KCL) at node X, v_x can be written in term of v_{in} as in (3).

$$\frac{v_x}{R_b \| r_{o1}} = g_{m1} v_{in} \tag{2}$$

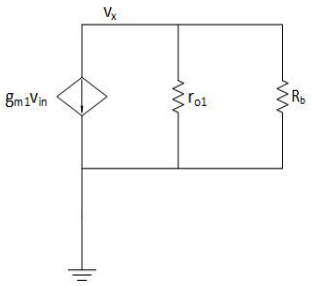
$$v_x = g_{m1}(R_b \| r_{o1}) v_{in} \tag{3}$$

To obtain the equation of R_{IN}, KCL is applied at node v_{in} of SSM in Fig. 4 and (4) is obtained. R_{IN} is derived in (5) by substitute (3) into (4).

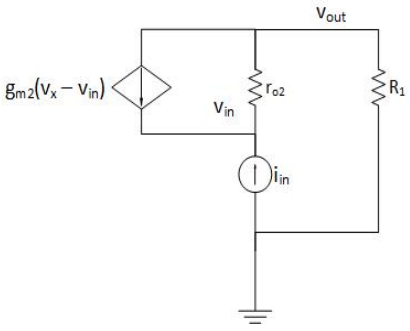
$$g_{m1}(v_x - v_{in}) + i_{in} + \frac{i_{in} R_1}{r_{o1}} - \frac{v_{in}}{r_{o2}} = 0 \tag{4}$$

$$R_{IN} = \frac{v_{in}}{i_{in}} = \frac{(\frac{1}{R_1} + \frac{1}{r_{o2}})R_1}{g_{m2}[g_{m1}(R_b \| r_{o1}) + 1] + \frac{1}{r_{o2}}} \tag{5}$$

A simplified high-frequency SSM is shown in Fig. 5 by neglecting the output load. Some of the capacitors in the SSM are lumped capacitor. Therefore, the channel modulation effect (CME) is ignored in the high-frequency model to ease the analysis. This simplified SSM is used to derive the transfer function (T_F) of $i_{out}(s)/i_{in}$ (s) as given in (6).



(a) Small signal model of M1



(b) Small signal model of M2

Fig. 4:

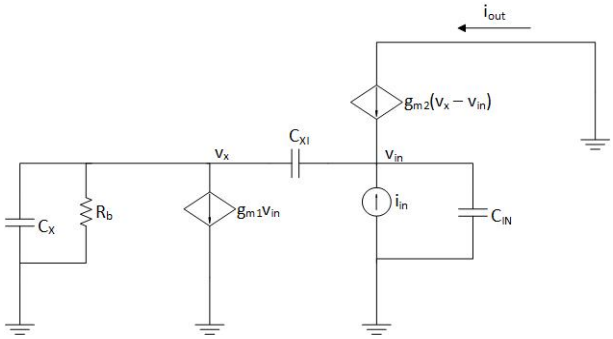


Fig. 5: Simplified high-frequency SSM

$$\frac{i_{out}(s)}{i_{in}(s)} = \frac{1 + \frac{s}{z_1}}{1 + \frac{s}{Q\omega_n} + \frac{s^2}{\omega_n^2}} \tag{6}$$

The BW can be estimated as (7) which is suggested that to achieve high BW, the R_b, R_{IN} and C_{IN} need to be small [4]. The C_{IN} is dominated by C_{PD} which normally is a fixed value. Therefore, for a fixed C_{PD}, R_{IN} and R_b need to small enough to meet target BW. By increasing the value of R_b will help to reduce R_{IN} but R_b cannot be too large as it might nullify the effect of the reduced R_{IN}. Nevertheless, the R_{IN} also can be manipulated by changing the size of transistor M1 and M2 or the g_m.

$$\omega_n^2 = \frac{g_{m2}(g_{m1} \| \frac{1}{R_b})}{(C_{xi}C_x + C_{xi}C_{in} + C_xC_{in})} = \frac{1}{R_b R_{in} \sum C^2} \tag{7}$$

B. Diode connected PMOS load

For the circuit in this project, only pmos is suitable to use according to the circuit DC operating point. Therefore, the diode-connected pmos is considered as another option. In term of process variation, both the poly-silicon resistor and the diode-connected pmos load are about the same in the 0.13 µm process (Zhang *et al.*, 2012). The study suggests the off-chip resistor ballast resistor can be subsitute with poly-silicon resistor and the diode-connected pmos load. Nevertheless, the optimized RGC TIA is realized using the diode-connected pmos load as shown in Fig. 6. This circuit performance is important for the design of the subsequent stage which aim to further amplify the signal to a rail-to-rail digital signal. Hence that, the decision on selecting pmos or nmos as input device for the second stage and also the voltage reference point will be considered.

IV. Simulation Results And Layout

Post layout simulation is performed on the designed TIA with the parasitic extracted from the layout of the two sub-circuits which are the RGC_cell and the current_mirror. The schematic of the proposed RGC TIA with two-subcircuits is depicted in Fig. 7. The BW and TI gain of the RGC TIA circuit is obtained from AC simulation using Mentor Graphics Spectre simulation with worst case C_{PD} of 2 pF. These results are depicted in Fig. 8. The BW of RGC3 is 1.90GHz while for CG4 is 1.76G, measured at the -3dB point. The TI gain for RGC3 and CG4 are 54dBΩ and 43.7 dBΩ respectively. The BW is 2.47 GHz when C_{PD} is 2 pF and doubled to 5.0 GHz when C_{PD} dropped to 0.5 pF, where the TI gain is 54 dBΩ. The transient simulation as depicted in Fig. 9 has been performed to determine whether the circuit is receiving the current signal correctly. The input signal applied to the circuit is a current signal quenching at 2.5GHz with 1mA amplitude. It models the actual current signal comes from PD. The output voltage signal swing of these TIAs are determined from the output waveforms. For RGC, the signal swing is around 500mV, $V_{OUT(max)}$ and $V_{OUT(min)}$ are 1.2V and 0.7V respectively. For CG4, $V_{OUT(max)}$ and $V_{OUT(min)}$ are 1.08V and 0.78V respectively. Therefore, signal swing is about 300mV, which is smaller compared RGC3. This result is important for the design of the subsequent stage which aims to further amplify the signal to a rail-to-rail digital signal. It determined whether PMOS or NMOS should be used as input device for the second stage and also the voltage reference point. These results have proven two things, first, the TIA designed is capable of acheiving 2.5 GHz BW target at worst case C_{PD} for Geiger mode PD. Second, the BW is significantly depends on the C_{PD}, reducing the C_{PD} improves the BW. This is agreed with the analysis in section III. The TI gain is 53.8 dBΩ. The input refered voltage noise (IRVN) can be obtained from the AC noise simulation, which is 0.86 nV/(Hz)$^{1/2}$ at 2.5 GHz.

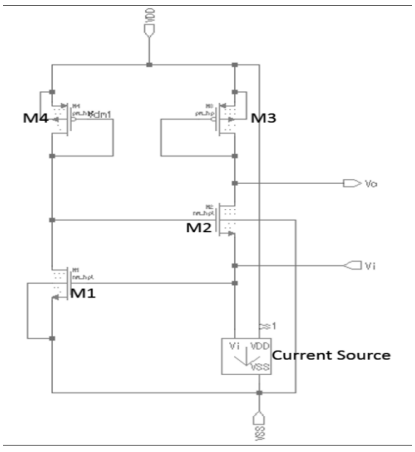
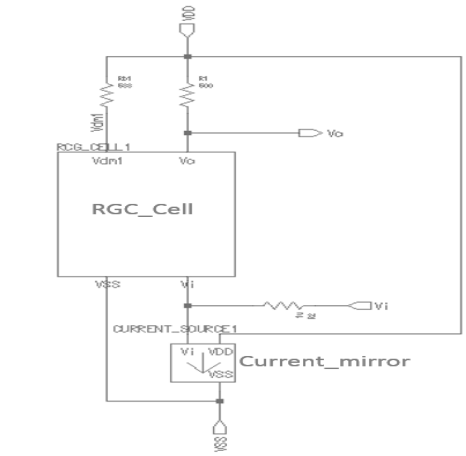
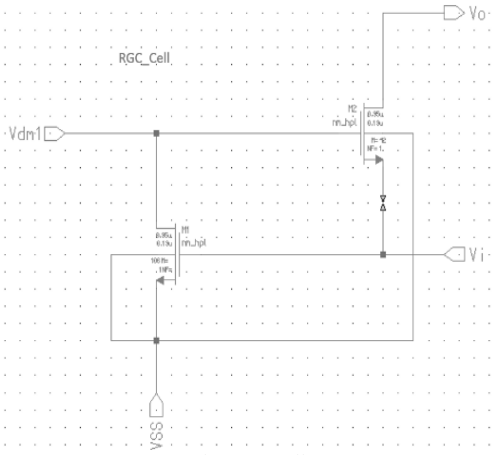


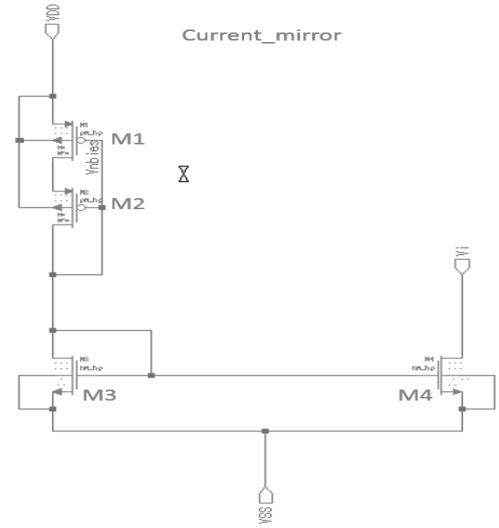
Fig. 6: RGC TIA with diode-connected pmos load



(a) The schematic of the proposed RGC TIA

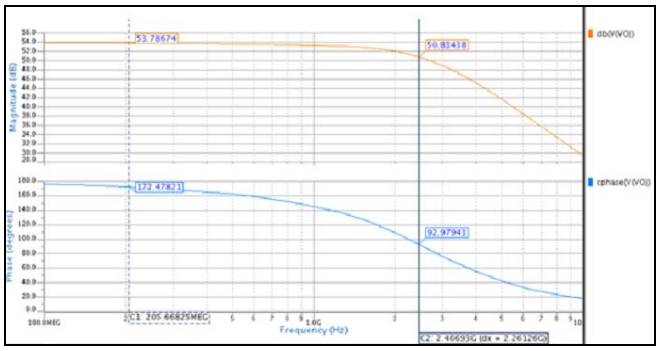


(b) RGC cell

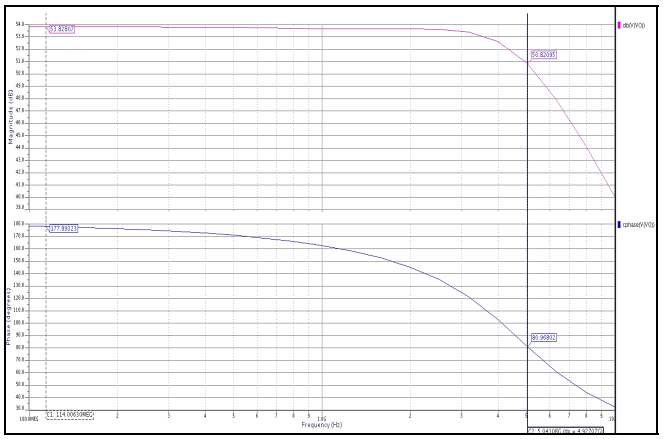


(c) current mirror

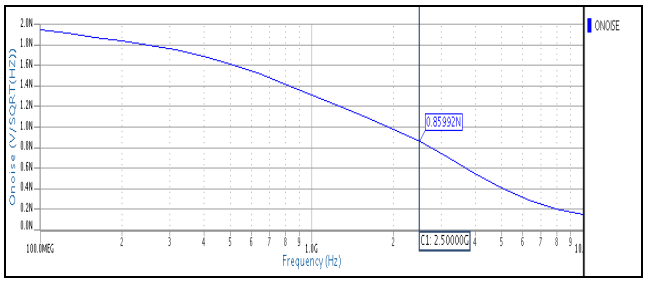
Fig. 7: The proposed RGC TIA with two-subcircuits



(a) Bode plot at C_{PD} = 2 pF



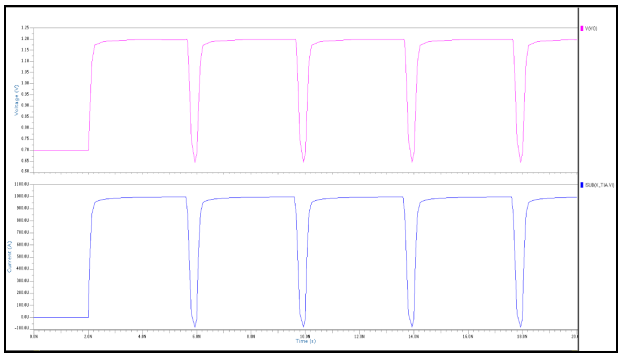
(b) Bode plot at C_{PD} = 0.5 pF



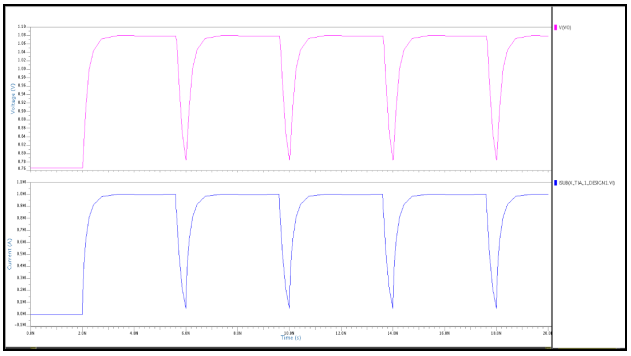
(c) IRVN at 2.5 GHz with 2 pF C_{PD}

Fig. 8: Plotted graphs of AC simulation

The performance of the designed TIA and others recents proposed TIA are summarized in Table 1. All these TIAs are in the same process technology, therefore, meaningful comparison can be made. Compared to the TIA by Taghavi *et al.*[10], which is also a RGC type TIA. The designed TIA gives better TI gain, lower IRCN and power consumption. The BW is low because C_{PD} of this work is eight times larger. On the other hands, the performance of the designed TIA is also comparable to the TIA by Ray and Hella [11] before any enhancement technique is employed to boost its performance. The BW of the TIA by Ray and Hella [11] is higher due to two reasons. First, it employs Shunt feedback technique to reduce R_{IN}. Second, the C_{PD} is half compared to this work.



(a) Input and Output signal of RGC3 input stage



(b) Input and Output signal of RGC4 input stage

Fig. 9: Transient simulation performances RGC3 and RGC4 input stages

V. CONCLUSIONS

The result shows that RGC topology outperforms CG-CSFB topology and CS topology. Hence, it is employed in this project and designed to meet 2.5 GHz BW with the use of off-chip resistor load. The objectives are accomplished as the designed TIA archived a BW of 2.47 GHz with TI gain of 53.8 dBΩ using Geiger mode PD with 2 pF CPD and 1 mA IPD. The IRCN are reasonable as compared to other recent proposed TIAs, it is considered small. The replacement of off-chip resistor with DCPL degrades the circuit performance. Circuit with DCPL is not capable of meeting 2.5 GHz.

TABLE I. PERFORMANCE SUMMARY OF THE PROPOSED RGC TIA

Specification	**Table Column Head**		
	This work	(Taghavi *et al.*, 2015)	(Ray and Hella, 2018)
Topology Type	**RGC**	RGC	CG
Enhancement technique	**No**	No	Yes. Shunt feedback
BW (GHz)	**2.47**	7.0	7.0
TI gain (dBΩ)	**53.8**	50.0	53.0
IRCN ($A/(Hz)^{1/2}$)	**28.1 p**	31.0 p	27.0 u
output signal swing (V)	**470 m**	NA	NA
R_{IN} (Ω)	**30.6**	NA	NA
Supply (V)	**1.2**	1.5	1.2
Power (mW)	**1.8**	7.0	1.44
Area (μm^2)	**900**	NA	NA

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