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COMPREHENSIVE MULTISITE EFFICIENCY EQUATION FOR SEMICONDUCTOR TEST EQUIPMENT

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Abstract

Multisite efficiency (MSE) determines the effectiveness of improving multisite testing throughput, which ultimately affects the cost of tests. As indicated by International Technology Roadmap for Semiconductors 2.0 2015 Edition a decrease of the MSE relative to the test site increment has a negative effect on the testing throughput improvement. However, calculating the MSE accurately needs to consider all related variables such as test time, unit indexing time, tray exchange sequence time, testing yield, jam rate, and production capacity. The MSE equations identified from the previous literature are inaccurate and do not reflect the actual MSE situation. This study develops an equation which incorporates all the relevant variables for better prediction of testing throughput and the cost of test.

Keywords: Concurrent test, Cost of test, Multisite efficiency, Multisite testing, Parallel test..

1. Introduction

The semiconductor cost of manufacturing is crucial because the average selling price (ASP) of semiconductor chips continues to decrease. Over a 10-year period, the ASP had decreased by 36% [1] as shown in Fig. 1.

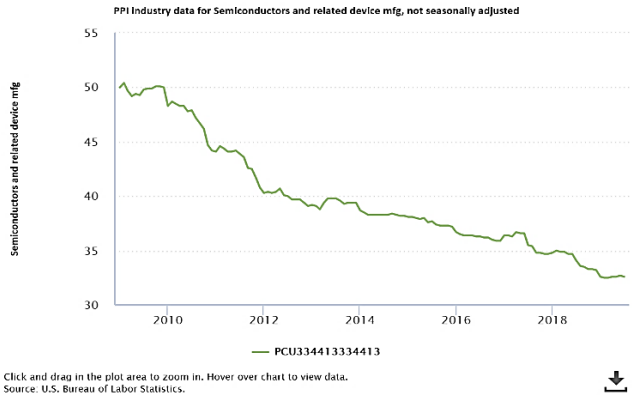

Fig. 1. PPI industry data for semiconductors and related devices (Adapted from [1]).

Effort has been exerted to overcome issues in the cost of manufacturing, which include assembly and test equipment cost, which are predicted equal [2] as illustrated in Fig. 2. Assembly equipment costs have been reduced but the test equipment cost is predicted to increase relatively with the increment of transistors per chips [3-5], which requires longer testing processing time and hardware resources. To overcome this problem, the industry has introduced multisite testing approaches for parallel testing of multiple chips.

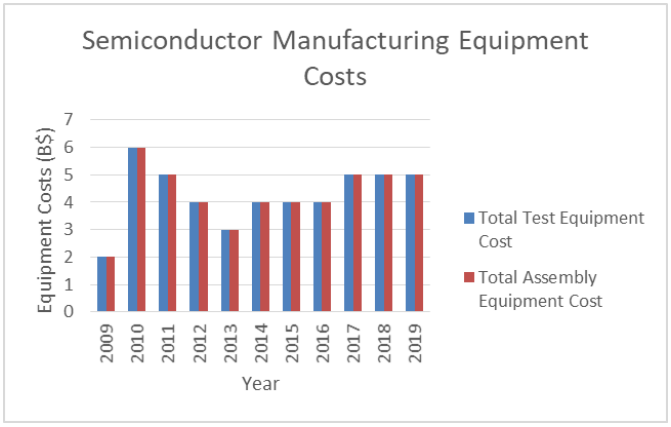

Fig. 2. Semiconductor total test equipment cost versus total assembly equipment cost (Adapted from [2]).

The main goal of multisite testing is to ensure that the testing throughput increases by adding test sites. However, as predicted by [2, 6, 7], the testing throughput of multisite testing depends on the multisite efficiency (MSE), as shown

in Fig. 3. If the increment of the test site causes the inefficiency of the test equipment to produce throughput, then the multisite testing will not be able to improve the throughput as expected. In this case, the inefficiency of the MSE cannot reduce the cost of the test but may be more expensive than the lower test site configuration, where the cost of the test involves three main investments: tester, test handler, and test accessories [2]. Therefore, the MSE needs to sustain the acceptable performance relative to the test site increment to improve the testing throughput. Thus, the cost of the test can be reduced, where per unit cost (average cost) is equal to total cost over total output [8, 9].

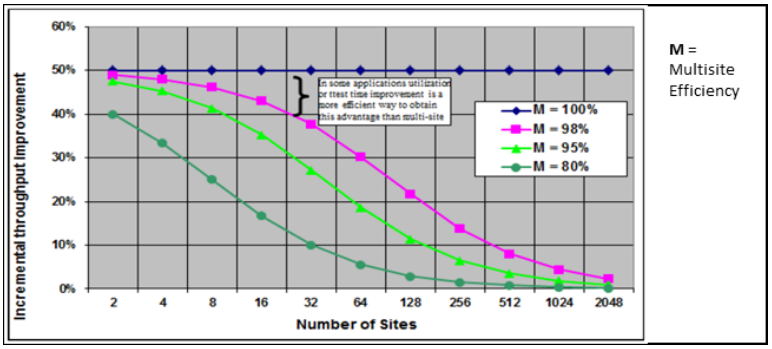

Fig. 3. Effect of multisite efficiency on testing throughput relatively with the number of test site (Adapted from [2]).

However, all the previous MSE studies consider the testing time, number of test sites, and unit indexing time as the variables to calculate the MSE [10-16]. The same equation is used by [2], where it is inaccurate because the MSE is also affected by other variables shown in Table 1. The testing process flow in Fig. 4 shows that before the semiconductor chips are tested, they need to be transferred from the input carrier, such as JeDex tray to the test site, which involves multiple variables included the tray exchange frequency, which is affected by the tray matrix. The transfer process is measured by the stability of the task, which is the jam rate. In addition, the different test site configurations affect the testing yield due to the contact positioning accuracy and electrical resistance [17]. The equipment utilization affects the cost because the increment of the production capacity requires additional test equipment where the utilization percentage varies [10]. Therefore, calculating the MSE with all the related variables is important to determine the actual situation instead of only the test and unit indexing times. This study takes the initiative to develop the equation, which includes all the multisite testing variables so that the accurate value can be obtained. This development is important for the cost of test study and test equipment selection process in the future.

2. Development of New Multisite Efficiency Equation

As discussed, the current multisite efficiency (MSE) equation only considers the unit indexing time, number of test site, and testing time, which is inaccurate. The reason is that other important variables are identified from the literature, and equipment technical specifications, which affect the MSE, are also needed to ensure the accuracy of the MSE calculation. Three types of equations are discussed in the following section. The MSE-related variables are presented in Table 1.

Table 1. Multisite efficiency variables.

Reference	Multisite efficiency variables
[8, 18]	Number of test sites
[8, 11]	Single site unit indexing time
[8, 19]	Multisite unit indexing time
[2, 11]	Single site test time
[2, 10]	Multisite test time
[19]	Tray indexing time
[20]	Wafer/strip indexing time
[2, 10]	Equipment utilization
[11, 17, 18]	Testing yield
[11]	Jam rate

The MSE equation identified from previous literature included the International Technology Roadmap for Semiconductors and is expressed as Eq. (1):

$$MSE = 1 - \frac{T_N - T_1}{(N-1)T_1} \quad (1)$$

where the multisite test time (T_N), single site test time (T_1), and number of test sites (N) are considered in the equation. However, the MSE is also influenced by other variables as shown in Table 1. Therefore, the equation should be improved to predict the MSE accurately. The variables that should be included in the MSE are the following as shown in Fig. 4 which is the process flow of the pick and place handler testing as explained below:

i. The input pick arm collects the chips from the input tray and transfers them to the input shuttle.
ii. The test arm takes the chips from the input shuttle and punches them into the test contactor to begin the testing.
iii. The tested chips are replaced with new ones and are then transferred to the output shuttle.
iv. The chips are sorted by the output sorting pick arm into the good tray for the tested good chips and the rejected tray for the tested bad chips.

This process flow shows that the MSE is affected not only by the test time but also by other variables as follows:

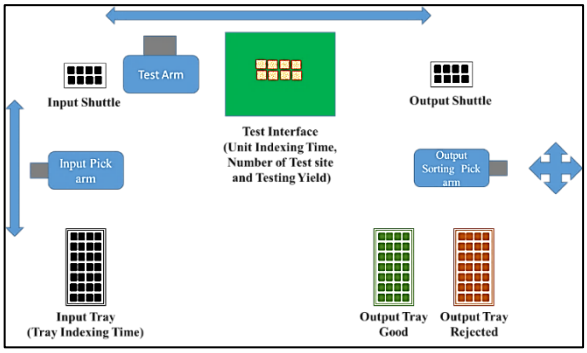

Fig. 4. Flowchart of testing process: pick and place handler.

2.1. Unit indexing time

The unit indexing time is an important variable where the unit indexing time is the time spent to replace the tested chips with the new chips. The multisite unit indexing time and single site unit indexing time need to be part of the equation to compare the multisite and the single site.

2.2. Testing yield

The testing yield is the percentage of tested good chips over the total number of incoming chips. The multisite testing yield is an important variable to determine the MSE to ensure when the test equipment is capable of handling the multiple chips without compromising the positioning accuracy [17]. In addition, the electrical resistance of different test sites affects the testing accuracy, which ultimately contributes to the testing yield [17].

2.3. Jam rate

Jam rate is the variable that measures the stability of the equipment to perform the task. For the multisite testing, understanding how the number of test sites affects the jam rate is important to ensure that the test equipment can handle the parallel testing effectively [11, 20], where instability causes the increment of the jam rate, which then reduces the MSE.

2.4. Tray matrix and tray exchange frequency

The tray matrix determines how many chips are carried by the tray. The higher the tray matrix, the lower the tray exchange frequency. The tray exchange frequency is also affected by the test site increment such that when more chips are tested in parallel, the tray exchange frequency also increases because the chips on a tray are completely tested faster than the lower test site configuration. Therefore, the tray exchange frequency is also an important variable that affects the MSE [12].

Therefore, the MSE equation needs to include all the variables as indicated. A detailed discussion of the MSE equation development is as follows.

As shown in Eq. (1), the *MSE* is calculated by dividing the test time delta between T_{ms} and T_1 over the total testing time for the test site delta between the single site and multisite (N-1). To develop the new MSE equation, which includes the testing yield, unit indexing time, tray exchange time and frequency and jam rate, need to incorporate the delta of testing yield between single site and multisite, the delta of unit indexing time between single site and multisite, the delta of jam rate between the single site and multisite and the delta of tray exchange frequency and time between the single site and multisite into Eq. (1)

The incorporated unit indexing time is shown as follows:

$$MSE = 1 - \frac{(T_N+I_N)-(T_1+I_1)}{(N-1)\ X\ (T_1+I_1)} \quad (2)$$

where I_N is the multisite unit indexing time and I_1 is the single site unit indexing time. Second, to incorporate the jam rate and tray exchange frequency and time, the per-chip time increase affected by the jam rate and tray exchange frequency needs to be derived as follows:

To derive it, first the equation of maximum testing throughput for multisite (MTTMS) and single sites (MTTSS) are derived as Eqs. (3) and (4):

$$MTTMS = \frac{3600\ X\ N}{T_{ms}+I_{ms}} \tag{3}$$

$$MTTSS = \frac{3600}{T_1+I_1} \tag{4}$$

where 3600 is the total second in one hour, T_{ms} is the multisite test time, I_{ms} is the multisite unit indexing time, T_1 is the single site test time, I_1 is the single site unit indexing time, and N is the number of test sites where single site N is equal to 1.

Second, the tray exchange frequency and jam rate need to be derived to calculate the extra time per chip on top of the test time and unit indexing time. The total tray exchange frequency time in one hour (TEH) is shown in Eq. (5):

$$TEH = \left(\frac{\frac{3600\ X\ N}{T_{ms}+I_{ms}}}{Tray\ Matrix}\right) X\ TITime \tag{5}$$

where *N* is the number of test sites (single site *N* is equal to 1), T_{ms} and I_{ms} is the multisite test time and unit indexing time (single site replaced with T_1 and I_1). The tray is a carrier upon which the semiconductor's chip rests. The tray matrix is the layout for carrying several chips on a tray, (see Fig. 5 for an example). TITime is the tray indexing time, which is the time spent by the test handler to replace the empty tray with the new fully loaded tray.

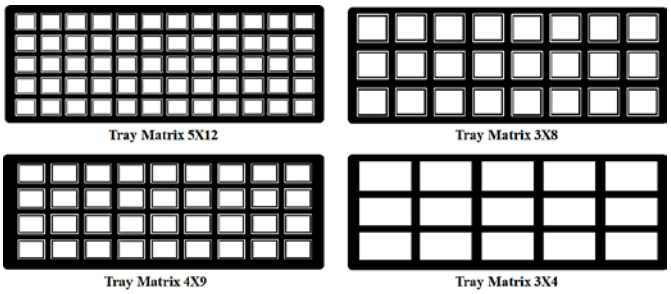

Fig. 5. Tray matrix.

To determine the extra time per chip needed for the tray exchange frequency (UTE_{ms}), Eq. (6) is derived as follows:

$$UTE_{ms} = \frac{\left(\frac{\frac{3600\ X\ N}{T_{ms}+I_{ms}}}{Tray\ Matrix}\right) X\ TITime}{MTTMS} \tag{6}$$

where the total tray exchange frequency time in one hour *(TEH)* is divided by the maximum testing throughput per hour to obtain the extra time per chip, which is affected by the tray exchange frequency. (Note: For the single site, the T_{ms}, I_{ms}, and *MTTMS* are replaced with T_1, I_1, and *MTTSS*.)

Third, the derivation of the jam rate also needs to be obtained, as shown in Eq. (7):

$$MTTRH = AMTTR\ X\ No\ of\ Jam\ per\ hour \tag{7}$$

where *MTTRH* is the mean time to resolve in one hour, *AMTTR* is the average mean time to resolve and is multiplied by the total number of jams in one hour. Similar

to the tray exchange frequency, the extra time spent by a chip with the jam rate is determined as shown in Eq. (8):

$$MTTR_{ms} = \frac{AMTTR\ X\ No\ of\ Jam\ per\ hour}{MTTMS} \quad (8)$$

where *MTTRMS* is the extra time spent by a chip with the jam rate for multisite configuration and is derived by using MTTRH divided by MTTMS. (Note: For the single site, *MTTMS* is replaced with MTTSS.)

Finally, the MSE equation with the variables such as test time, unit indexing time, tray exchange frequency, yield, and jam rate is derived as shown in Eq. (9):

$$MSE = 1 - \frac{\left(\left(\frac{T_{ms}+I_{ms}+UTE_{ms}+MTTR_{ms}}{MS\ Yield}\right)-\left(\frac{T_1+I_1+UTE_{ss}+MTTR_{ss}}{SS\text{-}Yield}\right)\right)}{(N-1)X\left(\frac{T_1+I_1+UTE_{ss}+MTTR_{ss}}{SS\text{-}Yield}\right)} \quad (9)$$

where the processing time delta between the multisite versus single site are compared. The test processing time includes test time (t), unit indexing time (i), tray exchange frequency (UTE), and jam rate (MTTR). The test processing time is divided by testing yield, as shown in Eq. (9). When the testing yield is equal to 100 percent, the testing processing time is optimized. However, when the testing yield is declined, the test processing time for good chips increases because of the decrease in the number of good chips produced.

3. Development of New Testing Throughput Equation

To develop the new testing throughput equation, we need to understand first the relationship between the MSE and testing throughput. The testing throughput equation identified from [6, 9] is shown in Eq. (10):

$$UPH_{ms} = \frac{3600\ X\ N}{T_{ms}+I_{ms}}\ X\ Testing\ Yield \quad (10)$$

where UPH_{ms} is the unit per hour for multisite, N is the number of sites, T_{ms} is the multisite test time, and I_{ms} is the multisite unit indexing time. For the testing throughput to include the tray exchange sequence and jam rate, Eq. (11) is derived:

$$UPH_{ms} = \frac{3600\ X\ N}{T_{ms}+I_{ms}+UTE_{ms}+MTTR_{ms}}\ X\ Testing\ Yield \quad (11)$$

To incorporate the MSE into Eq. (11), first we need to understand the relationship of *MSE* with UPH_{ms}, as shown in Fig. 6. Furthermore, we derive the following as shown in Eq. (12):

$$MSE = 1 - \frac{\left(\left(\frac{T_{ms}+I_{ms}+UTE_{ms}+MTTR_{ms}}{MS\ Yield}\right)-(T_1+I_1+UTE_{ss}+MTTR_{ss})\right)}{(N-1)X(T_1+I_1+UTE_{ss}+MTTR_{ss})}$$

Fig. 6. Relationship between T_{ms} and T_{ms} with *MSE*.

The step-by-step derivation of the *MSE* with *UPH* relationship is shown in Eqs. (12), (13), and (14), where the sum of T_{ms}, *Ims*, UTE_{ms}, and $MTTR_{ms}$ in Eq. (11) is replaced with the *MSE* relation as shown in (13), which is then derived as Eq. (14). The testing yield in Eq. (14) is cancelled and the final UPH_{ms} equation is derived in Eq. (15):

$$\frac{\left(\left(\frac{T_{ms}+T_{ms}+UTE_{ms}+MTTR_{ms}}{MS\ Yield}\right)-(T_1+I_1+UTE_{ss}+MTTR_{ss})\right)}{(N-1)X(T_1+I_1+UTE_{ss}+MTTR_{ss})} = 1 - MSE, \quad (12)$$

$$T_{ms} + I_{ms} + UTE_{ms} + MTTR_{ms} = (1 - MSE)X(N-1)X(T_1 + I_1 + UTE_{ss} + MTTR_{ss}) + (T_1 + I_1 + UTE_{ss} + MTTR_{ss})\ X\ MSYield, \quad (13)$$

$$UPH_{ms} = \frac{3600\ X\ N}{(1-MSE)X(N-1)X(T_1+I_1+UTE_{SS}+MTTR_{SS})+(T_1+I_1+UTE_{SS}+MTTR_{SS})\sout{X\ MS\ Yield}} \times \sout{Testing\ Yield} \quad (14)$$

$$UPH_{ms} = \frac{3600\ X\ N}{(1-MSE)X(N-1)X(T_1+I_1+UTE_{SS}+MTTR_{SS})+(T_1+I_1+UTE_{SS}+MTTR_{SS})} \quad (15)$$

Lastly, the cost of test equation to be derived through the economic average cost theory is shown in Eq. (16) [9]:

$$Average\ Cost\ = \frac{Total\ Cost}{Output} \quad (16)$$

The total cost identified from [8, 18] is shown in Eq. (17):

$$Total\ Cost_{Month} = Dep + DL + OH \quad (17)$$

where *Dep* is equipment depreciation cost; *DL* is direct labor cost; *OH* is overhead cost, which includes indirect labor, facility, floor space, maintenance, and test interface costs [8]. The total cost per utility hour is derived as Eq. (18):

$$Total\ Cost_{hour} = \frac{Dep+DL+OH}{729.6\ X\ U} \quad (18)$$

where 729.6 is the hour per month and *U* is the equipment utilization percentage. The total cost per hour, which considers the production capacity, is derived in Eq. (19):

$$Total\ Cost_{hourC} = \left(\frac{Dep+DL+OH}{729.6\ X\ AU}\right)\ X\ NOTE \quad (19)$$

where *AU* is the actual utility percentage based on the required production capacity derived in Eq. (20):

$$AU = \frac{U}{NOTE} \quad (20)$$

where *U* is the utilization percentage and NOTE is the number of test equipment based on the production capacity. The *U* is derived in Eq. (21):

$$U = \frac{Production\ Capacity}{MTTMS} \quad (21)$$

where the production capacity is divided by MTTMS, which is the maximum throughput that can be produced by the test equipment, as derived in Eq. (3). When the production capacity is equal to MTTMS, the test equipment is 100 percent utilized. When the production capacity is greater than the MTTMS, additional test equipment is required where the NOTE is equal to two. Furthermore, when the AU is over 200 percent utilized, the NOTE is equal to three, and so on.

$$Cost\ of\ Test = \frac{\left(\frac{Dep+DL+OH}{729.6\ X\ AU}\right)}{\left(\frac{3600\ X\ N}{(1-MSE)X(N-1)X(T_1+I_1+UTE_{SS}+MTTR_{SS})+(T_1+I_1+UTE_{SS}+MTTR_{SS})}\right)}\ X\ NOTE \quad (22)$$

The cost of test equation, which considers *MSE* and *AU*, is derived from the average cost in Eq. (16) as shown in Eq. (22).

Furthermore, the *Dep* is the Equipment depreciation cost derived as Eq. (23) [8, 21]:

$$Dep = \frac{C_{tester}+C_{handler}}{N_{cycle}X12} \quad (23)$$

where C_{tester} is the cost of tester, $C_{handler}$ is the cost of handler, and N_{cycle} is the test handler and tester life cycle (typically using five years as the standard).

DL is the direct labor cost, which consists of the operator's and technician's wages as shown in Eq. (24) [21].

$$DL = (W_{oper} + W_{tech})X3 \quad (24)$$

where W_{oper} is the monthly wage of the operator and W_{tech} is the monthly wage of the technician. The total wages are multiplied by three due to three rotation shifts per day. The technician wages can be further derived as Eq. (25) because the technician does not work full-time on a particular test equipment [21].

$$W_{tech} = \frac{G_{annual}}{12} X \frac{H_{participate}}{8}, \quad (25)$$

where G_{annual} is the gross annual salary, $H_{participate}$ represents the hours a technician participates in equipment troubleshooting per shift (eight hours). The $H_{participate}$ is equal to *MTTR*, which means that the stability of the test equipment affects the W_{tech} because the cost increases if a technician needs to spend additional time to recover the equipment. Thus, a firm needs to increase the technician headcount, which will affect the overall operation cost.

Lastly, *OH* variables are discuss as follow:

3.1. Facility costs

The facility costs denote the utility costs of the test equipment and compressed air as derived in Eq. (26) [12].

$$Utility = P_{rating} X\ 730\ X\ E_{rate} + CDA_{cost} \quad (26)$$

where P_{rating} is the total power rating of the tester and test handler in kilowatts, E_{rate} is the electricity rate per kWh, and CDA_{cost} is the compressed air cost consumed by the test handler.

3.2. Management cost

The management cost (*MGC*) is the monthly wage for indirect labor, including that of the manager, engineer, and supervisor [8, 21]. The monthly MGC is calculated as shown in Eq. (27):

$$MGC = W_{Mgr.} + W_{sup.} + W_{Engr.}, \quad (27)$$

where $W_{Mgr.}$ is the wage for the manager, $W_{sup.}$ is the wage for the production supervisor, and $W_{Engr.}$ is the wage for the engineer.

3.3. Floor space cost (FSC)

Floor space cost is the food print, or the area cost occupied by the test equipment. The bigger the test equipment is, the higher the FSC. The FSC is derived by Eq. (28) [8]:

$$FSC = Price\ per\ sq.ft.\ X\ TEFP \quad (28)$$

where the FSC is calculated by multiplying the price per sq. ft. with the test equipment footprint.

3.4. Maintenance cost

Maintenance cost (*MC*) is the cost spent in one month to maintain the test equipment, such as wear-and-tear part replacement, consumable part cost, electrical cost, and mechanical hard down repair cost [8]. The maintenance cost is expressed by Eq. (29) [21].

$$MC = Dep\ X\ D\%, \quad (29)$$

where the MC is calculated by multiplying the Dep with the downtime percentage (D%) to obtain the annual MC. The monthly MC is further divided into twelve months. The hourly MC is ascertained by dividing the monthly counterpart by 729.6, which is the total hours in a month.

3.5. Test interface cost

The test interface cost includes the test contactor and load board costs for the final testing. Conversely, the interface cost for the wafer test prober involves the probe card cost. The test interface cost is determined by a multisite configuration for which a higher test site entails higher cost [8]. This situation arises because increasing the test sites will also increase the number of test contactors. The load board fabrication cost will also rise because of the complex printed circuit board design and the number of electronics components involved.

4. Conclusion

The MSE equation, which considers all the relevant variables, namely, test time, unit indexing time, tray exchange frequency time, jam rate, and testing yield, has been developed. In addition, the relationship of MSE with the testing throughput is also derived, which is integrated into the cost of test equation. This equation considers the actual equipment utilization based on the required production capacity and NOTE so that the cost of test can be calculated when the production capacity changes. This approach is important for the firm to estimate the accurate cost of test according to the production capacity instead of simply calculating the MSE, testing throughput, and cost of test based only on the test time, which aims to reflect the actual situation. This study contributes to the body of knowledge in MSE, testing throughput, and cost of test for semiconductor test manufacturing firms and is expected to be a useful guideline in the equipment selection process and ultimately in profit and loss management.

5. Future Research

In the future, researchers can validate the equations by comparing the predicted value versus the actual testing throughput to determine the Robust Quality Index (RQI) so that the accuracy of the predictions can be ensured. ROI determines the robustness of data and process quality; the higher RQI is, the better the situation is [22] and the different between the predicted value versus the actual value must be less than 30% to confirmed condition is highly reproducible [23]. In addition, the equation can be used to optimize the multisite testing throughput with Taguchi Robust Parameter design which is an engineering optimization strategy ideally used for the development of new technologies in product and process design [24].

Finally, the method to calculate the maintenance cost based on the equipment mean time to failure can be further derived into the equation for the long-term determination of multisite technology return on investment.

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