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# Design of a DC-DC Converter in Residential Solar Photovoltaic System

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**Abstract.** This study looks at buck type switch mode power supplies (SMPS) suitability in residential solar photovoltaic (PV) applications, of which several factors affecting the desired output response are identified. The main objective of the study is to design robust converter controller, capable of maintaining constant output, with emphasis on good efficiency, stability and low output voltage ripple. One way of achieving this is by using the voltage mode control (VMC) technique. The main tool used for the converter analysis is the LT SPICE software. Converter performance is investigated without and with the developed control technique. Results obtained reveals satisfactory performance of voltage mode control (VMC).

## 1. Introduction

Solar photovoltaic (PV) is currently one of the fastest growing renewable energy technologies and has been installed in more than 80 countries around the world [1]. Continuous cost reduction and government incentives are helping to make this technology more widely installed [2], although in many parts of the world, e.g. the developing countries, this cost is still viewed as expensive. In comparison to other renewable sources, solar PV offers relatively low cost and maintenance.

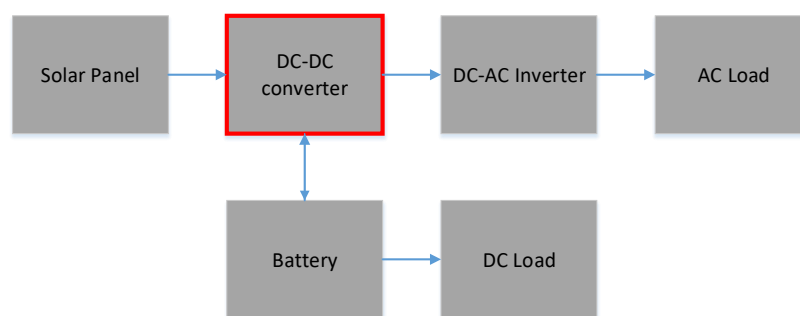
On global scale, PV accounts for a very small amount of energy production. Currently installed capacity is about 1% of the total renewable energy installed [1]. Solar PV systems tend to be more expensive when compared with conventional sources, however, they have no fuel cost [3]. Easy availability, relatively quick energy payback and grid independence are some of the main reasons driving PV evolution [4]. Currently, the efficiency of installed solar panels is considered moderate. To maximize the solar energy capture, investigation of PV system's energy conversion devices is needed. One of such key component is the DC-DC converter. To ensure maximum energy capture, strict requirements such as high efficiency and low output voltage ripple are placed at converter design stage. Such specification requires careful design and investigation.

The main objective of this project is to investigate DC-DC converter in residential solar home applications. The converter designed in this work will form part of a residential solar PV system. The emphasis is on efficient, low output voltage ripple and stable operation.



## 2. DC-DC Converter

In the past, conversion of fixed DC voltage to variable was inefficient and expensive. This was due to the use of linear voltage regulators. Such voltage regulation was achieved by dissipating power in the pass transistor. As a result, devices suffered from high power dissipation especially with big difference between input and output voltage levels. This meant increased size of the device due to the heatsink requirement to dissipate the heat of the pass transistor [5]. With introduction of power semiconductors and integrated circuits, it opened the door for new type of power electronic devices. Switch mode power supply (SMPS) such as DC-DC converter is of great importance in present day power electronics [6]. Typical applications are personal computers power supplies, office and telecommunication equipment, appliance control, automotive industry, aircrafts, etc. They are also one of the crucial components in any solar PV system, as shown in Figure 1.



**Figure 1.** Off-grid solar PV system block diagram.

SMPS achieves voltage conversion at desired levels by high frequency switching action, varying switch on to off time (duty cycle). This conversion is performed by temporarily storing energy in the form of magnetic and electric fields and then releasing it to the output at different voltage level. Such process involves the use of inductors and capacitors. Losses are minimised in this way and are not dependent on load variations. High frequency operation in these devices allows the use of small lightweight and cheaper components. Greater energy conversion efficiency is achieved as the switching device dissipates little power in on and off states. The efficiency is essential for battery operated PV systems in order to prolong the battery running life. Voltage from PV array varies with the change in insolation, temperature conditions or shading. Converter is expected to deliver efficient and stable performance when subjected to changes in input and output. Reduced physical size and ability to obtain higher output voltage than the input are some of the advantages [7]. These achievements however come with associated drawbacks. The circuit design is more complex due to greater amount of components needed. Output ripple voltage occurring at switching frequency is also a design concern. High voltage ripple can negatively impact the amount of power produced by the PV module. Switching action results in high amplitude, high frequency energy which needs to be filtered to avoid electromagnetic interference (EMI).

Converter operation mode is determined by continuity of inductor current within switching cycle. These are continuous conduction mode (CCM) and discontinuous conduction mode (DCM) [16]. If inductor current does not fall below zero when the switch is on, device is in CCM, and if the inductor current falling to zero before the switch turns on again results in DCM [8]. The CCM permits efficient use of semiconductor switches and passive components improving overall converter efficiency. The DCM requires a special control since the dynamic order of the converter is reduced. Thus, it is required to find out the minimum value of the inductor to maintain the CCM [9]. Converters can be of isolated or non-isolated type. Isolated type benefits from electrical isolation as the transformer is added to the circuit. However, they are not widely used in solar applications due to the added weight and size. Depending on the application converters are classified as buck, boost and buck-boost. All other topologies are either buck or boost derived [10]. To choose suitable converter topology, a comparison between three main topologies mentioned earlier was made. This can be seen in Table 1.

**Table 1.** SMPS topology comparison.

Topology	Advantages	Disadvantages	Efficiency	Power range
Buck	-Due to discontinuous input current, smoothing capacitor is needed. -Simplest design of all SMPS.	-High output ripple. Large output filter needed. -Protection circuit needed in case of short circuit across diode path.	90%	1000 W
Boost	Due to continuous input current small filter is needed.	Large inductor and output filter. Difficult to compensate.	80%	0-150 W
Buck-boost	Ability to self-regulate.	High peak current flow via transistor. Difficult to compensate.	80%	0-150 W

Based on Table 1, it is concluded that the design of the buck converter is simpler than others. It also delivers high efficiency and has a wide output power range which allows greater design flexibility. For those reasons buck type converter is chosen in further studies.

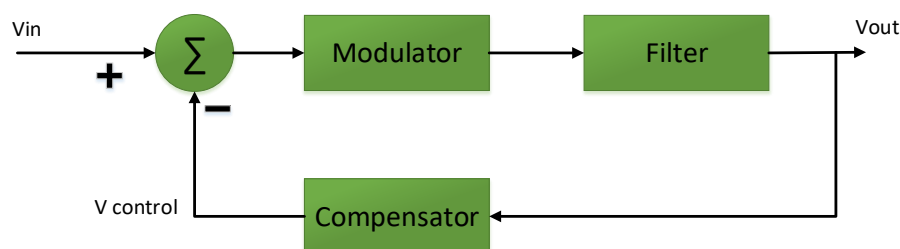
A study of a system that uses open loop buck converter SMPS was carried out in [11]. From the simulations, the existence of high output voltage ripple was noticed in the system. Addition of parallel smoothing capacitor with low ESR seemed so be an effective solution to problem. This outlines the importance of output capacitance in converter design, although such control measure will have the effect of slight reduction in efficiency. The reduction will become greater at light loads [12].

Transient response analysis clearly demonstrated converter response to any input and output changes. With variation of load resistance, changes in load demand were simulated. Changing the supply voltage helped to represent changes in solar energy production described in the literature. As a result of these tests, slow device response to input and output changes is observed. It is apparent that device was not able to respond to input and output changes. It is therefore concluded that this simple buck converter is not suitable solution for solar PV application. Some means of converter control is needed, which is addressed in the next sections.

### 3. Voltage Mode Control

#### Design

This section focuses on providing solution to problems associated with open loop SMPS. This is achieved by performing converter control stage design. One of the methods is voltage mode control (VMC). Figure 2 illustrates the concept of buck converter control consisting of three main blocks. The forward path is formed by the pulse width modulator and the output filter with load resistance. This is usually called a plant. The loop is closed by providing comparison between output and reference voltages to maintain desired output.

**Figure 2.** Buck converter control block diagram.

More in depth understanding can be achieved by analysing Figure 3. Converter output voltage,  $V_o$ , is monitored and scaled by potential divider network consisting of resistors  $R1$  and  $R2$ . It is then fed to differential error amplifier and compared with a reference voltage,  $V_{ref}$ . The result is control voltage,  $V_c$ , which is the input to comparator. Comparison between constant saw tooth ramp voltage and  $V_c$ , seen in Figure 4 produces corresponding duty cycle,  $D$ . PWM driver circuit then controls the main switch. Thus the output voltage is constantly monitored to adjust the duty cycle of converter [13].

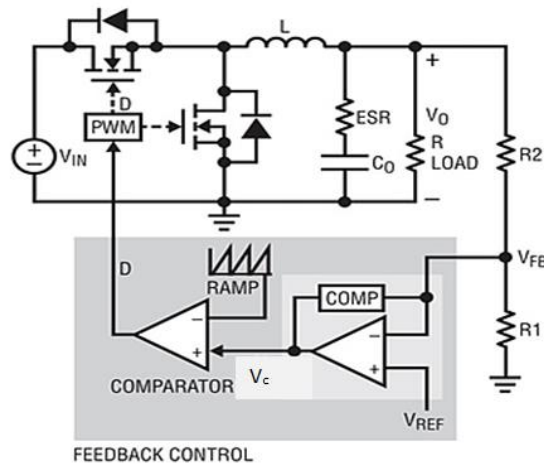


Figure 3. Voltage mode controlled buck converter [14].

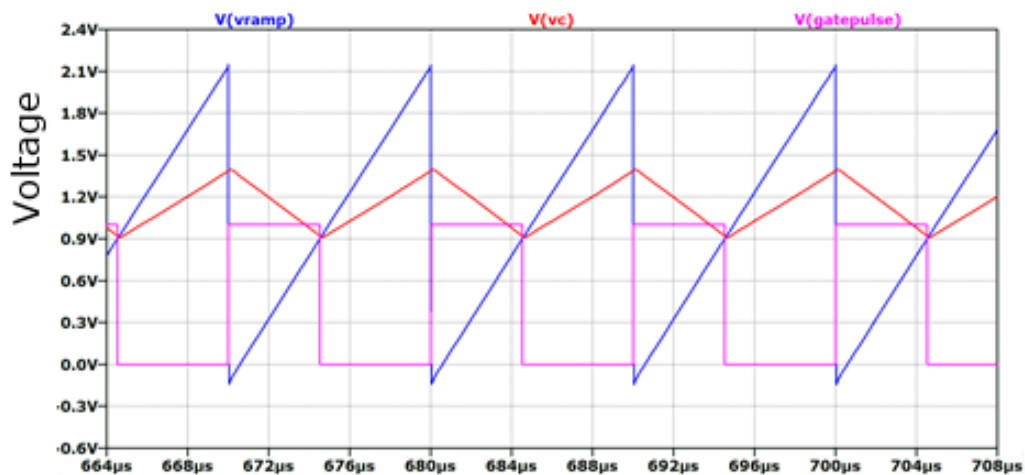


Figure 4. PWM in voltage mode control.

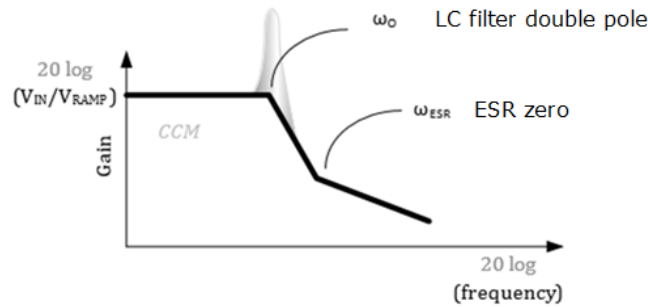
The LC network in Figure 4 forms a low pass filter. The cut off frequency is equal to  $f_o$ . This allows DC content but blocks  $f_{sw}$  and its harmonics. The cut off frequency is given as:

$$\omega_o = f_o = \frac{1}{2\pi\sqrt{LC}} \quad (1)$$

Buck converter plant can be expressed by transfer function in Laplace domain as:

$$G_{vd}(s) = \frac{V_{in}}{V_{ramp}} \times \frac{1 + \frac{s}{\omega_{ESR}}}{1 + \frac{s}{Q_o\omega_o} + \frac{s^2}{\omega_o^2}} = \frac{V_{in}}{V_{ramp}} \times \frac{1 + \frac{s}{\omega_{ESR}}}{1 + \frac{s^2}{\omega_o^2}} \quad (2)$$

The existence of complex double pole due to the LC output filter and a left half plane zero due to the output capacitor ESR can be seen. Location of poles and zeros can be depicted in Figure 5.



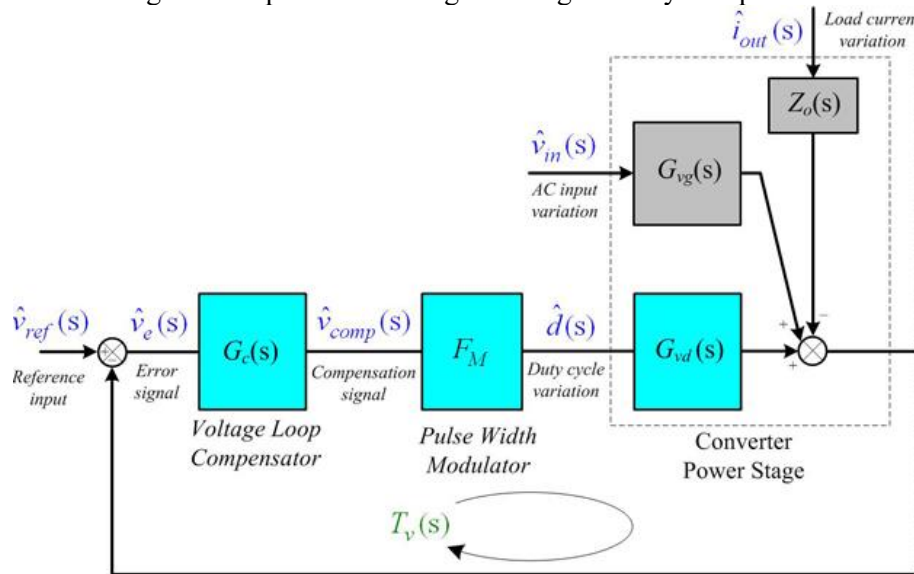
**Figure 5.** Buck converter power plant [13].

Using information about the plant compensator design can be proceeded. Desired open loop gain response should ideally be a straight line. The aim is to cancel poles and zeros or move them to the higher frequency. Location of these can be found by using the following equations:

$$f_o = \frac{\omega_o}{2\pi} = \frac{1}{2\pi \sqrt{L_o C_{out} \left[ \frac{1 + (R_{ESR}/R_L)}{1 + (R_{DAMP}/R_L)} \right]}} = \frac{1}{2\pi \sqrt{L_o C_o}} \quad (3)$$

$$f_{ESR} = \frac{\omega_{ESR}}{2\pi} = \frac{1}{2\pi R_{ESR} C_o} \quad (4)$$

where  $f_o$  is the frequency of the double pole of LC network,  $f_{ESR}$  is the Frequency of the ESR zero,  $R_L$  is the effective load resistance, and  $R_{DAMP}$  is the total series damping resistance not shown in Figure 3. The compensator circuit design can be performed using small signal analysis represented in Figure 6.



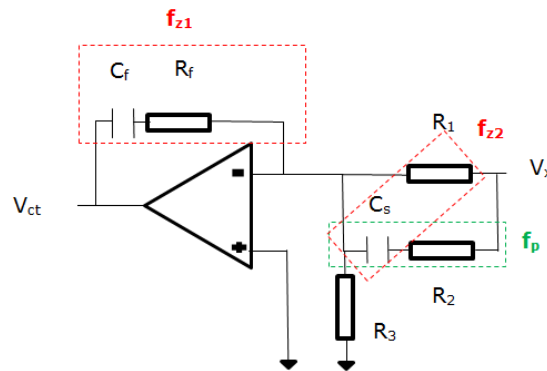
$$\hat{v}_{out}(s) = G_{vd}(s) \hat{d}(s) + G_{vg}(s) \hat{v}_{in}(s) - Z_o(s) \hat{i}_{out}$$

**Figure 6.** Block diagram representation of buck converter model [15].

The modulator gain  $F_m$  depends on the change in control voltage and duty ratio given as:

$$F_m = \frac{D}{V_{ct}} = \frac{1}{V_{ramp}} \quad (5)$$

There are three main types of error amplifiers used for SMPS compensation. These are discussed in [13]. In this case only two zeroes and a pole are needed for compensation, as illustrated in Figure 7. From Figure 7, error amplifier circuit components can be divided into zeros  $Z_f$  and poles  $Z_s$ . The output transfer function is defined as:



**Figure 7.** Error amplifier with compensation.

$$\frac{V_{ct}}{V_x} = \frac{Z_f}{Z_s} = \frac{sC_s(R_1 + R_2 + 1)}{sC_f R_1} \times \frac{sC_f(R_f + 1)}{sC_s R_2 + 1} \quad (6)$$

Loop gain now becomes

$$T = \frac{V_s}{V_m} = \frac{sC(R_{ESR} + 1)}{\left(\frac{s}{\omega_o}\right)^2 + \frac{1}{Q} \frac{s}{\omega_o} + 1} \left( \frac{sC_s(R_1 + R_2 + 1)}{sC_f R_1} \left( \frac{sC_f R_f + 1}{sC_s R_2 + 1} \right) \right) \quad (7)$$

where  $V_m$  is the ramp voltage.

Now setting the poles of Equation 7 to equal to zeros and vice versa leaves us with

$$T = \frac{V_s}{V_m} \frac{1}{sC_f R_1} = \frac{k}{s} \quad (8)$$

$$\text{where } k = \frac{V_s}{V_m} \frac{1}{C_f R_1} \quad (9)$$

The unity gain frequency at which 0 decibel line is crossed is expressed as  $f_u = f_s/10$ . Division factor is chosen so that the compensator bandwidth would be reasonably lower than  $f_s$ . This prevents PWM ripple from affecting the compensator. By setting the integrator operational amplifier at this cross over frequency, the loop gain becomes  $T = 1$ . Now, in Equation 8, let  $s = 2\pi f_u$ . Then we have  $T = 1$  and now it can be solved for  $C_f$  as follows.



$$C_f = \frac{V_s}{V_m} \frac{1}{2\pi f_u R_1} \quad (10)$$

The rest of the amplifier component values are given by [11]:

$$f_{z1} = \frac{1}{2\pi C_f R_f} \quad (11)$$

$$R_f = \frac{1}{2\pi f_{z1} C_f} \quad (12)$$

$$f_{z2} = \frac{1}{2\pi C_s R_1} \quad (13)$$

$$C_s = \frac{1}{2\pi f_{z2} R_1} \quad (14)$$

The pole to cancel ESR zero is

$$f_p = \frac{1}{2\pi C_s R_2} \quad (15)$$

$$R_2 = \frac{1}{2\pi f_p C_s} \quad (16)$$

With reference voltage provided in [16], the output voltage depends on ratio of two feedback resistors in potential divider network.

$$V_o = \left(1 + \frac{R_1}{R_3}\right) V_{ref} \quad (17)$$

Applying these equations, the compensator component values are listed in Table 2.

**Table 2.** VMC Error amplifier component values.

Component	Value
R1	85.0 kΩ
R2	56.2 kΩ
R3	10.0 kΩ
R <sub>f</sub>	95.3 kΩ
C <sub>f</sub>	3.0 nF
C <sub>s</sub>	3.0 nF

### Simulation model and results

The voltage mode converter model shown in Figure 8 was designed with calculated compensator values. Converter power and control stages are indicated by green and yellow dotted lines respectively. Constant voltage ramp to the PWM comparator was generated by internal clock along with current mirror circuit. The clock forms part of gate driver. It determined the moment when switch turns on in every cycle. The feedback loop determines the moment at which the switch turns off in every cycle. This ensures constant converter switching frequency. Figure 9 reveals transient output voltage response.

The output response was critically damped. A parallel capacitance branch was added to converter LC filter. This was necessary to reduce the quality factor to 0.596. This time system exhibited a critically damped response with no overshoot (see Table 3). Smoothing capacitor used in open loop simulation was not needed in this case. However, the ESR value of the output capacitor was changed to bring satisfying performance.



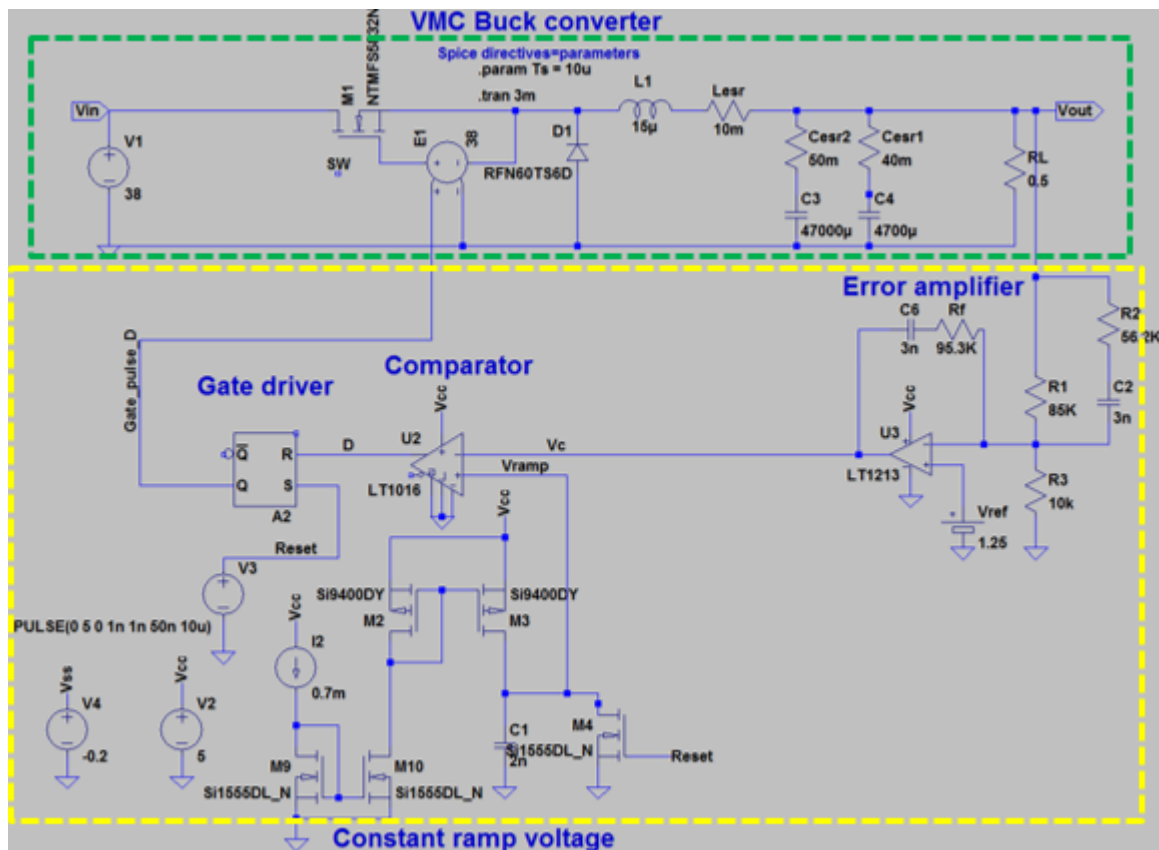


Figure 8. LT spice model of VMC buck converter.

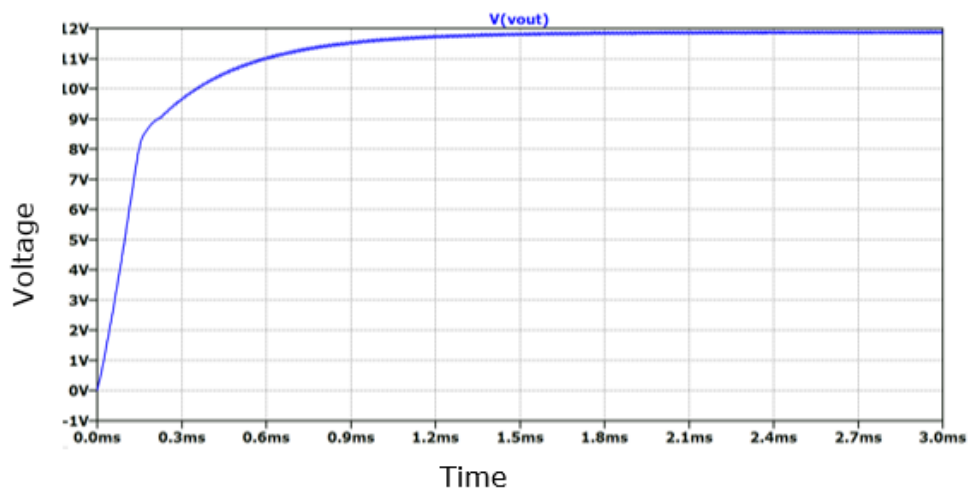


Figure 9. Transient response of closed loop VMC buck converter.

Using this control method, the output was maintained at constant value despite variations in load. Comparing Tables 3 with the initial analysis of open loop buck converter SMPS in [11], the voltage ripple has dropped from 80 to 56 mV. Settling time was constant for all values of load resistance. Furthermore a decrease of 2.5 s in settling time was evident. For loads above 3 Ω, it is reduced by half. The settling time is slightly greater than in [17].

**Table 3.** VMC buck converter response to load variation, when  $V_{in}$  was kept at 38 V.

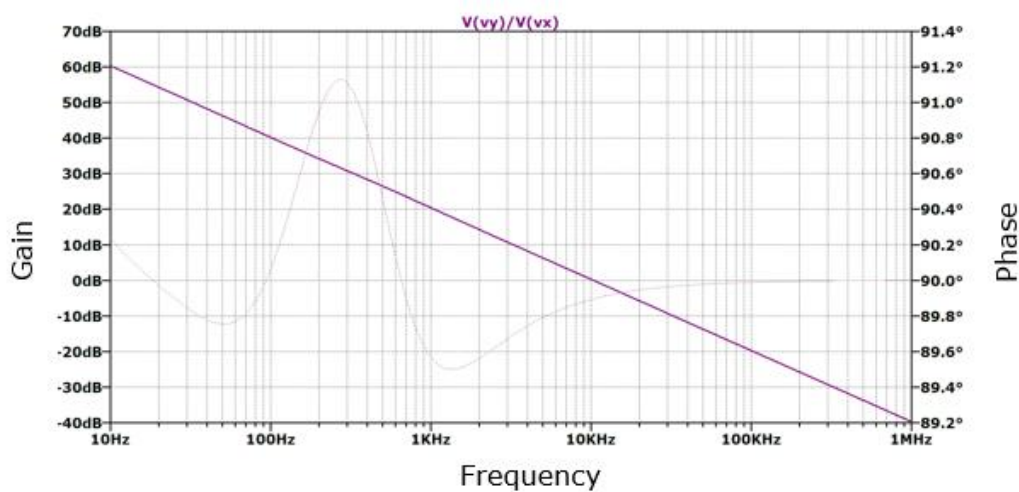
$R_{Load}$ ( $\Omega$ )	Overshoot (%)	$T_{sett}$ (ms)	$V_{ripple}$ (mV)	$V_{Out}$ (V)
0.5	0	1.5	56	12
1	0	1.5	56	12
3	0	1.5	56	12
5	0	1.5	56	12
6	0	1.5	56	12
8	0	1.5	56	12
20	0	1.5	56	12
100	0	1.5	56	12

Looking at Table 4, converter showed ability to adapt to input voltage changes. It was true for any input voltage above 10 V. This was achieved with greater output voltage ripple. Output ripple also increased in greater increments than in previous results. For voltages above 30 V, ripple was almost the same in both cases. Surprisingly no ripple exist at input of 10 V. The settling time has reduced by 0.6 s. Percentage overshoot was completely eliminated for input voltages above 10 V.

**Table 4.** VMC buck converter response to the input change.

$V_{in}$	$R_{Load}$ ( $\Omega$ )	Overshoot (%)	$T_{sett}$ (ms)	$V_{ripple}$ (mV)	$V_{out}$ (V)
10	1	120	2.4	0	9.0
15	1	0	2.4	25	11.8
20	1	0	2.4	63	11.8
25	1	0	2.4	90	11.9
30	1	0	2.4	110	11.9
35	1	0	2.4	120	11.9

The initial stability response was not as expected. This was rectified by introducing another capacitor in parallel. The value chosen was ten times of the original. Figure 10 presents result of the system stability in form of bode plot. Variation of phase and gain with respect to frequency is shown.

**Figure 10.** VMC loop gain bode plot indicating stability.

The gain rolled off as expected for this type of compensation. The crossover frequency occurred at expected frequency of 10 kHz. Response shared some similarities as the results presented in [18]. Device has a good phase margin of  $89^\circ$ . The gain margin was infinite as the phase never reaches  $0^\circ$ .

It was known earlier that converter was not able to respond to input and output changes. It was demonstrated that the VMC control can eliminate this problem. By monitoring output voltage and comparing it with desired reference value, constant output voltage was maintained. This was valid for changes at both, the input and output side. Stable operation was ensured by modified type 3 compensator circuit.

Transient response analysis revealed converter to have a critically damped response with no overshoot. Such feature is desirable for maximum power extraction from PV module. Great reduction in output voltage ripple observed proved this statement. The transient response time also seems to follow same trend demonstrating great reduction. Reduction of voltage ripple in VMC was accomplished without the need for additional smoothing capacitor.

Compensation circuit design was assessed by bode plot analysis indicating the main parameters describing system stability. Some modifications to initial design were needed to reduce the Q factor of the circuit and produce wanted stability response. The use of output filter capacitor has emerged as effective solution to mitigate this issue. Variation of capacitance values proves to have direct effect on transient response and stability. With VMC a good phase margin of  $89^\circ$  and infinite gain were achieved.

Converter demonstrated ability to respond to input and output changes. Constant output voltage for input and load variations was maintained. Use of VMC allows converter to be used for applications in solar PV systems. Nevertheless, this developed model still has relatively slow transient response. This encourages to seek alternative control solutions, discussed in the next section.

#### **4. Conclusions**

This work investigated non isolated buck converter topology. Converter analysis was performed using LT SPICE software. The emphasis of investigation was on efficiency, low output voltage ripple and stability required for applications in residential solar PV system. Study was performed with buck converter topology due to its simplicity among other topologies and relatively good performance.

Based on an earlier study on uncontrolled converter model [11], it was found that the open loop buck converter SMPS has high efficiency. Software simulations performed allows to gather important data about converter behaviour. Output voltage ripple has emerged as the main issue. The importance of output capacitance in ripple reduction became apparent. Although it has to be noted that use of additional capacitance will cause slight reduction in efficiency. Converter behaviour was analysed by transient response analysis. The observed underdamped response did not contribute towards desired performance. Test results revealed that converter was not able to respond to variations in input and output. Furthermore design suffered from slow transient response time. Thus converter was deemed as not suitable for solar PV applications.

This paper presented VMC as a solution. Converter was tested using same methods as in [11]. The transient response was critically damped and had no overshoot. This was a desired feature for maximum power extraction from PV module. Reduction in output voltage ripple was evident. Such improvement was accomplished without the need for additional capacitor. Control technique also demonstrated reduction in settling time. Evaluation of compensator circuit design by bode plot analysis indicated the main system stability parameters. Furthermore the investigation again proved the important role of capacitance in circuit design. It demonstrated to be effective measure in quality factor reduction allowing to produce wanted stability and transient response. Device showed ability to respond to input and output changes. Constant output voltage was maintained for variations in input and output. Design results indicated achievement of good phase and gain margins. Converter was confirmed to be suitable for solar PV applications. Nevertheless developed model still had relatively slow transient response.

#### **Acknowledgments**

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