

Characteristic evaluation of 20-bit consecutive codes in high performance optical burst mode receiver configuration

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ABSTRACT

Optical burst mode receivers are indispensable components for Passive Optical Network (PON) and Ethernet Optical Access Network (E-OSAN). An optical burst mode receiver with transfer function $G_n(j\omega/\omega_0) = 1 - H_n(j\omega/\omega_0)$ is proposed, of which better performance is anticipated than that of conventional AC-coupling. Next, an optical burst mode receiver with fast response $G_n(j\omega/\omega_F)$ and slow response $G_n(j\omega/\omega_S)$, whereby $G_n(j\omega/\omega_F)$ switches to $G_n(j\omega/\omega_S)$ right after the DC component of the input burst signal converges to 0 is proposed. Then, an automatically switching circuit that switches fast response $G_n(j\omega/\omega_F)$ to slow response $G_n(j\omega/\omega_S)$ circuits right after the maximum peak value of the output burst $G_n(j\omega/\omega_F)$ is 1/2 and the DC components of the input burst converges to 0 is also proposed. This paper presents the experiments on same consecutive codes in burst mode receivers using the proposed automatically switching circuit, with evaluation on its characteristics made through simulation.

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1. INTRODUCTION

Optical burst mode receivers are essential for Optical Line Terminals (OLTs) in Time Division Multiplexing based Passive Optical Networks (TDM-PONs) [1-5]. Optical burst mode receivers [6-8] are also crucial components for both Optical Network Units (ONUs) and OLTs in Ethernet Optical Switched Access Networks (E-OSANs) [9].

Previously, Nomura et al. developed a prototype E-OSAN system. They contrived optical burst mode receivers with AC-coupling using commercial components [10-12]. In improving the performance of the AC-coupling receivers, Ueda et al. engineered an optical burst mode receiver with transfer function $G_n(j\omega/\omega_0) = 1 - H_n(j\omega/\omega_0)$, where $H_n(j\omega/\omega_0)$ denotes the transfer function of a Bessel filter with degree n . This proposal generalizes the AC-coupling to $n = 1$ [13-15]. Afterwards, they proposed a design method transfer function $G_n(j\omega/\omega_0)$ and evaluated the optical burst mode receiver that employ the designed transfer function $G_n(j\omega/\omega_0)$. They also introduced a method for realizing LCR circuits from the designed transfer function $G_n(j\omega/\omega_0)$ [16-19].

Based on [5, 6], a stable optical burst mode receiver with shorter clock recovery time is proposed. The proposed configuration uses a fast response transfer function $G_n(j\omega/\omega_F)$ to eliminate DC components rapidly from the input burst, which is then replaced by a slow response transfer function $G_n(j\omega/\omega_S)$

immediately after the DC component of the input burst signal converges to 0. This proposed configuration manually switches the fast response transfer function $G_n(j\omega/\omega_F)$ to a slow response transfer function $G_n(j\omega/\omega_S)$ at selected switching time [20].

Based on [21], a method for automatically switching between fast response circuit $G_n(j\omega/\omega_F)$ and slow response circuit $G_n(j\omega/\omega_S)$ is proposed. The proposed method automatically switches the fast response circuit $G_n(j\omega/\omega_F)$ to a slow response circuit $G_n(j\omega/\omega_S)$ right after the maximum peak value of the output burst of $G_n(j\omega/\omega_F)$ is $1/2$, and the DC components of the input burst converges to 0. The slow response circuit $G_n(j\omega/\omega_S)$ then automatically re-switches to a fast response circuit $G_n(j\omega/\omega_F)$ when the burst signal ends [22]. The performance of the proposed configuration in [23] with 10-bit consecutive code placed at selected times is then evaluated and showed that the fast response circuit $G_n(j\omega/\omega_F)$ automatically switches to slow response circuit $G_n(j\omega/\omega_S)$ right after the maximum peak value of output burst of $G_n(j\omega/\omega_F)$ is $1/2$, i.e. uninfluenced by the 10-bit consecutive codes [24-25]. This paper presents the performance evaluation of a 20-bit consecutive code in the automatically switching fast response $G_n(j\omega/\omega_F)$ and slow response $G_n(j\omega/\omega_S)$ circuits.

2. RESEARCH METHOD

This paper presents the performance evaluation on 20-bit consecutive 0 and 1 code in burst mode receiver. Using an automatic switch between fast response $G_n(j\omega/\omega_F)$ and slow response $G_n(j\omega/\omega_S)$ circuits, 20 bits of the same consecutive 0 and 1 code will be placed at the vicinity of switching mechanism at time, $t_u = 2, 4, 6, 8, 10$ ns of the input burst signals.

Previously, 10 bits of the same consecutive 0 and 1 code is placed at the vicinity of switching mechanism occurring at time, $t_u = 2, 4, 6, 8, 10$ ns of the input burst signal using the same automatic switching between the two circuits.

The automatic switching LCR circuit switches the fast response circuit $G_n(j\omega/\omega_F)$ to slow response circuit $G_n(j\omega/\omega_S)$ right after the maximum peak value of the output burst of $G_n(j\omega/\omega_F)$ reaches $1/2$, and the DC components of input burst converges to 0. The slow response circuit $G_n(j\omega/\omega_S)$ then automatically re-switches to the fast response circuit $G_n(j\omega/\omega_F)$ when the burst signal ends [7].

Function block of the automatic switch between fast response $G_n(j\omega/\omega_F)$ and slow response $G_n(j\omega/\omega_S)$ circuits are shown in Figure 1 while Figure 2 (a) ~ (h) shows the signal waveforms for each (a) ~ (h) in Figure 1.

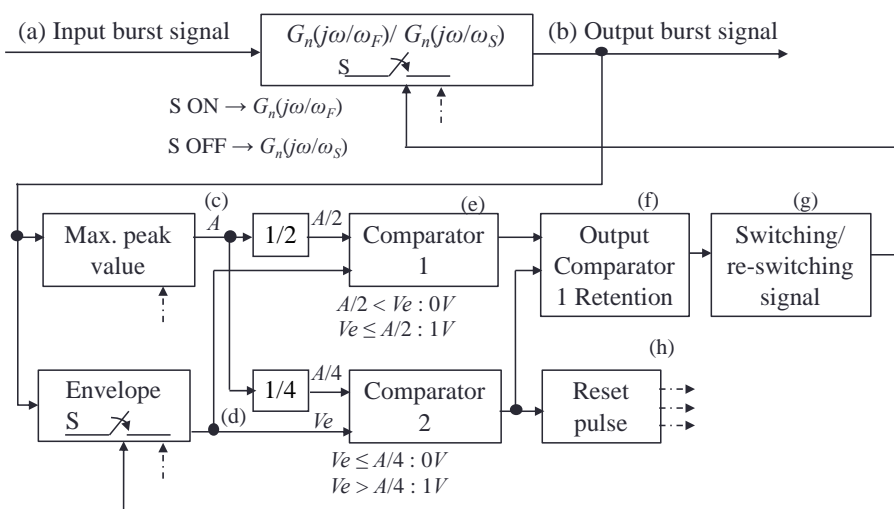


Figure 1. Function block of automatically switching LCR circuit

The maximum peak output value A is shown in Figure 2(c). The output from comparators 1 and 2 are received and held at comparator 1 retention part, as shown in Figure 2(f). According to Figure 2(d), if the output of the envelope value V_e is $V_e > A/2$, $V_e > A/4$, the output from comparator 1 retention part becomes $0V$; if $A/4 < V_e < A/2$, the output becomes $1V$. Then, the switching/re-switching signal is generated by inverting the signal waveform at Figure 2(d), as shown in Figure 2(g). If the output is $1V$, switch S will be

turned ON, and $G_n(j\omega/\omega_F)$ circuit is selected. If the output is 0V, switch S will be turned OFF, and $G_n(j\omega/\omega_S)$ circuit is selected.

For the output of comparator 2, if $V_e > A/4$, the output becomes 1V; if $V_e < A/4$, the output becomes 0V. As a result, the amplitude of the envelope drops until $A/4$, thus indicating the end of a burst signal. When the end of a burst signal is detected, the output of switching/re-switching signal becomes 1V, and $G_n(j\omega/\omega_S)$ is re-switched to $G_n(j\omega/\omega_F)$ circuit, as shown in Figure 2(d).

Reset pulse signal shown in Figure 2(g) is generated by differentiating the signal in Figure 2(d), and each part of the electric charge realized from the capacitor is released. Besides that, the loop of the coil is open, and the accumulative energy is released instantaneously after the re-switching mechanism is activated.

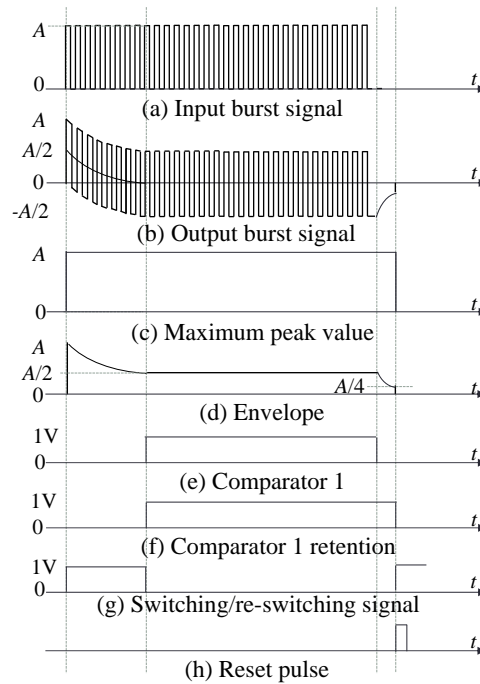


Figure 2. Signal waveform of automatically switching LCR circuit

3. RESULTS AND ANALYSIS

The automatic switching between fast response $G_n(j\omega/\omega_F)$ and slow response $G_n(j\omega/\omega_S)$ circuits is designed from a simulation in PSpice, and the characteristics of 10-bit and 20-bit 0, 1 consecutive codes are evaluated. The design of the automatically switching circuit is shown in Figure 3.

3.1. 10-Bit Consecutive Codes

A similar 10-bit consecutive 0 code is placed at the vicinity of switching mechanism occurring at time, $t_u = 2, 4, 6, 7, 8$ ns of the input burst signal. Then, the characteristics of the output burst signal are evaluated. As shown in Figure 4, the result shows that fast response circuit $G_n(j\omega/\omega_F)$ automatically switches to slow response circuit $G_n(j\omega/\omega_S)$ right after the maximum peak value of the output burst of $G_n(j\omega/\omega_F)$ is $1/2$, and the DC components of the input burst converges to 0, regardless of the consecutive codes.

Subsequently, similar 10-bit consecutive codes of 1 are placed at the vicinity of switching mechanism at time $t_u = 2, 4, 6, 7, 8$ ns of the input burst signal, and the characteristics of the output burst signal are evaluated. Figure 5 shows the anticipated result, similarly unaffected by the presence of the consecutive codes.

3.2. 20-Bit Consecutive Codes

Similarly, 20 bits of similar consecutive codes of 0, 1 are situated at the vicinity of the switching mechanism occurring at time $t_u = 2, 4, 6, 7, 8$ ns of the input burst signal, and the characteristics of output burst signal are evaluated. Based on Figure 6 and Figure 7, when 20 bits of the same consecutive codes of 0, 1 are placed at the vicinity of switching mechanism occurring at time $t_u = 4$ ns and $t_u = 2$, the results are unobtainable due to the output burst signal being affected by the existence of the consecutive codes.

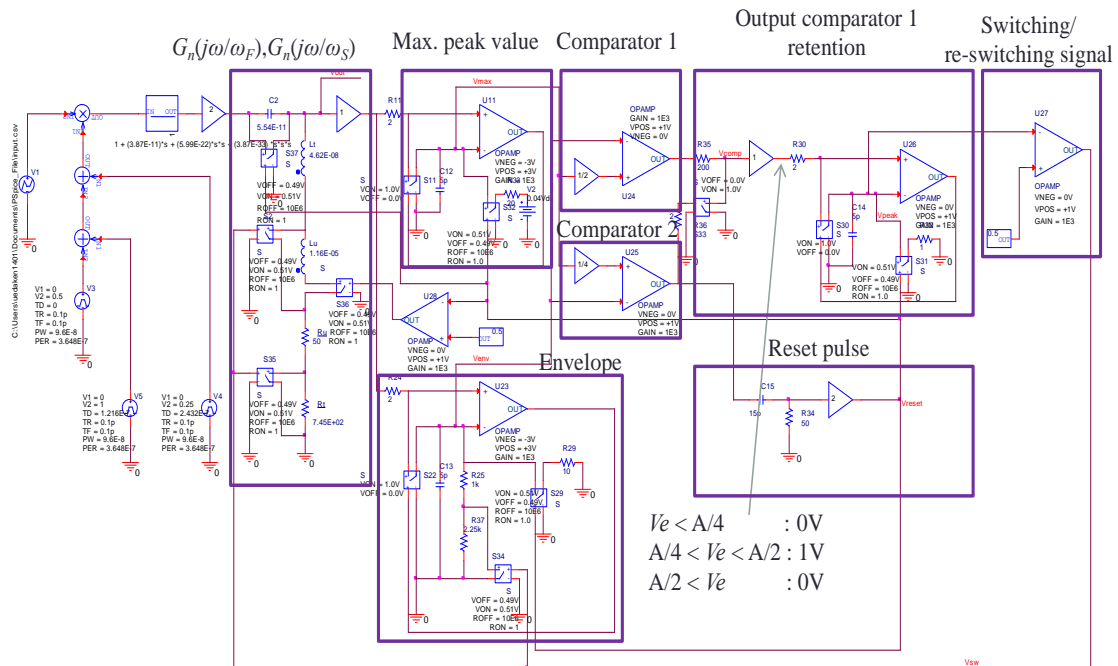


Figure 3. Example of automatically switching circuit in PSpice

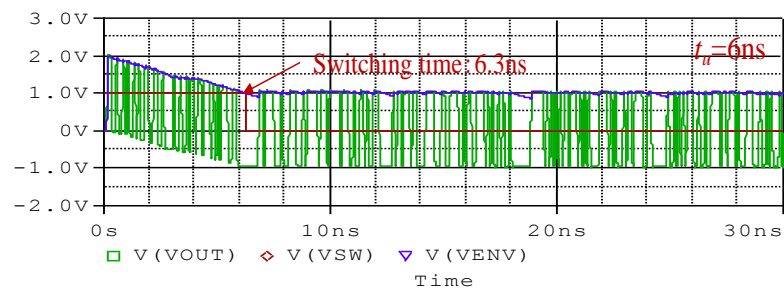


Figure 4. 10 bits of 0 code

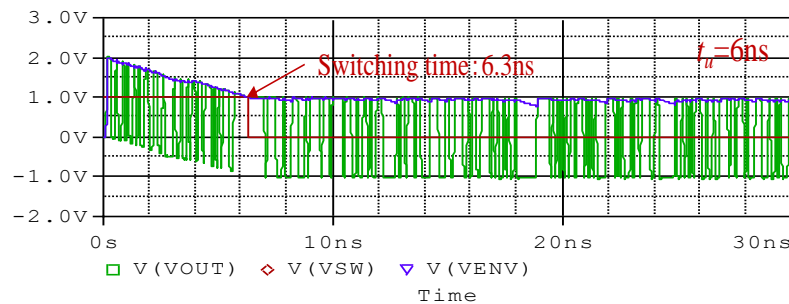


Figure 5. 10 bits of 1 code

3.3. Discussion

Based on the characteristics analyses in Figure 6, the fast response $G_n(j\omega/\omega_F)$ switches to slow response $G_n(j\omega/\omega_S)$ circuits at switching time $t = 5.6$ ns. For switching time $t > 5.6$ ns, the envelope value V_e is $V_e > 1$, as shown in Figure 8(b). When $t = 5.6$ ns is detected, the output of comparator 1 should become $V_{comp} = \text{High}$ (1V). However, V_{comp} remains as $V_{comp} = \text{Low}$ (0V), as shown in Figure 8(c). This causes

the output of comparator 1 retention, V_{peak} to gradually decrease from 1V to 0.5V as shown in Figure 8(d), and switch V_{SW} switches from OFF to ON. Correspondingly, the slow response $G_n(j\omega/\omega_S)$ re-switches to fast response $G_n(j\omega/\omega_F)$ circuit at $t = 19.0$ ns.

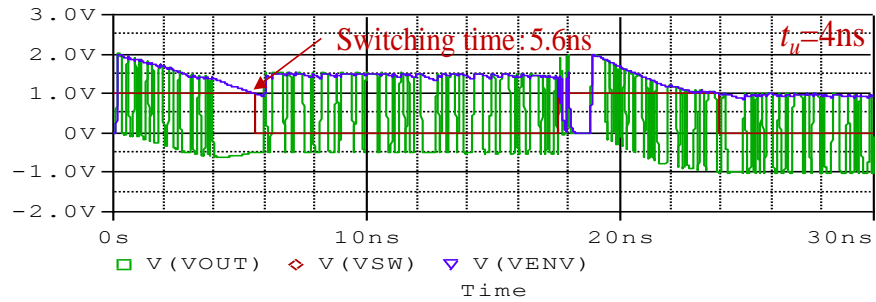


Figure 6. 20 bits of 0 code

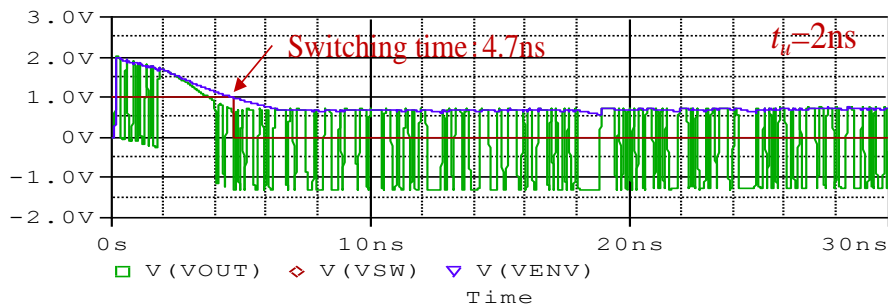


Figure 7. 20 bits of 1 code

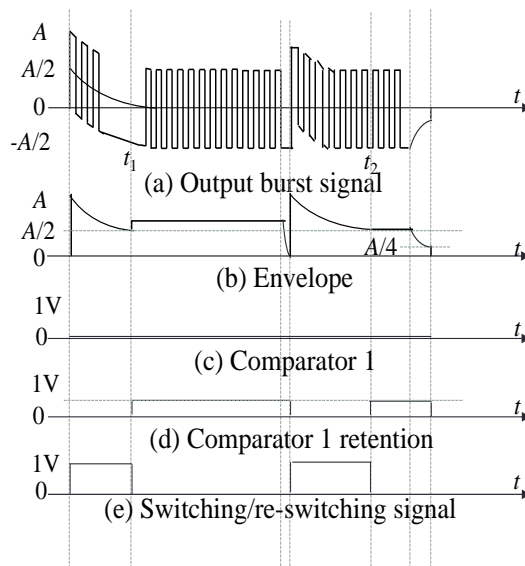


Figure 8. Signal waveform of evaluation in Figure 6

4. CONCLUSION

The evaluation on similar 10-bit consecutive codes in the burst mode receiver shows better performance than that of the 20-bit consecutive codes. This confirms an instantaneous automatic switching from fast response circuit $G_n(j\omega/\omega_F)$ to slow response circuit $G_n(j\omega/\omega_S)$ after the maximum peak value of output burst of $G_n(j\omega/\omega_F)$ is 1/2, and the DC components of input burst converges to 0, uninfluenced by the existence of the consecutive codes. Items for further study may involve the enhancement and assessment of the 20-bit consecutive codes in burst mode receiver through simulations.

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