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Adaptive random testing with total cartesian distance for black box circuit under test

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ABSTRACT

Testing and verification of digital circuits is of vital importance in electronics industry. Moreover, key designs require preservation of their intellectual property that might restrict access to the internal structure of circuit under test. Random testing is a classical solution to black box testing as it generates test patterns without using the structural implementation of the circuit under test. However, random testing ignores the importance of previously applied test patterns while generating subsequent test patterns. An improvement to random testing is Antirandom that diversifies every subsequent test pattern in the test sequence. Whereas, computational intensive process of distance calculation restricts its scalability for large input circuit under test. Fixed sized candidate set adaptive random testing uses predetermined number of patterns for distance calculations to avoid computational complexity. A combination of max-min distance with previously executed patterns is carried out for each test pattern candidate. However, the reduction in computational complexity reduces the effectiveness of test set in terms of fault coverage. This paper uses a total cartesian distance based approach on fixed sized candidate set to enhance diversity in test sequence. The proposed approach has a two way effect on the test pattern generation as it lowers the computational intensity along with enhancement in the fault coverage. Fault simulation results on ISCAS'85 and ISCAS'89 benchmark circuits show that fault coverage of the proposed method increases up to 20.22% compared to previous method.

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1. INTRODUCTION

The simplest approach to test stuck-at faults in digital combinational circuits is to use an exhaustive test pattern generation, where the test set comprises of all the possible input combinations (input space) [1-10]. For an N-input circuit under test, it requires 2^N test patterns to achieve complete fault coverage. Consider exhaustive testing of c7552, ISCAS'85 benchmark circuit with 207 primary inputs. Exhaustive testing requires 2^{207} test patterns, therefore, regardless of the clock speed testing process will take substantial amount of time to complete. Random testing is another type of test pattern generation that chooses random test patterns from input space and applies on circuit under test until the required fault coverage is achieved [5, 11-17]. Unfortunately, literature suggests random testing is unable to utilize all the information available in the black box environment. Random testing uses only the information of the primary inputs to generate subsequent patterns. However, the success or failure rate of the previously executed test patterns is important to derive effective subsequent test patterns. Random testing fails to utilize this information. As a result, test length increases without any effect on the fault coverage.

Compact size of test sequence has dual advantage on the circuit testing as both test time and test power can be minimized by reducing the length of testing sequence. Moreover, subsequent test patterns targeting different fault location in the circuit under test have higher probability of exposing novel faults. A diverse testing sequence minimizes generation of redundant test patterns that target same fault locations with subsequent test patterns. Therefore, Random like testing sequence [14] uses maximization of total hamming distance (THD) to enhance the fault coverage. Every subsequent test pattern is chosen such that it has maximum THD with the set of previously executed test patterns. Another improvement to random testing is Antirandom [18-22] that proposes two way distance calculations. Antirandom uses THD along with total Cartesian distance (TCD) between test patterns in order to diversify the testing sequence. The resulted test sequence is able to achieve high fault coverage with few number of test patterns. However, the distance computations restrict the use of Antirandom to small input circuit under test.

In literature, a number of approaches have been proposed to reduce the computational complexity in distance calculation. Fast antirandom [23] uses centralization and orthogonal selection to avoid the TCD calculations for subsequent test pattern selection. Fast Antriandom successfully reduces the computational complexity but fault coverage is highly dependent on the initial set of seeding test patterns. Increase or decrease in the quantity of seed patterns highly effects the quality of the testing sequence. Scalable test pattern generation [24] proposes addition of a distance factor in the previously executed patterns to generate subsequent test patterns. The addition factor is an important variable in this type of test pattern generation. The lower value of addition factor may result in a large amount of test patterns and vice versa according to hamming bound. Moreover, there are no guidelines available for the determination of addition factor. Scalable antirandom [11] testing proposes another test pattern generation method to avoid distance computations in the diversity enhancement of testing sequence. Scalable antirandom uses periodic bit swapping in regular intervals of 2^n, where "n" represents the index of primary input. However, with the reduction in computational complexity the fault coverage is highly compromised. Fixed sized candidate set adaptive random (FSCS-ART) [25, 26] testing uses selection of "k" candidate patterns. The distance computations are only carried out on the fixed sized candidate set and the fittest candidtate is selected. FSCS-ART suggests distance computations of each candidate with the previously applied test patterns. The minimum of the distances with the previously executed patterns is selected for each of the candidate pattern. Consequently, a candidate with maximum of the minimum distances is selected. All these algorithms successfully reduce the computational complexity at the cost of compromised fault coverage [1, 2, 7, 8, 10, 27, 28].

This paper proposes an alternative summation of distances approach inspired by the algorithm of Antirandom test pattern generation. The proposed approach uses summation of the individual distances for fixed sized candidate set. A candidate pattern with maximum of the summed distances is selected for the subsequent selection. Therefore, diversity in the testing sequence is enhanced by exposing large number of faults with less number of test patterns. The proposed algorithm is implemented using high level MATLAB programming. Moreover, ISCAS'85 and ISCAS'89 benchmark circuits are used to test the effectiveness of the proposed algorithm. These benchmark circuits range form 7 to 233 primary inputs providing intense challenge to the proposed algorithm of test pattern generation.

The remainder of this paper is organized as follows. Section 2 proposes the methodology to generate test patterns for enhanced diversity in testing sequence. Section 3 presents the fault simulation setup and result on ISCAS'85 and ISCAS'89 benchmark circuits. The fault simulation results are followed by comparative discussion on fault coverage. Section 4 concludes the paper with the summary of findings, their significance and future directions in the area of black box circuit testing.

2. RESEARCH METHOD

Literature review in the previous section has shown that a number of test generation techniques have been proposed to reduce the computational complexity in the generation of diverse testing sequence. This section proposes a max-sum approach for black box circuit testing in order to achieve high fault coverage with comparatively same computational complexity as FSCS-ART. The proposed approach uses carteisan distance (CD) and TCD in order to diversify the testing sequence. Testing sequence is a collection of test patterns represented by T. As shown in (1) and (2) report definitions for CD and TCD. These definitions are true for testing sequence $T = \{t_0, t_1, t_2 \dots t_{m-1}\}$ and test pattern $t_{i,j} \in \{0,1\}$ where $j \leq N$ for an N-input circuit under test [1, 2, 7, 8, 10, 11, 18, 20, 27, 28].

CD represents the distance between two individual test patterns. However, TCD is a summation of individual CDs for a candidate pattern with the list of previously executed test patterns. CD can also be interpreted as square root of bitwise XOR summation between two test patterns. As shown in (2) represents TCD for a candidate pattern t_m with a test set T of previously applied test patterns. CD of a candidate pattern

t_m is calculated with each pattern in the test set T and summation of individual CDs is termed as TCD. The next subsection proposes selection criteria for an adaptive random test generation algorithm with fixed sized candiates using TCD.

$$CD(t_1, t_2) = \sqrt{\sum_{i=0}^{n} t_{1,i} \oplus t_{2,i}} \quad (1)$$

$$TCD\ (t_m, T)\ =\ \sum_{k=1}^{m-1} CD(t_m, T_k) \quad (2)$$

2.1. Propoesd algorithm

Test pattern generation is a process of successive selection of test patterns from set of candidate patterns to build a testing sequence. The selection criteria varies with the different algorithms in literature. Moreover, the length of candidate set may reach $2^N - 1$ for an N-input circuit under test. Therefore, distance calculations for each of the candidate test patterm leads to a computational intensive process. This paper proposes selection of a fixed size of candidate set and computes only those patterns for distance calculations.

Table 1 shows the steps of the proposed algorithm for test pattern generation. The proposed algorithm uses generation of the first test pattern to be all ones pattern. This is to avoid the infinite loop in pseudorandom generation with an input of all zeros pattern. The seeding pattern t_0 can be any pattern except all zeros pattern. This paper proposes psuedorandom generation of k patterns with a seed of the last pattern in the test sequence. Resulted k patterns are used to calculate individual TCDs with test sequence. The proposed algorithm uses TCD instead of CD as used in FSCS-ART. Therefore, the proposed algorithm of adaptive random circuit testing uses max-sum procedure with TCD calculations. The resulted TCDs are used to select a test pattern with maximum TCD and test sequence is updated. The proposed algorithm enahces the diversity in the test sequence by using summation of individual CDs and maximum of the k candidates is chosen to generate a divergent selection for subsequent test pattern.

Consider test sequence generation for c17, ISCAS'85 benchmark circuit. c17 has 5 primary inputs and 2 primary outputs. Following the proposed algorithm in Table 1 and using $k = 5$, the first element of the test sequence is $t_0 = \{11111\}$. Step 2 in the algorithm requires random generation of k patterns. Therefore, pseudorandom generation is carried out with a seed of last pattern in the test sequence (In this case $t_0 = \{11111\}$). Table 2 lists all the pseudorandom patterns along with their individual TCDs for the first test pattern selection. It can be seen that pattern $\{10001\}$ has maximum value of TCD. Therefore, the test sequence is updated by adding $\{10001\}$ in the test sequence. Similarly, for the second test pattern selection, last test pattern in the test sequence is used as seed for pseudorandom generation. Moreover, a random pattern with maximum TCD is selected as subsequent test pattern in the test sequence. This example only generates a test sequence of test length equal to 3. However, the process is repeated for larger test sequences.

Table 1. Proposed algorithm for test pattern generation

Step #	Operation
Step 1	Generate $t_0 = \{111 \ldots 1\}$ test pattern and put it in the test sequence.
Step 2	Randomly select "k" patterns for the distance computations.
Step 3	Calculate THD of each pattern in Step 2 with the test sequence.
Step 4	Select a pattern with maximum THD in Step 3.
Step 5	Add the selected pattern in test sequence.
Step 6	Repeat Step 2 to Step 5 until required test length is achieved.

Table 2. c17 test pattern generation using proposed method

Test pattern selection 1			Test Pattern Selection 2		
Pseudorandom generation k = 5, seed = {11111}[26]		Updated test sequence	Pseudorandom generation k = 5 , seed ={10001}		Updated test sequence
Patterns	TCD with test sequence		Patterns	TCD with test sequence	
10001	1.7321		01101	3.1463	
01101	1.4142	$\{t_0 = 11111,$	11010	3.1463	$\{t_0 = 11111,$
11010	1.4142	$t_1 = 10001\}$	11011	2.4142	$t_1 = 10001,$
11011	1.0000		11001	2.4142	$t_2 = 01101\}$
11001	1.4142		11101	2.4142	

3. RESULTS AND ANALYSIS

International symposium for circuits and system provides list of benchmark circuits. These benchmark circuits are used by reserearchers to verify the effectiveness of the test sequences. This paper uses

both combinational and sequential circuits to test the effectiveness of the proposed test generation algorithm. The proposed algorithm is enhancement of FSCS-ART, therefore, a fault coverage comparison is carried with FSCS-ART on ISCAS'85 [29] and ISCAS'89 [30] benchmark circuits. The proposed algorithm is implemented using high level programming in MATLAB to generate list of test patterns for each benchmark circuit. The resulted test sequences are exposed to the benchmark circuits using ATLANTA fault simulator. ATLANTA is capable of generating report on the detected faults for an input test sequence. Therefore, quality of test patterns is analyzed by the measure of fault coverage with each testing sequence.

Table 3 lists ISCAS'85 and ISCAS'89 benchmark circuits with primary inputs in second column ranging from 7 to 233. The second column gives the number of outputs for the benchmark circuits. The complexity of the circuit can be analyzed by the number of gates shown for each circuit in the fourth column of Table 3. Each ISCAS'85 and ISCAS'89 benchmark circuit is tested using two different types of test sequences. Firstly, using the FSCS-ART algorithm that uses max-min approach to generate subsequent test patterns. Secondly, test sequence is generated using proposed ART with TCD computations for subsequent test pattern selection. Length of test sequences is given in column six of Table 3. The number of faults exposed by each test sequence are listed in column seven and column eight of Table 3. It can be observed that the number of faults exposed by the proposed approach are always higher than the number of faults exposed by FSCS-ART. This is in accordance with the hypothesis that diverse selection of subsequent patterns result in exposing different faults in a black box environment.

Tabel 3. Fault coverage comparison on ISCAS'85 benchmark circuits

Circuit Name	Inputs	Outputs	Gates	Faults	Test Length	FSCS-ART(max-min) [9]	ART(max-sum)	Percentage Increase
c1908	33	25	880	1879	50	1254	1348	7.49
c432	36	7	160	524	50	425	449	5.64
c3540	50	22	1669	3428	50	2125	2268	6.72
c880	60	26	383	942	50	706	779	10.34
c5315	178	123	2307	5350	50	2457	2954	20.22
c7552	207	108	3512	7550	100	5350	5660	5.79
c2670	233	140	1193	2747	100	1774	1869	5.35
s298	17	20	119	308	50	270	275	1.85
s344	24	26	101	342	50	318	326	2.51
s349	24	26	104	350	50	324	332	2.46
s382	24	27	99	399	50	352	373	5.96
s400	24	27	106	424	50	369	392	6.23
s444	24	27	119	474	50	396	404	2.02
s510	25	13	211	564	50	459	469	2.17
s526	24	27	141	555	50	386	419	8.54
s820	23	24	256	850	50	408	420	2.94
s832	23	24	262	870	50	407	419	2.94
s1423	91	79	657	1515	50	1152	1210	5.03
s5378	214	213	2836	4551	100	2661	2797	5.11

Last column in Table 3 lists the percentage increase in fault coverage with the proposed algorithm relative to FSCS-ART. An average of 5.7532% of fault coverage increase is observed with the proposed algorithm. Table 3 shows c5315 benchmark circuit with 178 primary inputs is exposed with 20.22 % increased fault coverage with the proposed method. The fault coverage comparison confirms the effectiveness of the proposed test pattern generation for black box circuit testing.

Figure 1 shows a fault coverage comparison on c2670 benchmark circuit. This is the largest circuit available in the ISCAS'85 benchmark list, with 233 inputs and 1193 internal gates. c2670 benchmark circuit is tested using both FSCS-ART and proposed algorithm of ART TCD approach. The resulted fault coverage is plotted with regular intervals of 10 patterns. The red curve in the Figure 1 represents the fault coverage achieved by FSCS-ART. Black dashed curve represents the fault coverage achieved by the proposed ART max-sum algorithm. It can be observed that the proposed algorithm is able to enhance fault coverage with the increasing length of the test sequence. Initially test coverage is same for first 10 test patterns. Whereas, proposed algorithm gives higher fault coverage as test length exceeds 20 test patterns. This is because diversity is enhanced as the test length increases. Moreover, the TCD maximization enhances diversity between the previously executed patterns and subsequent test pattern with each test pattern selection.

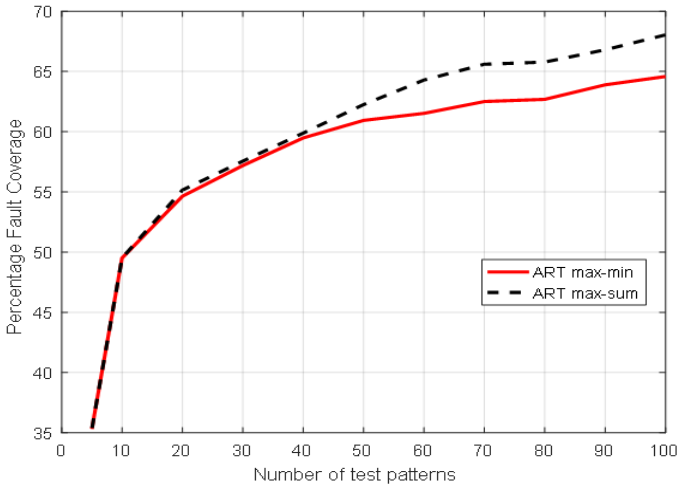

Figure 1. Percentage fault coverage comparison on c2670 benchmark circuit

4. CONCLUSION

This paper proposed ART TCD algorithm to enhance diversity in the testing sequence for high fault coverage in black box circuit testing. Fault simulation results have shown that the proposed approach is able to improve fault coverage by 20.22% for c5315 and an average of 5.7532% increase in fault coverage is observed for ISCAS'85 and ISCAS'89 benchmark circuits. A comparative study reveals that proposed approach of adaptive random testing is more effective in achieving higher fault coverage as compared to FSCS-ART with max-min approach. One possible way to utilize proposed algorithm is to replace it with deterministic testing after sufficient high fault coverage is achieved. This is due to the non testing capability of the hard to test faults. Moreover, this research uses fixed candidate size of 25 for all benchmark circuits except 40 for c7550 and c2670 benchmark circuit. However, additional research is required to optimize the candidate size for further increase in fault coverage.

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