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DC bus stabilization using passive damping network in distributed power system with constant power load

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Abstract

In distributed power system (DPS), the stability performance is always associated with the behaviour of constant power load (CPL). Since DPS large complex system build up from many power electronic converters, the DC bus of the system becomes unstable due to the strenuous action from power converters. When these converters tightly regulated, it behaves as constant power load and exhibit negative incremental input impedance which becomes the main reason in stability degradation of DPS. In this paper, four passive damping network topologies was proposed to reduce the DC bus instability. The best damping performance of the topologies was chosen and analysed using MATLAB/Simulink. The DC bus performances was studied in four cases which are damping behavior due to CPL power level, CPL disconnection, effects of filter and damping capacitor, and effects of filter cut-off frequency. Simulation results obtained shows that the DC bus was successfully stabilized and the resonance damped when passive damper installed. An experimental hardware tests was conducted to verify the proposed damping method and the results were compared with the simulated output waveforms. The analysis results in overshoot, settling time and steady state error of bus voltage shows system improvement with the proposed damper network.

Keywords*: constant power load, distributed power system, negative incremental impedance, passive damping, stabilization*

1. Introduction

Distributed power system (DPS) is a system build up from spatially separated power processing units which connected to electrical loads such as power electronic converter via DC bus [1-4]. The DPS system are most popular known to be exceptionally suited for power grid integration using renewable energy as power sources and expected to be the key-enabling technology in the future [5]. The main advantage in employing DPS are due to the weight, size, regulatory performance and flexibility of the system [4-6]. Due to the wide range of DPS flexibility, it is being used extensively in many fields such as aircraft, hybrid electric vehicles, military naval vessel and telecommunication network [2], [7], [8]. However, there are some unavoidable weakness in DPS. Yet the most critical issue concerned is the stability degradation of the system caused by the interaction of power converters. This could lead to the failure of the system performance.

The causes of DC bus instability in DPS system

When various subsystems interconnected together to one common DC bus bar, the interactions between these subsystems may complicate the whole systems performance. Since each converter in the interconnected system possesses their own internal control function to regulate its output voltage, those converters tend to draw constant power. This causes the power converter produces negative incremental input impedance within their closed loop bandwidth. In [2-13] the authors describe that interaction between converters and bus instability causes unequal power distribution among parallel converters which in turn produce enormous stress on the converter module. Moreover, a tightly regulated power converter will exhibit negative incremental impedance which behaves as constant power load (CPL). The existence of CPL is the main reason in the degradation of the systems performance and instability.

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Constant power load and negative incremental impedance

Constant power load is a load that consumes fixed amount of power irrespective the voltage supply received by it [9]. It is usually represented by power electronic converter that attempts to sink constant power from DC bus of the system and causes constant power characteristic arise [14]. This CPL's characteristic is commonly known as negative impedance characteristic or negative incremental impedance. Figure 1 shows the hyperbolic power contour curve of the negative impedance behaviour of constant power load. The curve represents how much current that the load can sink at different voltages up to their maximum power level. The graph behaves such that the current increases as voltage applied to it decrease and vice versa.

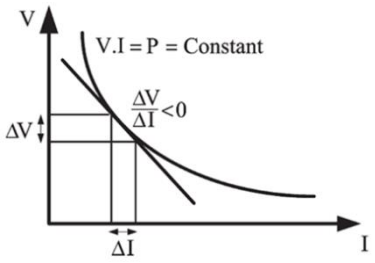


Figure 1. Negative impedance characteristic of constant power load

2. Passive Damping Network Topologies

Passive damping is a method used to increase stability of system where damper network consists of resistor, inductor and capacitor configured into certain topology and installed at output filter of the system. A suitable damper should be used for a particular system so that the damping performance and stability of the system can be assured. The Middlebrook stability criterion is a very powerful method in determining stability behaviour of converter when connected to input filter [7]. Therefore, the concept of the instability and causes of resonance output at DC bus need to be studied and analysed carefully in order to come out with the suitable passive damper. Figure 2 shows four different passive damping topologies with its transfer function as proposed in [15].

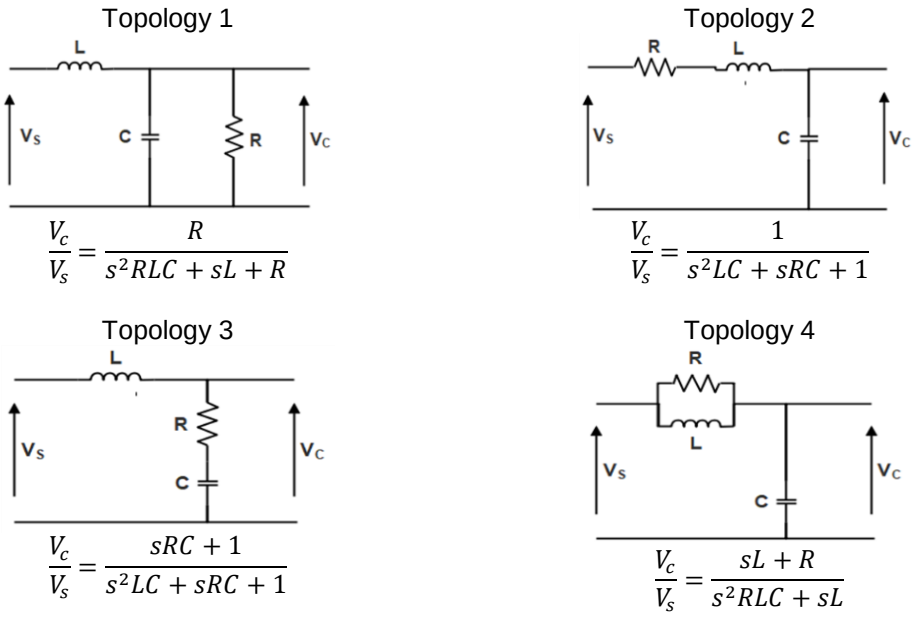


Figure 2. Passive damping topologies

By conducting Laplace transform analysis, the transfer function of each topology was obtained. Then, bode plot comparisons of the topologies was performed based on the transfer functions using MATLAB/Simulink software as shown in Figure 3. The value of parameters used for the simulation are L=100 mH, C=1000 µF and R=1 Ω. In the analysis, LC filter circuit was used as reference in determining the damping performance of the different topologies at filter resonance frequency.

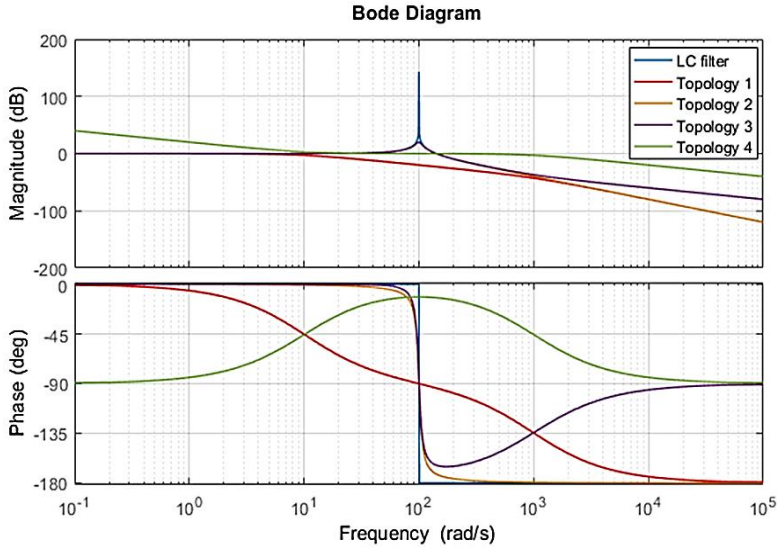


Figure 3. Bode plot response of different passive damping topologies

Based on the bode plot waveforms, at resonant frequency of 100 rad/s, damper topology 1 shows the least peaking which indicates that it has the best damping performance when connected to LC filter circuit. Additionally, the oscillation occur due to instability can also be reduced by installation a resistor in parallel to LC filter as configured in passive damper topology 1. Therefore, damper topology 1 was chosen to be installed in the DPS system with CPL. The damping performance can be further enhanced by installation of a blocking capacitor in series with damping resistor.

3. Design of DPS Circuit with Passive Damping Network

The chosen damper configuration was modelled as RC series damper having resistor and capacitor arrange in series and plugged in parallel to the DC bus system. The damping resistor serves to damp the instability at filter resonance frequency while the damping capacitor functions to block and prevent the current from entering damping resistor [5] at DC condition. Figure 4 shows the circuit connection of LC filter with passive damping network and CPL which represented by -RL.

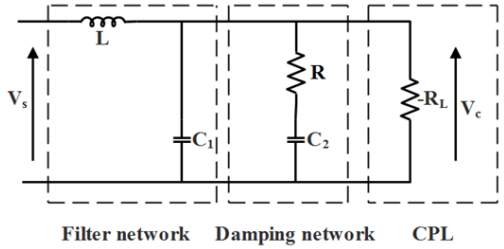


Figure 4. LC filter with passive damping network and constant power load

In the design, the damping capacitor C_2 was assumed to be much larger than filter capacitor C_1, C2>>C_1, and that makes impedance of C_2 very small at higher frequencies [2]. Therefore, the total effective resistance of the circuit can be obtained as $R_{eff} = \frac{-|R|.|R_L|}{|R|-|R_L|}$ [2]. From this relationship, it can be seen that when $|R_L|<|R|$, the LC filter will possess a net negative damping which causes DC bus to oscillate [3]. By applying the impedance stability of Middlebrooks criterion, the oscillation can be eliminated and stabilized when damping resistor R is treated to be smaller than R_L. This will make the total effective resistance to be positive since the negative impedance characteristic was eliminated [3]. Through some Laplace transform analysis made in the circuit, the output to input voltage transfer function can be obtained as shown in (1) and (2).

$$\frac{V_C(s)}{V_S(s)} = \frac{\frac{1+sRC_2}{LRC_1C_2}}{s^3+s^2\left(\frac{C_1R_L+C_2R_L-C_2R}{C_1C_2RR_L}\right)+s\left(\frac{C_2RR_L-L}{LC_1C_2RR_L}\right)+\left(\frac{1}{LC_1C_2R}\right)} \quad (1)$$

$$\frac{V_C(s)}{V_S} = \frac{sRR_LC_2+R_L}{s^3LC_1C_2RR_L+s^2(LR_L(C_1+C_2)-LRC_2)+s(C_2RR_L-L)+R_L} \quad (2)$$

Rearranging and equating the denominator in (2), yields (3)

$$-R = -\frac{1}{K} = \frac{s^2(LR_LC_1+LR_LC_2)-sL+R_L}{s^3LC_1C_2R_L-s^2LC_2+sC_2R_L} \quad (3)$$

Parameter R can be adjusted to set the poles position on s-plane so that it will satisfy the stability characteristic as desired. In order to obtain the passive damping network parameter specification, design analysis was made by factorizing (3) to yields (4):

$$\left(s+\frac{1}{RC_2}\right)\left(s^2+s\frac{1}{C_1}\left[\frac{R_L-R}{R_LR}\right]+\frac{1}{LC_1}\right)=0 \quad (4)$$

multiplying (4), results in (5)

$$s^3+s^2\left(\frac{C_1R_L+C_2(R_L-R)}{C_1C_2RR_L}\right)+s\left(\frac{C_2RR_L+\frac{L}{R}[R_L-R]}{LC_1C_2RR_L}\right)+\left(\frac{1}{LC_1C_2R}\right)=0 \quad (5)$$

Comparing both (1) and (5), an extra term of $S\frac{LR_L}{R}$ arrised. For (1) to be valid, the stability criteria of R_L>R was considered and thus creates the term $C_2RR_L \gg \frac{LR_L}{R}$. This condition results in (6).

$$C_2 \gg \frac{L}{R^2} \quad (6)$$

At this stage, the parameter of the passive damping network can be obtained provided that damping resistor R acquired first. The damping resistor R must be chosen using (7) such that it satisfies the damping performance of complex poles to the quadratic portion in (5). Damping capacitor can be obtained from (8).

$$R = \frac{R_L\sqrt{LC_1}}{\sqrt{LC_1}+\sqrt{2}C_1R_L} \quad (7)$$

$$C_2 = \frac{L}{R^2} \quad (8)$$

4. Result and discussion

The circuit was supplied by 115 V DC voltage source. This value is typical DC bus voltage used in an aircraft having loads such as cooling exhaust fan, weather radar, auto throttle and battery charger [16-17]. A step voltage of ±5 V DC is applied at voltage source to step up

and step down of the 115 V main voltage source. Resistor R_1 of 2.8 Ω was used in series with voltage source to represent parasitic element in the circuit. The circuit was then connected to LC filter used previously when comparing damper topologies, having values of L_1=100 mH and C_1 =1000 μF.

The electronic load bank was configured into several CPL power level of 30 W, 60 W and 100 W respectively. The purpose of testing different CPL power level is to investigate how far the passive damper can handle the oscillation suppression of the DPS system. The value of R_2 and C_2 used are 6.7 Ω and 2500 μF, which was obtained using (7) and (8) respectively. These values were chosen based on CPL 100 W power level and by considering the availability of components in experimental hardware set up. The completed designed simulation circuit is shown in Figure 5.

The experimental set up involves the connection of two DC power supplies each supplying main voltage 115 V and step voltage 5 V respectively, oscilloscope, and DC load bank to PCB circuit. The voltage and current were measured using Lecroy WaveSurfer 3024 Series oscilloscope to obtain more enhanced visual of the waveform. For the DC load bank, DC Electronic Load Model M9711 was used to function as CPL since the device can be set to operate in constant power mode. Figure 6 shows the project experimental set up.

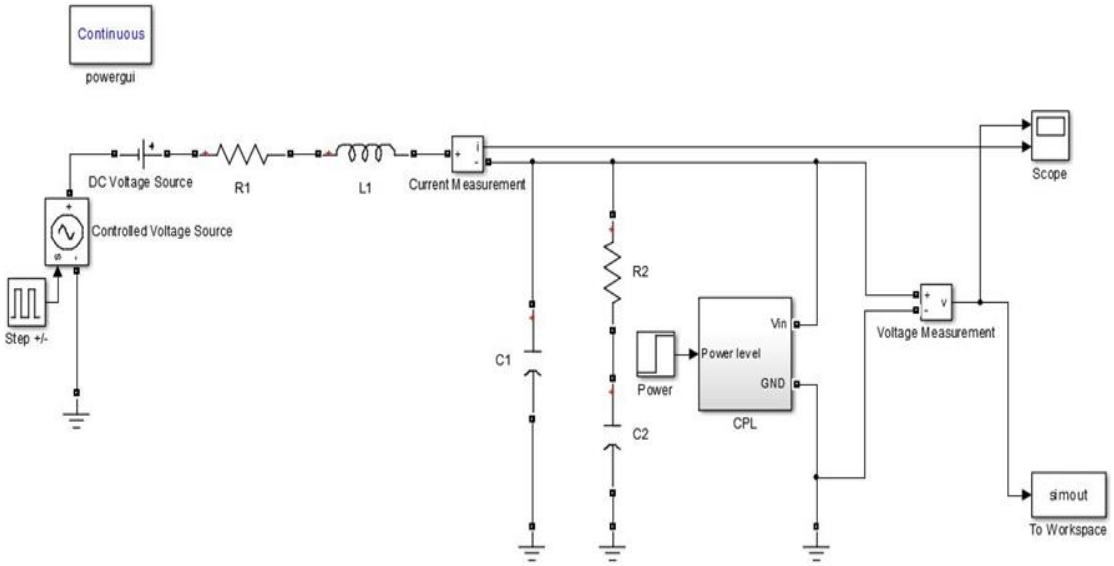


Figure 5. Simulation circuit

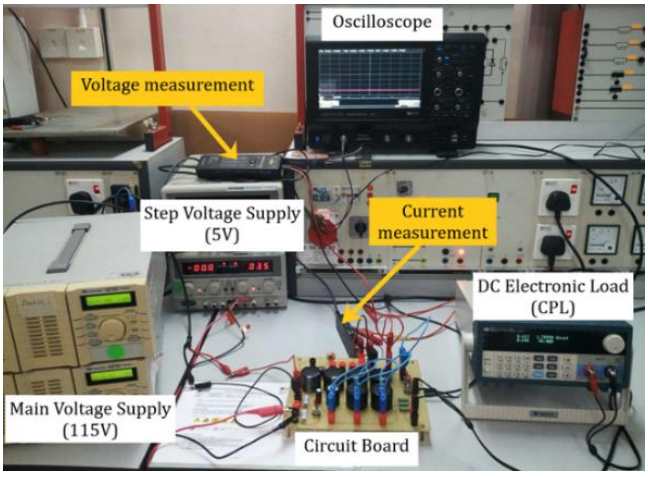


Figure 6. Experimental setup

4.1. Damping Behaviour Due to Different CPL Power Level

For the first test, the performance of the passive damping in eliminating bus oscillation with different CPL power level of 30 W, 60 W and 100 W were examined. The results for both simulation and experiment of DC bus voltage with and without passive damper with CPL power of 60W is shown in Figure 7. The analysis for damping performance was carried out based on voltage/current overshoots, settling time and steady state error responses. Table 1 summarises the comparison of bus voltage behaviour without and with passive damping network for constant DC voltage supply of 115 V.

Table 1. Comparison of DC Bus Voltage Behaviour without and with Passive Damping Network

System Behavior		Without damper			With damper		
CPL Power (W)		30	60	100	30	60	100
Overshoot (%)	Simulation	2.66	4.61	7.75	0.17	0.26	0.53
	Experiment	3.71	6.23	3.69	0.25	0.29	0.46
Settling Time (s)	Simulation	0.68	0.74	1.06	0.43	0.27	0.26
	Experiment	0.55	0.60	0.61	0.32	0.18	0.21
Steady State Error (%)	Simulation	0.72	1.63	2.90	0.70	1.40	2.40
	Experiment	0.60	0.88	0.88	0.30	0.38	0.38

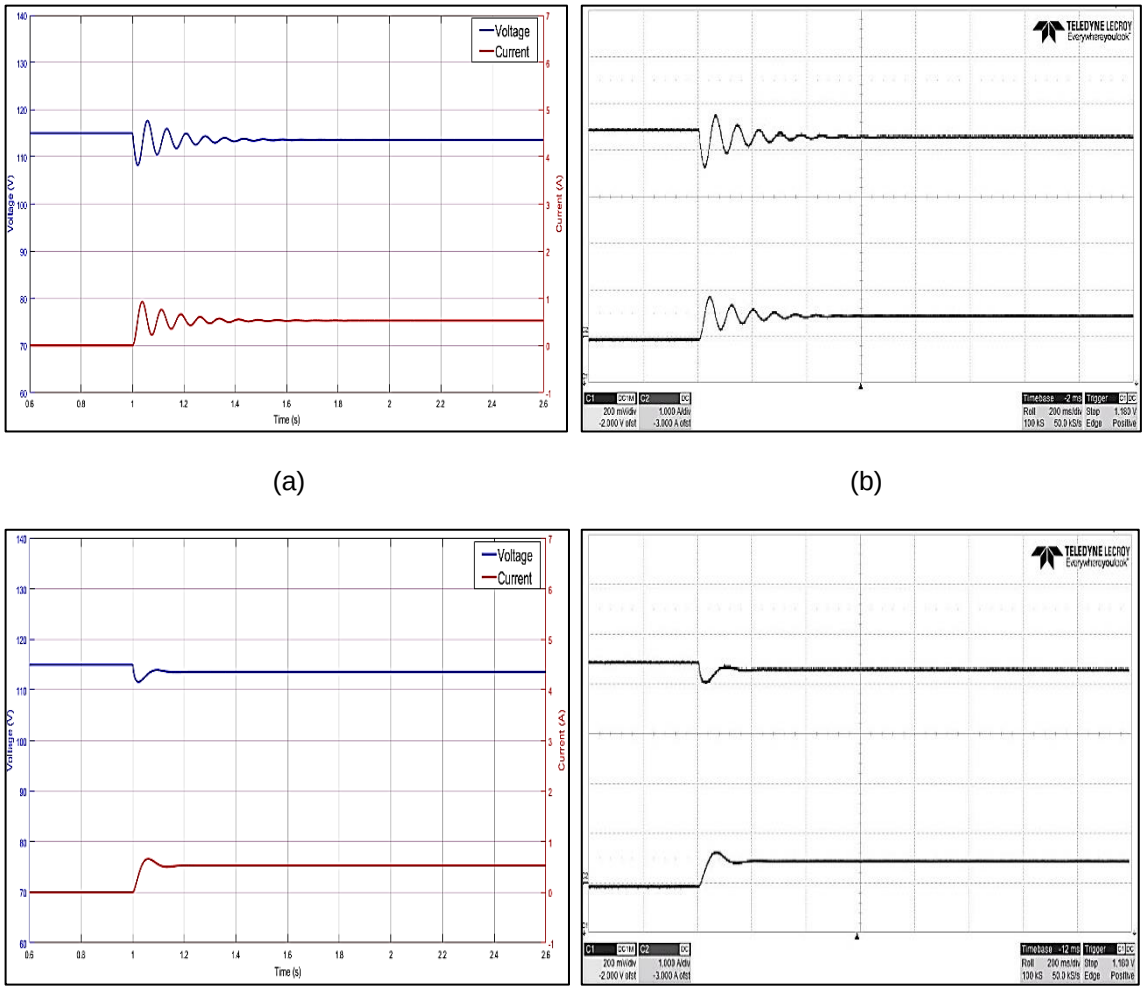
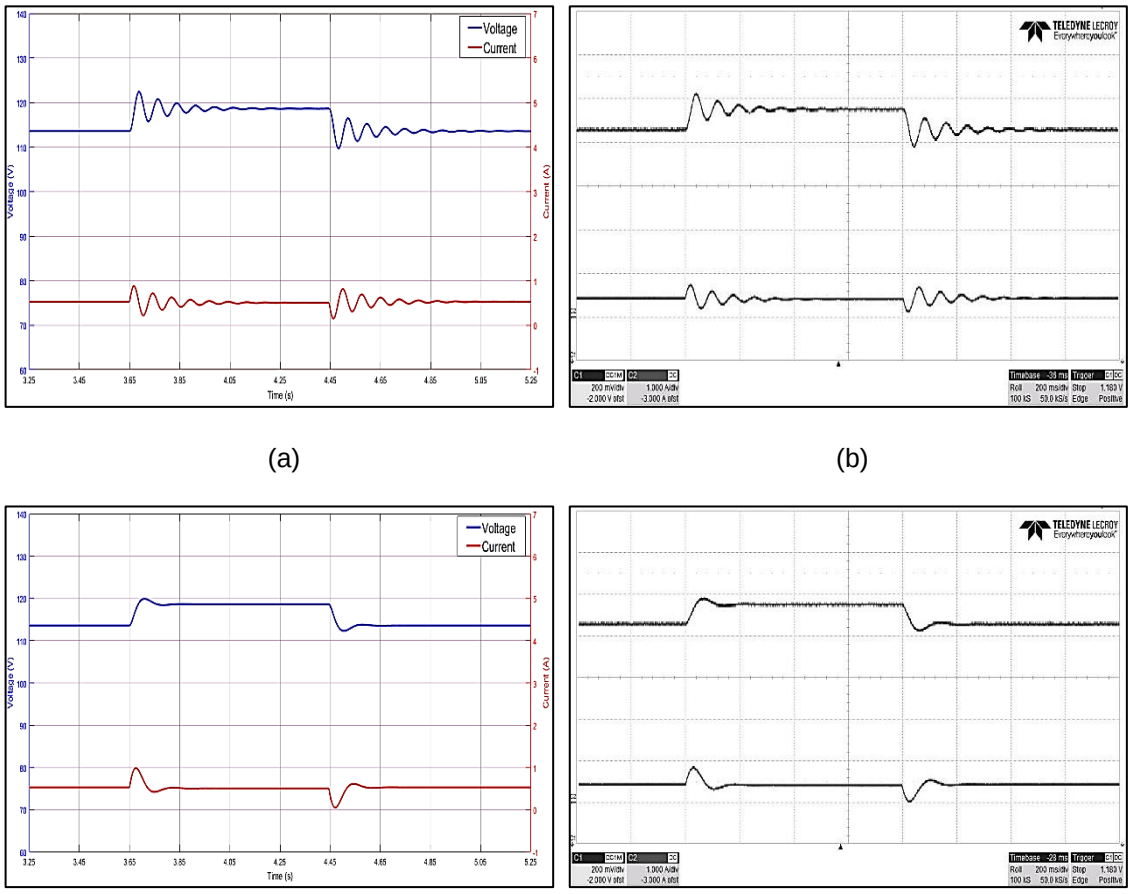


Figure 7. Output response of DC bus voltage and current with CPL power of 60 W
(a) simulation without passive damper, (b) experiment without passive damper
(c) simulation with passive damper (d) experiment with passive damper

Based on the waveform in Figure 7, when CPL connected to the system without passive damper, obviously the voltage and current oscillates before settled at steady state value. There were obvious difference in the output waveform where it shows more overshoot and vigorous oscillation as CPL power level increased from 30 W to 100 W. At 100 W, the settling time was 1.06 second which is longer compared to 30 W and 60 W CPL power. On the other hand, the difference between simulation and experiment for steady state error shows rather wide marginal deviation due to the losses occur caused by jumper wires and noises from components of PCB board.

When passive damping network connected to the system, the plots clearly shows the reduction of the DC bus voltage in terms of their overshoot, settling time and steady state error at each CPL power level. The experimental output for 100 W shows that less overshoot difference between system without damper and system with passive damper. This implies that passive damping network performance was not very suitable to be implemented for high power level. However, the settling time and steady state error for all CPL power decreased which indicates the bus stability has been improved.

The circuit was then applied with step of the input voltage of ± 5 V DC. This will cause the voltage at DC bus oscillates at 120 V for positive transience and 115 V for negative transience. The output waveform for DC bus voltage with 60 CPL power level and stepped voltage supply were shown in Figure 8. The simulation and experimental results is summarised as in Tables 2 and 3.



(a) (b)

(c) (d)

Figure 8. Output response of step DC bus voltage and current with CPL power of 60 W
(a) simulation without passive damper, (b) experiment without passive damper
(c) simulation with passive damper (d) experiment with passive damper

When the input voltage is step up to 120 V without passive damper, the output waveform shows overshoot response and oscillates at an average time of 0.70 seconds for simulation and 0.57 seconds for experiment before stable. Consequently, the percentage of overshoot increases with high CPL power level indicating the resonance behaviour or ringing occur at the DC bus. At negative transience voltage back to 115 V, the overshoot and settling time for both simulation and experiment slightly increases compared to positive transience due to the inductive kick when current decreases as result from voltage drop when stepping down the input supply.

With passive damping network introduced to the system, bus voltage at positive transience gives much less overshoot and settling time at an average time of 0.20 seconds. The output waveform produced shows that oscillation has been damped out, giving more stable performance of DC bus system. Subsequently, during step down with passive damping network, the results shows improvement in overshoot, settling time, and steady state error regardless of CPL power level for both simulation and experiment.

Table 2. Comparison of DC Bus Voltage Behaviour for Step Up Input without and with Passive Damping Network

System Behavior		Without damper			With damper		
CPL Power (W)		30	60	100	30	60	100
Overshoot (%)	Simulation	3.10	4.29	5.48	1.00	1.10	1.10
	Experiment	2.92	3.60	4.10	1.24	1.25	0.67
Settling Time (s)	Simulation	0.60	0.72	0.80	0.26	0.26	0.13
	Experiment	0.48	0.58	0.64	0.18	0.19	0.16
Steady State Error	Simulation	2.00	2.50	3.00	1.52	2.00	2.20
(%)	Experiment	1.80	0.50	2.00	1.50	0.50	1.00

Table 3. Comparison of DC Bus Voltage Behaviour for Step Down Input without and with Passive Damping Network

System Behavior		Without damper			With damper		
CPL Power (W)		30	60	100	30	60	100
Overshoot (%)	Simulation	3.36	4.55	5.01	0.17	0.18	0.18
	Experiment	2.59	3.73	4.56	0.43	0.45	0.39
Settling Time (s)	Simulation	0.57	0.74	0.86	0.18	0.28	0.19
	Experiment	0.45	0.59	0.71	0.18	0.20	0.23
Steady State Error	Simulation	1.70	2.40	2.95	0.60	1.32	1.40
(%)	Experiment	1.00	1.20	1.40	0.70	1.00	1.20

4.2. Behaviour of DC Bus Voltage When CPL Disconnected From the System

Damping disconnection test was conducted to analyse the bus voltage behaviour when CPL being disconnected from the system. The CPL was first connected to the system and allowed to become stable at steady state value before disconnecting it. Next, the behaviour was compared with presence of passive damper network in the system. Figure 9 shows the DC bus voltage behaviour at 100 W CPL power level during disconnection.

As the CPL power level increases, it can be seen that the voltage oscillates more vigorously and took longer time until it becomes stable. This was presented in Table 4 of 100 W CPL response where the system overshoot at an average of 7.93 percent with 0.49 seconds settling time which are longer compared to response in 30 W and 60 W. However, with passive damping network implemented in the system, the bus voltage waveform shows much better performance when CPL disconnected. The bus voltage shows very small overshoot with faster settling time which indicates the instability has been improved.

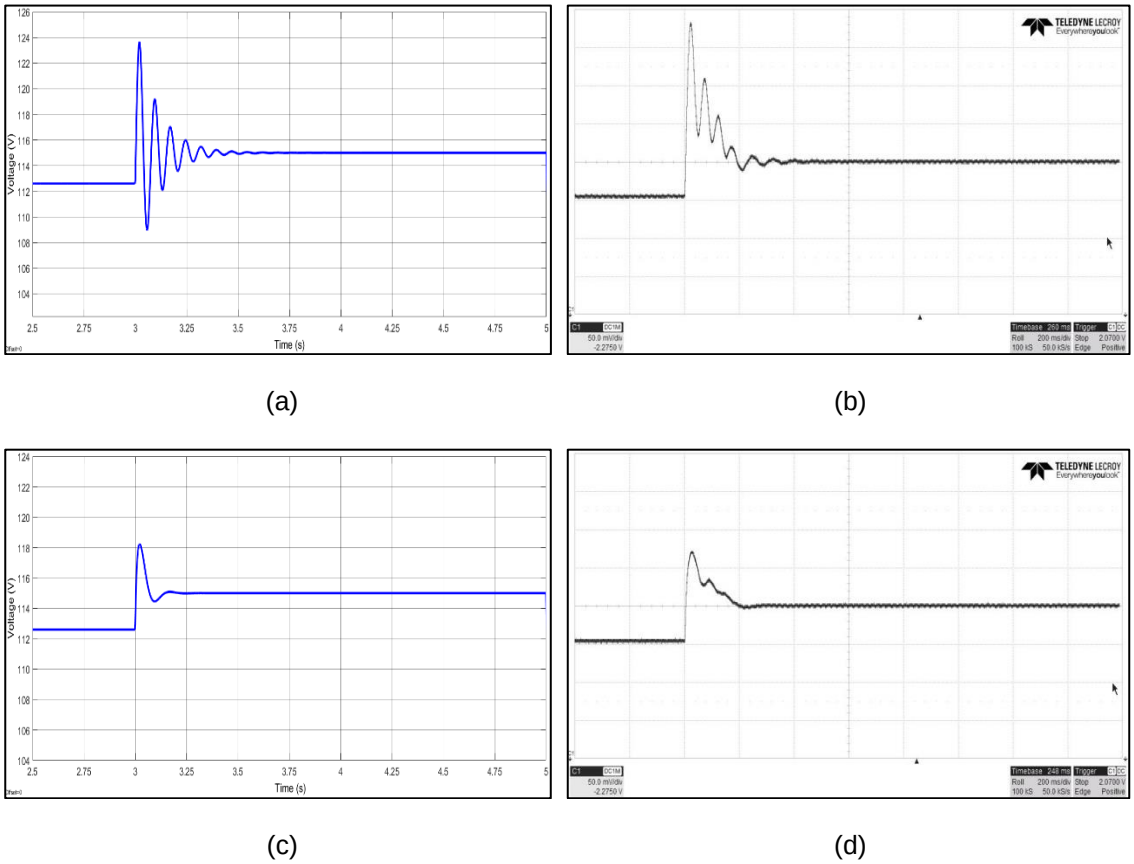


Figure 9. Bus voltage behaviour at 100 W CPL disconnection;
(a) simulation without passive damper, (b) experiment without passive damper
(c) simulation with passive damper (d) experiment with passive damper

Table 4. Comparison of DC Bus Voltage Behaviour when CPL Disconnected from the System

System Behavior		Without damper			With damper		
CPL Power (W)		30	60	100	30	60	100
Overshoot (%)	Simulation	2.43	4.52	7.83	0.87	1.46	1.55
	Experiment	2.21	4.22	8.02	0.55	1.20	1.48
Settling Time (s)	Simulation	0.22	0.41	0.49	0.13	0.18	0.21
	Experiment	0.30	0.45	0.51	0.13	0.21	0.24
Steady State Error (%)	Simulation	1.03	1.32	1.51	0.10	0.12	0.15
	Experiment	1.25	1.33	1.98	0.14	0.22	0.22

4.3. Damping Behavior Due to Effects of Damping Capacitor and Filter Capacitor

The passive damper network was connected at all times. The damping capacitor was varied to examine damping performance of the DC bus system. The CPL power level was set to constant value of 60 W throughout the test. Three conditions between the input capacitor filter and the damping capacitor was observed, which $C_1<C_2$, $C_1>C_2$ and $C_1=C_2$ where C_1 and C_2 represented by filter capacitor and damping capacitor respectively. The capacitors value was presented in Table 5.

Table 5. Capacitor Relationship with Their Benchmark Values

Capacitor Relationship	Filter Capacitor, C_1 (µF)	Damping Capacitor, C_2 (µF)
$C_1<C_2$	1000	2500
$C_1>C_2$	1000	500
$C_1=C_2$	1000	1000

Figure 10 shows the simulated DC bus voltage for each capacitor, while Figure 11 gives the experimental output waveform of the system when passive damping network connected at different capacitor relationship. Analysis for overshoot, settling time and steady state error were presented in Table 6.

Table 6. Comparison of DC Bus Voltage Behaviour for Different Capacitor Relationship with Passive Damping Network and Fixed Input Voltage

Capacitor Relationship		$C_1>C_2$	$C_1=C_2$	$C_1<C_2$
Overshoot (%)	Simulation	2.11	1.23	0.35
	Experiment	2.30	1.45	0.30
Settling Time (s)	Simulation	0.47	0.26	0.15
	Experiment	0.35	0.28	0.16
Steady State Error (%)	Simulation	1.50	1.50	1.50
	Experiment	1.56	1.48	1.48

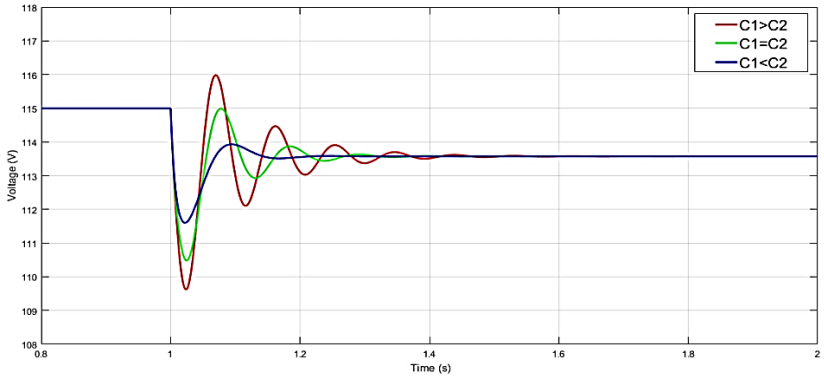
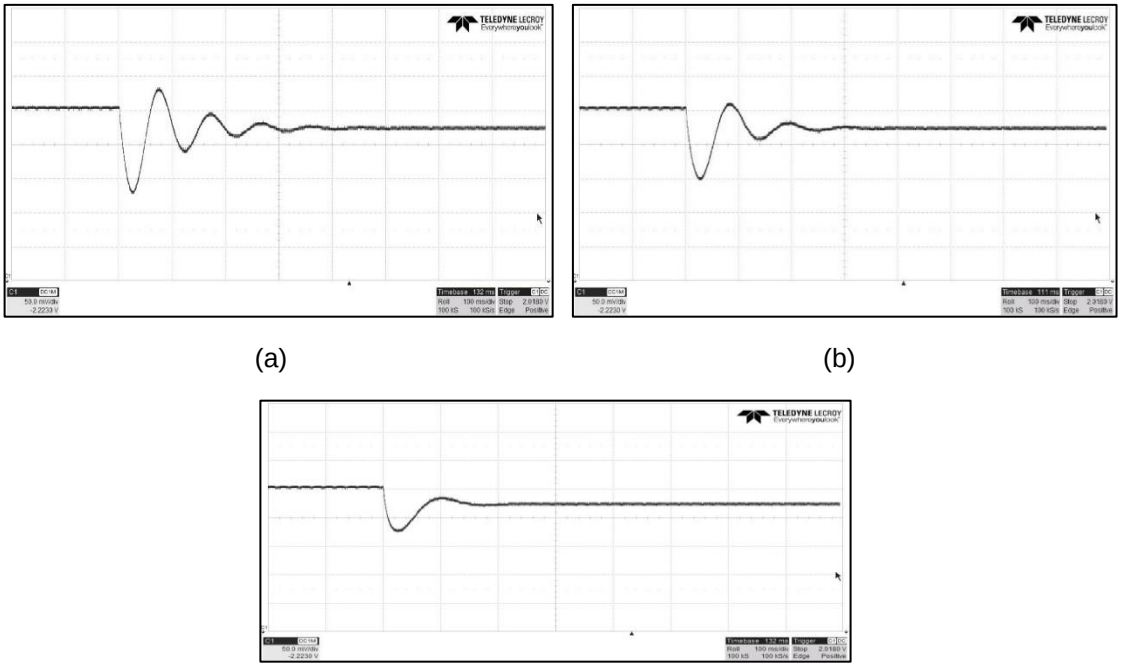


Figure 10. Bus voltage response of different capacitors relationships with fixed input voltage



(a) (b)

(c)

Figure 11. Experimental output waveform for different capacitor relationship with fixed input voltage; (a) $C_1>C_2$, (b) $C_1=C_2$ (c) $C_1<C_2$

The DC bus output waveform shows that there was still vigorous oscillation occur even after connecting damper network to the system for capacitor relation C_1>C_2. In addition, the voltage oscillates longer with high overshoot for about 0.4 seconds before settled at steady state value. This implies that design of damper network with smaller damping capacitance compared to filter capacitance gives poor damping performance in the system. However, when using larger damping capacitance compare to filter capacitance, the oscillation was suppressed and improved with very low overshoot and faster settling time at 0.15 seconds. This shows that system with C_1<C_2 gives the best damping performance.

4.4. Damping Behaviour Due to Effects of Filter Cut-off Frequency

The purpose of this test was to observe the damping capability of bus voltage when DC load with CPL characteristic connected to filter network with different cut-off frequencies. The filter cut-off frequency was varied to several benchmark values of 50 rad/s, 100 rad/s and 500 rad/s respectively. These values chosen such that frequency of the other two condition is less or more than 100 rad/s of original filter cut-off frequency accordingly. Using the filter cut-off frequency formula $\omega = \frac{1}{\sqrt{LC}}$, the value of filter inductor and capacitor can be manipulated to give the desired values as presented in Table 7.

Table 7. Parameter Values for Varied Cut-off Frequency Filter

Cut-off Frequency (rad/s)	Filter Inductor, L (mH)	Filter Capacitor, C_1 (μF)
50	100	4000
100	100	1000
500	100	40

Figures 12 and 13 show the results of simulation and experiment respectively. The analysis for overshoot, settling time and steady state error for each cut-off filter frequency level were presented in Table 8. The CPL power level was maintained at 60 W for all frequencies.

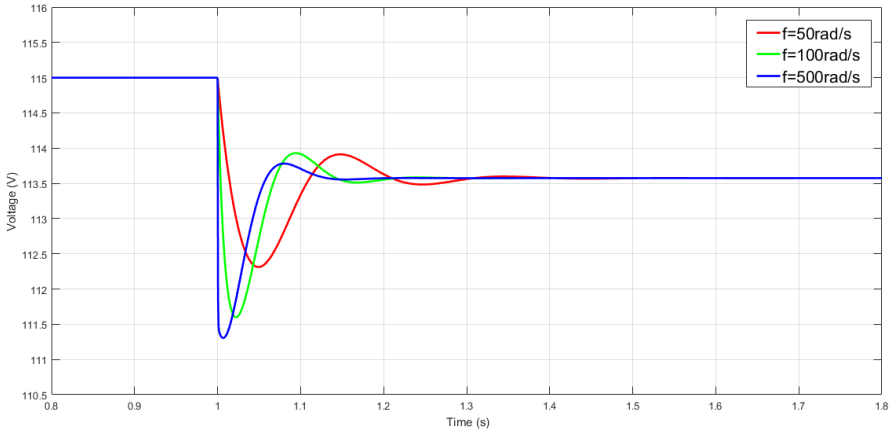
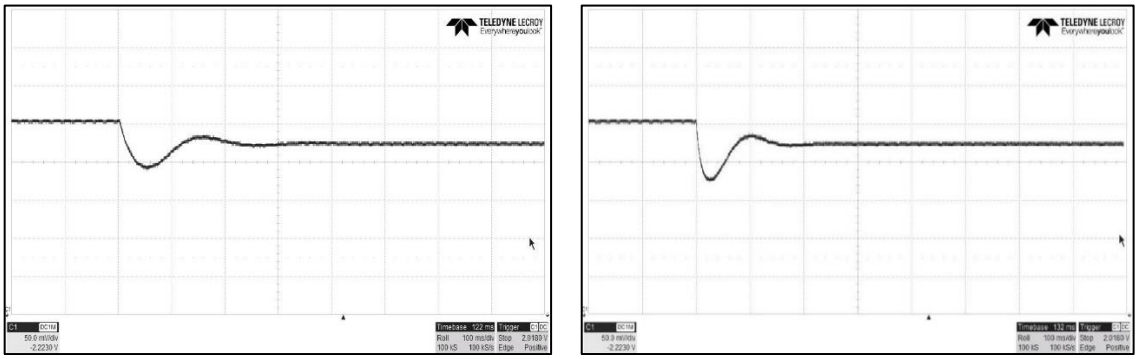
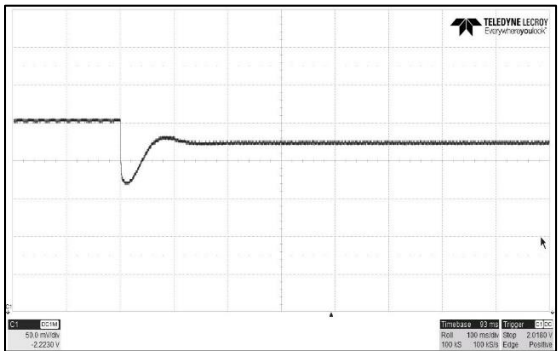


Figure 12. Bus voltage response of system with different filter cut-off frequencies

The results shows significant differences in overshoot for all cut-off frequencies level. Although the differences were quite small, system with 500 rad/s filter presents the smallest overshoot compare to the others. In addition, the settling time was also slightly faster than response of system with 50 rad/s and 100 rad/s, bearing 0.14 seconds upon reaching steady state value. The steady state stays about 1.5 percent at all filter frequencies due to the constant 60 W CPL power used. From this test, it was found that passive damping network with higher filter cut-off frequency able to give better damping performance of the DC bus system.



(a) (b)



(c)

Figure 13. Experimental output waveform for system with different filter cut-off frequencies; (a) 50 rad/s, (b) 100 rad/s (c) 500 rad/s

Table 8. Comparison of DC Bus Voltage Behaviour for Different Filter Cut-off Frequency with Passive Damping Network and Fixed Input Voltage

Cut-off Frequency (rad/s)		50	100	500
Overshoot (%)	Simulation	0.46	0.44	0.26
	Experiment	0.58	0.40	0.22
Settling Time (s)	Simulation	0.36	0.21	0.14
	Experiment	0.30	0.19	0.14
Steady State Error (%)	Simulation	1.50	1.50	1.50
	Experiment	1.50	1.48	1.48

5. Conclusion

Passive damping method was proposed in this paper to solve the instability phenomena that occurs in the DC bus. Four common damping topologies were compared and the selected topology was implemented. In designing the passive damping network, stability criteria was always concerned and Middlebrook criterion was used as guideline in the design process. Modelling, analysis and simulation was conducted to choose the best parameters for the circuit configuration and experimental hardware tests was conducted to verify the obtained simulation results. Four tests was conducted to analyse the damper network performances which are damping behaviour due to different CPL power level, CPL disconnection, effects of the combination of capacitor filter and damping capacitor, and also effects of different filter cut-off frequencies.

Analysis of overshoot, settling time and steady state error of the output waveform shows significant improvement in the system with passive damping network. This indicates that the instability occurred in the system has been reduced with the damper installation. Moreover, the damping performance was better with the usage of high damping capacitor which satisfy the

Middlebrook criterion. It was also found that the damper network able to damp out oscillation better with high cut-off filter frequency. In conclusion, the passive damper have successfully stabilized DC bus in DPS system and the conducted tests has verified the behavior of damping performance.

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