CHARACTERIZATIONS OF GALLIUM ARSENIDE NANOWIRES GROWN BY BUFFER LAYER ASSISTED MAGNETRON SPUTTERING TECHNIQUE

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Kerana tuhan untuk manusia….Thank you Allah

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ABSTRACT

Semiconductor nanowires (NWs) are among the most extensively studied nanostructure for their potential applications in nanoscale devices. Gallium arsenide (GaAs) NWs is a high-performance material with direct bandgap and high electron mobility. Despite the great potential for future nanotechnology, its widespread use when integrated with silicon (Si) has been limited by lattice mismatch, difference in thermal expansion coefficient, antiphase boundaries, relatively high production cost and inadequate ecological safety. Here, the results of growing GaAs NWs onto Si substrate via radio frequency (RF) magnetron sputtering by using a simple single buffer layer are reported. This research presents the integration of GaAs NWs on Si with various thickness of sputtered GaAs buffer layer ranging from 10 nm to 110 nm using aurum (Au) nanoparticles as a seeding catalyst via vapour-liquid-solid mechanism. The desired morphology and uniform thickness of GaAs buffer layer with Au nanoparticles were annealed at Au-GaAs eutectic temperature in order to form an eutectic liquid alloy, followed by growth process between 570 $^{\circ}$C and 690 $^{\circ}$C growth temperature. The structural and optical properties of GaAs NWs were characterized using field emission scanning electron microscopy, energy dispersive X-ray spectroscopy and atomic force microscopy as well as photoluminescence, X-ray diffraction and ultraviolet-visible spectrophotometers. The results have shown that the sufficient thickness of buffer layer of about 19.48 nm, optimized annealing temperature at 630 $^{\circ}$C and a suitable growth temperature at 630 $^{\circ}$C play important roles in producing high quality buffer layer which then lead to growth of GaAs NWs.

ABSTRAK

Semikonduktor nanowayar (NWs) adalah antara nanostruktur yang paling banyak dikaji untuk potensi aplikasi dalam peranti skala nano. Gallium arsenide (GaAs) NWs adalah bahan berprestasi tinggi dengan jurang jalur langsung dan mobiliti elektron yang tinggi. Walaupun berpotensi besar dalam teknologi nano pada masa hadapan, penggunaannya yang meluas apabila diintegrasikan dengan silikon (Si) telah dibatasi oleh ketidakpadanan kekisi, perbezaan dalam pekali pengembangan terma, sempadan antifasa, kos penghasilan yang relatifnya tinggi dan kekurangan keselamatan ekologi. Di sini, keputusan pertumbuhan GaAs NWs di atas substrat Si melalui teknik percikan magnetron frekuensi radio (RF) dengan menggunakan lapisan penimbal tunggal mudah telah dilaporkan. Kajian ini membentangkan integrasi GaAs NWs pada Si dengan pelbagai ketebalan lapisan penimbal percikan GaAs pada julat 10 nm hingga 110 nm menggunakan nano zarah aurum (Au) sebagai pemangkin pembiakan melalui mekanisma wap-cecair-pepejal. Morfologi yang dikehendaki dan ketebalan seragam lapisan penimbal GaAs dengan nano zarah Au telah disepuh lindap pada suhu eutektik Au-GaAs untuk membentuk aloi cecair eutektik, diikuti dengan proses pertumbuhan pada suhu pertumbuhan antara 570 $^{\circ}$C dan 690 $^{\circ}$C. Ciri-ciri struktur dan optik GaAs NWs telah dicirikan menggunakan mikroskop elektron pengimbas pancaran medan, mikroskop tenaga terlesap sinar-X dan mikroskopi daya atom serta spekrometer fotoluminesen, pembelauan sinar-X dan ultra-ungu nampak. Hasil penyelidikan menunjukkan bahawa ketebalan lapisan penimbal yang mencukupi pada kira - kira 19.48 nm, suhu penyepuhlindapan optimum pada 630 $^{\circ}$C dan suhu pertumbuhan yang sesuai pada 630 $^{\circ}$C memainkan peranan penting dalam menghasilkan lapisan penimbal yang berkualiti tinggi yang kemudiannya membawa kepada pertumbuhan GaAs NWs.

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2D	-	Two-dimensional
AFM	-	Atomic force microscopy
AP	-	Atmospheric pressure
CB	-	Conduction band
APBs	-	Antiphase boundaries
CVD	-	Chemical vapor deposition
DI	-	Deionized
EDS	-	Energy dispersive spectroscopy
FESEM	-	Field emission scanning electron microscope
FWHM	-	Full wide half maximum
h_c	-	Critical thickness
HF		Hydrofluoric acid
LO	-	Longitudinal optical
LP	-	Low pressure
LPE	-	Liquid phase epitaxy
LT	-	Low temperature
MBE	-	Molecular beam epitaxy
MDs	-	Misfit dislocation
MOCVD	-	Metal organic chemical vapor deposition
NWs	-	Nanowires
PECVD	-	Plasma enhanced chemical vapor deposition
PL	-	Photoluminescence
PLD	-	Pulsed laser deposition
PLL	-	Poly-L-lysine

PVD	-	Physical vapor deposition
QG	-	Quartz glass
QW	-	Quantum well
Raman	-	Raman spectroscopy
RF	-	Radio frequency
RIE	-	Reactive ion etching
RT	-	Room temperature
SEM	-	Scanning electron microscope
TO	-	Transverse optical
UV-Vis	-	Ultraviolet-visible
VB	-	Valence band
VHF	-	Very high frequency
VLS	-	Vapor-liquid-solid
XRD	-	X-ray diffraction
NIR	-	Near infrared
ATR	-	Attenuated total reflection
GI-XRD	-	Glazing incident X-ray diffraction
OP-GI	-	Out-of plane glazing incident
IP-GI	-	In-plane glazing incident
SE	-	Secondary electron
BSE	-	Back scattering electron
FEG	-	Field emission gun
RMS	-	Root-mean-square roughness
WZ	-	Wurtzite
ZB	-	Zinc blende

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CHAPTER 1

INTRODUCTION

1.1 Overview

This chapter presents the background of this study, which mainly related to the current integration of III-V group on Si and problem statement of the current research. Towards the end of this chapter, the aim and outline of the thesis will be discussed thoroughly.

1.2 Background of the Study

The key material in semiconductor nanoelectronics innovation is mostly based on Si. Some important features of Si which make it the best for various applications among other semiconductor materials are great electrical properties, high thermal conductivity, low cost and large-scale availability. However, Si has an indirect bandgap and weak optical properties. A good electronic device requires optical properties of the material with a direct band gap, high carrier mobility, high absorption coefficient, and it presents in the III-V compound semiconductor such as gallium arsenide (GaAs) [1].

In contrast to Si, GaAs has a direct band gap that enables it to emit light with high efficiency which empowers its utilization in the future of optoelectronic applications. GaAs is a semiconductor compound which is also known as III-V semiconductors and falls into some classes of the element. They are lumped together with either three or five valence electrons. Gallium is a category III element and arsenic is a category V element. Combining a category III element with a category V element delivers a covalent security with eight electrons, constructing one of a kind semiconductor. Such semiconductors have higher electron mobility than Si and beneficial at higher frequencies.

Recently, the nanowire (NW) with a one-dimensional (1D) columnar shape has increased an extraordinary attention. The diameter of the NWs is ordinarily ranged from a few nanometers to hundreds of nanometers, while its length can go up to thousand nanometers. One dimensional nanostructure has been called with a variety of names including whisker, fibers, and nanorods. Although whisker and nanorods are in general considered to be shorter than fibers and NWs, the definition is often a little arbitrary. NWs are confined for two dimensions and hence enable them to grow freely along the third dimension. If the diameter of the NWs is sufficiently small, carriers are subjected to quantum confinement. In the NWs geometry, III–V materials can show different features contrary to their thin film. Due to their small dimensions, III–V NWs have a great tolerance in strain, which can accommodate large lattice and thermal expansion coefficient mismatch when polar III–V NWs are grown on non-polar substrates. Hence, possible integration of III–V NWs on an extensive variety of substrates. During their development, most III–V NWs can take on both zinc blende (ZB) and wurtzite (WZ) crystal structure by changing the growth conditions. It is exceptionally hard to accomplish with the thin film innovation [2]-[5].

Furthermore, the NWs have an extensive surface-to-volume ratio. III-V group semiconductor nanowires which arrays of large volume-to-surface ratios are a potential material whose bandgap can be tuned for efficient transfer of solar energy to electric energy. In spite of the fact that NWs devices with promising properties have been illustrated, the III-V NWs on Si growth is extremely challenging. Due to the small dimension, novel geometry, and the special growth modes, the NWs growth is substantially more sensitive to the substrate condition and the growth parameters contrasted with its thin film. Additionally, the NWs keeps opening new entrance in fundamental research and they are an outstanding contender for integration to existing device. The semiconductor industry is always hunting down the future technique to shrink feature sizes, enhance efficiency, decrease cost, and increase speed [2].

Si is the basic material of electronic devices and almost 95% of all semiconductor devices are manufactured utilizing Si substrates. As a carrier, Si substrate is commonly used because of its good thermal conductivity, superior mechanical properties and low in cost. In contrast, GaAs has impressively higher carrier mobility which is the basis of high-speed devices. However, single-crystal GaAs substrate is expensive and difficult to integrate into the present Si-based industry. On this basis, Si substrate is more desirable in support of III-V group semiconductor nanowires growth via vapor-liquid-solid (VLS) mechanism [5].

A decade of research had performed to develop high-quality III-V layers on Si substrates, but there is still a challenge to be solved. The first challenge was the lattice mismatch between Si and GaAs, which led to the formation of crystal defects to accommodate strain in the material. Thus to reduce the density of crystalline defects, various improvements have been investigated such as post-growth thermal cycle annealing, insertion of dislocation filter layer, selective growth in trenches using Ge / GeSi buffer layers. The second challenge is the difference in coefficient of thermal expansion between Si and III-V that limits the thickness of the film before the crack appears. The third challenge is the emergence of anti-phase domains at the interface between the III-V and Si substrate. The antiphase boundaries (APBs) come from the III-IV polar material on Si non-polar materials [6].

GaAs NWs on Si challenge is to fabricate NWs with good control of dimensions and phase purity. In the nanoscale regime, small size variations can have a big impact on device performance as a whole because nanowire dimensions determine the degree of confinement. Thus, it affected the behavior of charge carriers in quantum electronic devices. It is important to control the nanowire diameter, as most device applications require a well-defined uniform diameter. In a proposed nanowire laser, a uniform diameter is critical for the performance of NWs as a resonant cavity. Phase purity is important because the crystallographic phase, whether ZB or WZ, adversely affects the bandstructure of NWs. In addition, crystallographic defects such as twin plane and stacking faults make non-radiative recombination centers that affect optoelectronic device performance [2], [3], [7].

Over the past few years, NWs of III-V compound semiconductors have become the focus of the nano-building blocks for future integrated electronic and optoelectronic devices. Direct growth of GaAs NWs on Si substrate was investigated in three ways through Au-assisted vapor-liquid-solid (VLS) growth, selective area growth, and a self-catalyzed growth [5]. Regardless of the method of growth, defects such as twin, stacking faults and phase polytypism still exist in NWs. In addition, the high thermal stability of native oxide on the surface and unintentional Si doping of GaAs NWs from Au-Si alloy droplet adversely affects the controllability of NWs direct growth on Si.

As observed from previous studies, an assembly of horizontal and vertical NWs during direct growth of GaAs NWs on Si, the high solubility of Si in Au brings down Au-Si interface energy thus contributes to Si contamination in NWs [3]. Observation using Transmission Electron Microscope demonstrates that there is a lot of stacking flaws and twins in the NWs. The effect of the annealing and growth temperature on NWs results is explored as well as the structural and optical properties of NWs. It has been found from previous research that the vertical growth of NWs and crystalline properties can basically be altered by changing growth temperatures [8].

Au has a moderate melting temperature and hence is able to form low-melting alloys [9]. Most group III and V elements have high diffusion coefficients in it. Therefore, it is quite suitable to be the catalyst for NWs growth. Moreover, Au has good resistance for oxidation and other parasitic reactions, which can simplify the growth preparation. During growth, the Au is not a fast consumption material and hence less sensitive to the changes of parameters, compared with the group-III material in the self-catalytic droplet [3]. The growth window for the Au catalysed growth, such as the growth temperature and V/III ratio, is much wider compared to other growth modes. This offers much greater freedom in controlling the NWs fabrication, such as axial or radial selectivity, crystal phase, growth direction, and growth rate [10].

In previous studies, different substrate preparation methods have been compared to obtain high-quality III-V NWs. One method is to deposit a thin layer of 1-10 nm Au on the substrate through thermal or electron beam evaporation. When annealing, the layer splits into small Au droplets whose size depends on the annealing temperature and its density relies on the thickness of the layer. This method is simple yet hard to acquire a uniform nanoparticle in the size or distribution [11]. Furthermore, Au nanoparticles can also be sourced in Au colloidal nanoparticles in solution. Each solution contains an Au monodisperse nanoparticle of a given diameter and density. Au colloidal nanoparticles carry a net negative surface charge thus Coulombic repulsion prevents agglomeration of nanoparticles in solution. Due to their net negative charges, nanoparticles do not naturally adhere with the III-V buffer layer. In this research, these colloidal nanoparticles can be deposited on the III-V buffer layer by poly-L-lysine (PLL). PLL positively charged polyelectrolyte that attracts negatively charged Au nanoparticles and diverts them to the surface of the substrate. The Au-functional PLL deposition method prevents the agglomeration of nanoparticles during deposition and reaches distribution on the substrate. The PLL functionalization of Au-colloids used routinely in this work is suitable for most device applications and ideally suited for research into the nanowire growth process and also suitable for all substrates used [12].

A gold-catalyzed vapor-liquid-solid method is extensively applied to III–V NWs growth on Si substrate. However, possible Si contamination, easy oxidations of Si, a high sensitivity of the NWs morphology to growth conditions generally restricts its controllability. In previous research, a buffer layer technique was developed by introducing the GaAs film with a designated polarity as GaAs target [13]. The most common technique used to develop a GaAs buffer layer on Si substrate is the two-steps growth. A low-temperature buffer has a smooth morphology which brings a high yield of vertical NWs, yet the NWs have a few imperfections. While high-temperature buffer has lower vertical NWs yield with rough morphology, it brings a perfect NWs quality with deficient in deformities and sharp lattice flange. The buffer layer technique can eliminate unintentional Si doping by preventing Si-Au alloy formation and by expanding the Si diffusion barrier, consequently giving greater flexibility to vertical NWs growth. The controlled properties of NWs are exceptionally encouraging for optoelectronic device applications based on GaAs NWs [14]-[16].

The key in improving the quality of the GaAs buffer layer on Si is the relaxation of the strain during the buffer layer growth process. In buffer layers of GaAs, the presence of threading dislocation or other defects generated by strain relaxation may affect the quality of the buffer layer. In addition, the thickness of the buffer layer has some relationship with surface morphology and its root-mean-square (RMS) roughness. The buffer layer thickness has proven to be an important factor in high-quality thin films in many experiments. SEM and optical measurements have shown that the best surface morphology and the lowest RMS roughness are achieved with a 20 nm buffer layer [17]. There is a significant reduction in RMS roughness during the initial stage of increasing the thickness of the buffer layer [14], [17].

On the other hand, the surface morphology of the buffer layer has a strong influence on the quality of the thin film. The optimum thickness of the buffer layer is around 20 nm, thick or thin thickness layer reduces the quality of the buffer layer [17]. The morphological surface of the buffer layer affects the buffer layer quality and the optical properties. The surface morphology of the buffer layer depends largely on the condition of the buffer layer deposition. In the process of crystal growth, the structural design of the buffer layer has two main advantages: (i) avoiding high misfit strain between the buffer layer and the top substrate and (ii) reducing the density of defects which caused by misfit strain [18]. However, understanding of the physical mechanisms in the buffer layer, the strain distribution in the buffer layer and its effect on surface roughness is required. Therefore, the optimized thickness for buffer layer can be predicted based on theoretical studies, but only a few studies have been done in the laboratory [19].

In this research, a high-quality surface and uniform thickness of the single GaAs buffer layer growth on Si substrates are expected to be achieved since a simple and easy-to-reproducible approach is very desirable to achieve III-V NWs straight on Si. Previous research indicates the possibility of growing GaAs NWs by magnetron sputtering deposition techniques. It is reported that the grown GaAs NWs was in a cone-shaped of GaAs nanowhiskers and characterized by a feature height of 300 to 10000 nm, and the transverse size is about 200 nm at the base and from 200 to 10 nm or smaller at the top. This feature shows the length of GaAs nanowhisker varies in direct proportion to the effective thickness of the deposited buffer layer and inverse proportion the horizontal nanowhisker size at the top [20]-[22]. This present investigation confirms that the buffer layer should be sufficiently thick to obtain good quality and smooth surface of GaAs buffer layers and subsequently assist to the growth of GaAs NWs. Since the initial nucleation of the NWs is extremely reliant on the quality of the surface, accomplishing buffer layers with great morphology, uniform, and sufficient thickness is vital in this research.

Most of the common NWs synthesis techniques used for the growth of GaAs NWs such are metal organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE). There are also many techniques that improve previous methods such as laser ablation. In this systematic study, GaAs NWs are grown under RF magnetron sputtering system on Si (111) via Au-catalyzed VLS mechanism. The investigation includes annealing conditions of the GaAs buffer layer and the effects of growth temperature on structural and optical properties on grown sample are studied. In order to get epitaxial layers with the desired features for optoelectronic applications, it is necessary to grow them with a sufficient level of purity and crystal quality. Features such as thickness control, crystal qualities, optical properties are associated with the growth techniques used for their preparation [23].

MOCVD, MBE and Liquid phase epitaxy (LPE) are the most successful system. However, each has significant advantages and disadvantages. The MOCVD has been widely used for the growth of epitaxial semiconductor layer with brilliant surface morphology and high crystal quality. The difficulty in a deposition of GaAs epitaxial layer by MOCVD is the consolidation of carbon and oxygen as the residual impurities [19]. These impurities in small concentrations have a very strong effect on their optical properties. This technique has become a major problem in the use of extremely toxic gases, such as arsine which is used as the precursor of the element of the V families. The LPE has become a major problem in surface thickness and morphological control.

The MBE uses an expensive growth system that refers to initial investment and operational costs. These methods are described by a relatively high cost of production and insufficient ecological safety. The need for combining Gallium and Arsenic element on Si substrates currently poses an important problem in developing alternative, economical and ecologically safe methods. The development of a low cost, large area fabrication procedure for GaAs NWs using sputtering is investigated in this research. This work gives an enhanced technique to defect-free GaAs NWs growth on Si by sputtering [20], [21], [24], [25].

1.3 Problem Statement

Over 2 decades, many attempts have been given to the growth of III–V semiconductor layers on Si. It has been discovered that III–V semiconductor layers are grown on Si substrates at high temperature which have great crystal structure but instead forming a continuous layer yet it develops into island structures due to the difference in interface energy and strain effect resulting from lattice mismatch. The layers grown at low temperature conversely, form into thin continuous layers. However, the quality of the layers is moderately low with critical carbon contamination [2]. In this work, a buffer layer must fulfil two requirements for the nucleation of NWs: it must have a good surface quality and must cover the entire surface as a continuous layer with minimum surface roughness. In previous work, NWs nucleation has been controlled in utilizing substrate etching, a baking process, and the specific annealing temperature [26]. In a defective semiconductor material, the high-temperature annealing allows atoms to move back to their lattice and restructuring materials from amorphous to crystalline structures [14], [27]-[29]. Hence, an optimization of annealing temperature needs to perform in this research in order to fulfil a desired buffer layer requirement. Optimization in annealing temperature can enhance the smooth surface and the quality of the buffer layer. This, in turn, increases chances of nucleation and NWs growth with the help of an Au catalyst.

Previous studies have shown that growth temperatures have significant effects on NWs properties. Morphological changes on GaAs NWs occur with different growth temperatures. When temperatures increase above 450 °C only radial and planar growth rates continue to increase and the axial growth rate decreases. This is due to the increasing radial growth and planar growth competes with the axial growth to diffuse adatoms [30]-[32]. Therefore, at the highest growth temperature, the nanowires are short and have severe tapering [27], [29]. Tapering is undesirable for many device applications, including lasers, where uniform diameters are required. Tapering can be reduced using low growth temperature. However, at a lower temperature of 400 °C and below, nanowires growth is kinked and irregular [28]. In addition, NWs growth can only occur within a certain temperature range for each material system. NWs nucleation failure and bad morphology may also be caused by inadequate temperature. Therefore, studies on the effect of growth temperature to the overall properties of deposited GaAs NWs grown by RF magnetron sputtering techniques should be carried out [5].

The performance of GaAs NWs devices depends critically on the presence of crystallographic defects in the NWs such as twinning planes and stacking faults [32]. A change in the crystal structure can essentially change the band structure, and consequently the optical properties of the materials [2]-[5]. Many considerable efforts have been devoted to understand and prevent the occurrence of these. Further improvements in structural and optical quality of NWs can be achieved by optimizing the quality of the buffer layer with the method of two-step growth. This method was developed by Joyce et. al in 2015 [3] by using two methods of temperature growth. This method is performed with the initial growth using high temperatures for the NWs nucleation and subsequent growth with low temperatures for NWs growth. It is possible to optimize the quality of the buffer layer and reduce the structural and optical defect in GaAs NWs [33].

1.4 Objectives

This scientific work focuses on a few main objectives:-

1) To grown GaAs NWs using a single buffer layer technique for surface roughness optimization.
2) To determine the effect of buffer layer thickness and growth temperature on the overall properties of deposited GaAs NWs.
3) To characterize the structural and optical properties of the grown GaAs NWs.

1.5 Scope of Study

In this work, a single GaAs buffer layer has been used as a mid layer between GaAs NWs and Si (111) substrate. The buffer layer thickness in the range of 10 nm to 110 nm, which could be adjusted by deposition time is used in order to investigate the influence of buffer layer thickness to the roughness of the surface morphology. Therefore, achieving the desired thickness of the buffer layer with good morphological is very important with annealing temperature range 510 °C to 630 °C will be studied in this research. The effect of the growth temperature ranged from 570 °C to 690 °C to the morphology of GaAs NWs has explored as well as the structural and optical properties of NWs. The morphology samples were characterized by using Field Emission Scanning Electron Microscopy (FESEM) at high magnification. The rough surface of the buffer layer was characterized by Atomic Force Microscopy (AFM). The characterization of structural and optical properties of GaAs NWs was investigated as a function of growth temperature using X-ray diffraction (XRD), Energy dispersive X-ray spectroscopy (EDX), UV-Vis and Photoluminescence (PL). These results set some basis for optimized development to achieve a good surface quality of GaAs buffer layer on Si substrates by RF magnetron sputtering technique.

1.6 Significances of Study

This study is essentially vital to clarify the techniques and mechanisms of GaAs NWs growth on Si by magnetron RF sputtering as one of the alternative routes to the integration of III-V. In addition, a growth temperature range from 570 °C to 690 °C with (70±5) W of RF power is set to study the effects of growth parameter on the structural and optical properties of GaAs NWs. Hence, a straightforward and practical approach to producing III-V NWs through RF sputtering systems is exceedingly anticipated.

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