Top-Down Fabrication Process of ZnO NWFETs

N.M.J. Ditshego[1,a], S.M. Sultan[2]

[1]Electrical, Computer and Telecommunications Engineering Department, CET,
Botswana International University of Science and Technology (BIUST), Private bag 16,
Palapye, Botswana

[2]School of Electrical Engineering (FKE), Universiti Teknologi Malaysia, 81310 UTM Skudai, Johor
Darul Takzim, Malaysia

Email: ditshegon@biust.ac.bw

Abstract: ZnO NWFETs were fabricated with and without Al_2O_3 passivation. This was done by developing a new recipe for depositing the thin film of ZnO. By using a high donor concentration of 1.7×10^{18} cm^{-3} for the thin film, contact resistance values were lowered (passivated device had R_{con} = 2.5×10^4 Ω; unpassivated device had R_{con} = 3.0×10^5 Ω). By depositing Zn first instead of O_2, steep subthreshold slopes were obtained. The passivated device had a subthreshold slope of 225 mV/decade and the unpassivated device had a slope of 125 mV/decade. Well-behaved electrical characteristics have been obtained and the passivated device shows field effect mobility of 10.9 cm^2/Vs and the un-passivated device shows a value of 31.4 cm^2/Vs. To verify the results, 3D simulation was also carried out which shows that the obtained values of sub-threshold slope translate into interface state number densities of -1.86×10^{13} cm^{-2} for the unpassivated device and 3.35×10^{14} cm^{-2} for the passivated device. The passivated device is suitable for biosensing applications.

Introduction

Nanowire field effect transistors (NWFETs) can be fabricated using bottom-up or top-down processes [1]. Bottom-up methods involve preparing the nanowires from molecular precursors [1]. The fabrication process has two main approaches: vapour-liquid-solid (VLS) and laser ablation VLS [1]. Both techniques utilized catalyst nanoparticles that are uniformly dispersed on a substrate and gases are flowed over them [2]. The nanowires grow randomly over the substrate and the size is determined by the size of the catalyst nanoparticles [2–4]. The method produces single crystalline nanowires (NWs) having high quality electrical characteristics [2]. Although bottom-up devices have better electrical characteristics; controlling their orientation, dimension and addressability can be challenging [2–4]. They are also limited by high temperatures during the synthesis process which are typically in the 800 – 1000 °C range [1]. Lower fabrication temperatures have been reported but most nanowires with excellent electrical characteristics are still made at these high temperatures. NWFETs fabricated with bottom-up approaches have been reported to exhibit high values of field effect mobility > 2000 cm^2/Vs [2–4].

Top-down fabrication technology starts with bulk material and uses conventional microelectronics technology to pattern the bulk material into the desired geometry and sizes [1]. This is done through a variety of techniques (such as UV photolithography, e-beam lithography, reactive ion etch, etc) in order to cut, shape, pattern and etch the material [2–4]. These techniques tend to produce highly uniform and well-aligned devices [2]. Their pre-determined orientation and position on the substrate enable the nanowires to be configured into functional devices such as biosensors [2]. This subsequently paves the way for mass production. Whereas the bottom-up tends to produce higher mobility > 2000 cm^2/Vs [2–4], these top-down nanowire devices tend to suffer from a lower field effect mobility, typically < 50 cm^2/Vs [5, 6].

This paper aims to improve the top-down fabricated ZnO NWFET developed using spacer technique [4, 6–14]. The fabricated devices are known to be limited by the contact resistance and

interface state defects, therefore, in this work these limitations will be addressed by altering the deposition recipe of the ZnO layer. In addition, a technology for ZnO surface passivation is developed to prepare the ZnO NWFET towards biosensing applications. The paper shows novelty by being the first to show how ZnO devices can be converted from enhancement to depletion mode via passivation. No research has ever shown this before for ZnO devices. Finally, 3-D simulations is carried out to verify that the devices have indeed been optimized.
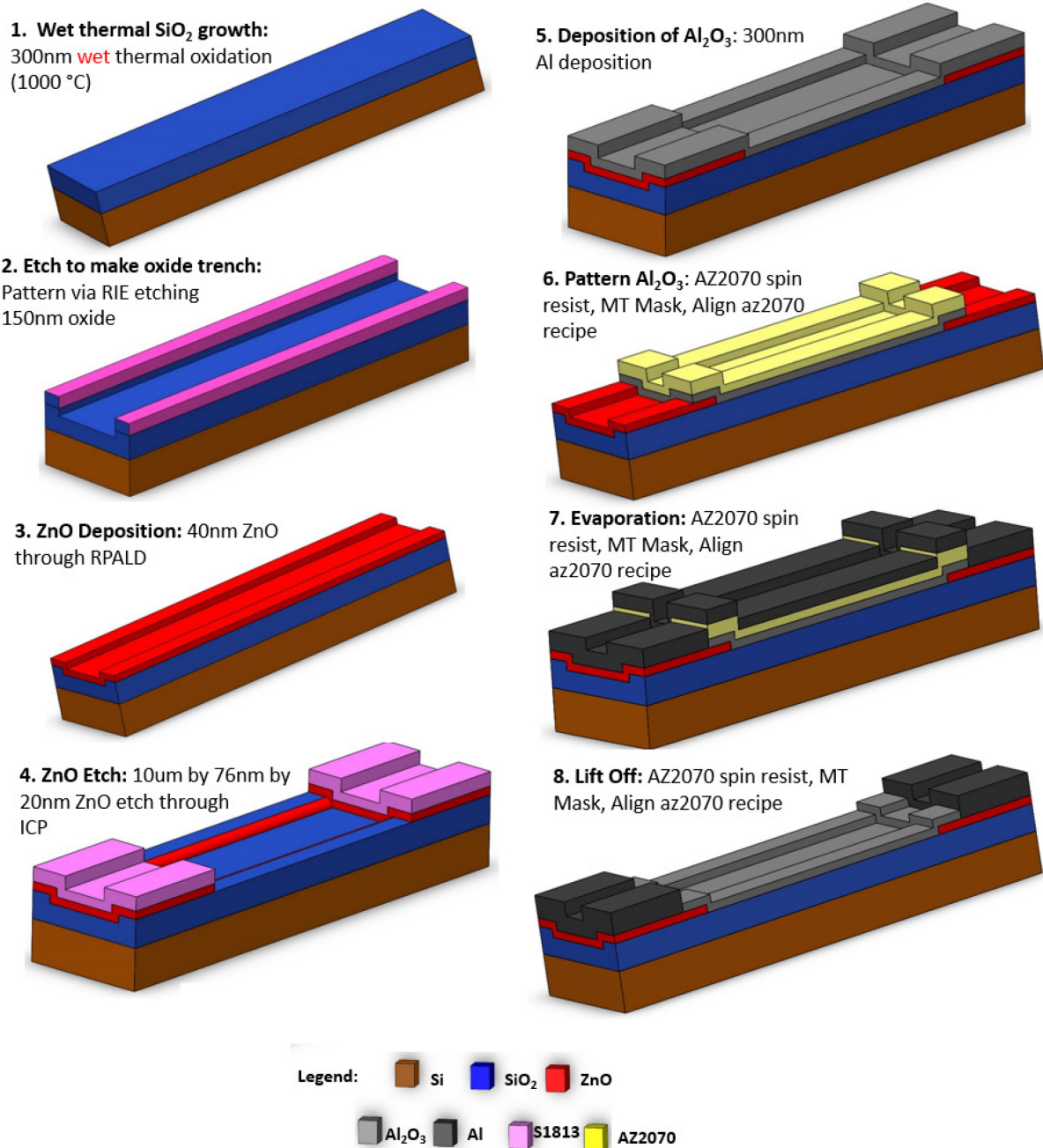
1. Wet thermal SiO$_2$ growth:
300nm wet thermal oxidation (1000 °C)

2. Etch to make oxide trench:
Pattern via RIE etching 150nm oxide

3. ZnO Deposition: 40nm ZnO through RPALD

4. ZnO Etch: 10um by 76nm by 20nm ZnO etch through ICP

5. Deposition of Al$_2$O$_3$: 300nm Al deposition

6. Pattern Al$_2$O$_3$: AZ2070 spin resist, MT Mask, Align az2070 recipe

7. Evaporation: AZ2070 spin resist, MT Mask, Align az2070 recipe

8. Lift Off: AZ2070 spin resist, MT Mask, Align az2070 recipe

Legend: Si   SiO$_2$ ZnO   Al$_2$O$_3$ Al   S1813   AZ2070

Fig. 1: The fabrication process of passivated and unpassivated ZnO NWFETs (1) SiO$_2$ insulator grown through wet thermal oxidation having a thickness of 300nm. (2) RIE anisotropic etch to make a 120 nm trench on the oxide layer. (3) a 76 nm ZnO deposition through RPALD. (4) Anisotropic ICP etch to make nanowires having dimensions of 10 μm x 120 nm x 20 nm. After this step Al metal is deposited to make unpassivated devices. To make passivated devices, Al is not deposited but Al$_2$O$_3$ at step 5 through thermal ALD having a thickness of 18 nm. The Al$_2$O$_3$ passivates the nanowire channel. (6) Patterning and ICP etch of the Al$_2$O$_3$. (7) Evaporation of Al metal using the thermal evaporator tool. (8) Removal of unwanted Al through lift-off allowing for patterned metal to be the source and drain.

Device Fabrication

The fabrication process for the bottom gated ZnO NWFET is outlined in Fig. 1. The process starts with a cleaning procedures of a 150 mm diameter of a p-type Si wafer. The wafer was cleaned in fuming nitric acid (FNA) for 10 minutes; then in 'RCA1 and RCA2' for 10 minutes each. RCA1 is a $H_2O:NH_4OH:H_2O_2$ solution that chemically attacks organic impurities while RCA2 is a $H2O:HCl:H2O2$ solution that attacks and removes metal impurities. RCA cleaning is important to ensure a high quality gate oxide can be grown on the wafer. The wafer afterwards is dipped in hydrofluoric acid (HF) for 30 seconds.

After the cleaning process, a 300 nm of SiO_2 was grown on the wafer using thermal oxidation. The oxide was patterned by photolithography and etched in Reactive Ion Etch (RIE) to form the spacer templates. SiO_2 trenches were produced with a depth of 120 nm and a width of 10 μm. The RIE trench process utilizes anisotropic etch at a temperature of 20 °C, RF power of 200 W, pressure of 20mTorr, Ar gas flow of 38 sccm and CHF_3 gas flow of 12 sccm. A ZnO layer was then deposited on the SiO_2 trenches by remote plasma atomic layer deposition (RPALD) using the Oxford Instrument FlexAL system. The deposition process was conducted for 900 cycles. Each cycle consists of a 50 ms diethyl zinc (DEZ) precursor dose time, a 4 s Ar purge, a 2.65 s oxygen plasma, and a final 4s Ar purge. The deposition temperature was at 190 °C and the RF power and pressure were set at 100 W and 15 mTorr, respectively. RPALD can produce high quality films within temperature range of 120°C to 210°C depending on other parameters such as RF power and pressure. The ellipsometer measurement of the deposited ZnO layer thickness was 76 nm. The ZnO layer was later etched in Inductively Coupled Plasma (ICP) etch to form the nanowires.

Anisotropic inductively coupled plasma (ICP) etcher and CHF_3 gas chemistry was used to etch and pattern the ZnO layer. This was done at a temperature and pressure of 20 °C and 10 mTorr, respectively. CHF_3 gas was kept at a flow rate of 30 sccm while RF and ICP generator powers are kept at 100 W and 2000 W, respectively.

Fig. 2 shows a cross-sectional SEM of the fabricated ZnO nanowire. The ZnO thickness at the edge of the spacer is approximately twice the thickness to the flat surface, hence after the ICP etch, ZnO at the spacer leaves a thin nanowire having a height of 120 nm which was equivalent to the height of the SiO_2 trench. ZnO layer at the non-spacer regions were fully etched out in ICP etch. The nanowires were produced on sidewall of the SiO_2 trenches. The advantage of this method is the maskless approach and the nanowires are self-aligned to the source and drain. The thickness of the nanowires achieved in this process is 20 nm. The etching process is not optimized and the thickness tends to vary form ~5 nm to ~30 nm across a single chip.
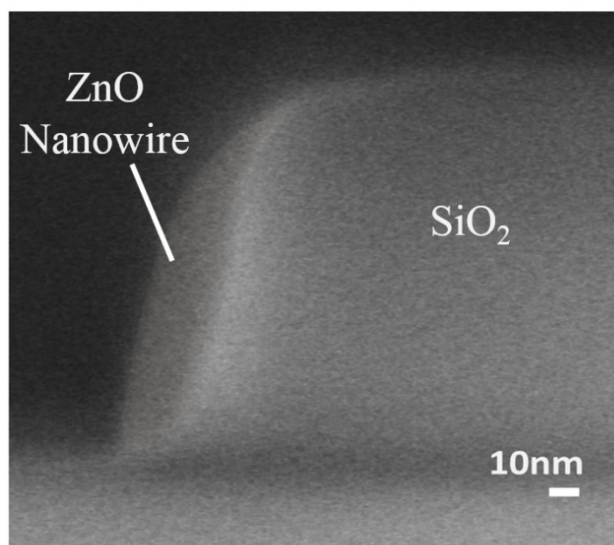

Fig. 2: Cross-sectional SEM image of fabricated high-doped ZnO nanowire.

The thermal ALD tool was used to deposit Al_2O_3 passivation layer of 18 nm thick over the ZnO nanowires at temperature of 200 $^{\circ}$C. The process had 163 cycles using trimethyl-aluminium (TMA) precursor for the aluminium source and distilled ionised water for oxidation. The pressure was kept at 1.0 torr while the TMA and H_2O have a dose of 0.030 sec and 0.075 sec, respectively. The aluminium oxide was dry etched from the contact widows using the ICP tool at a temperature and pressure of 20 $^{\circ}$C and 10 mtorr. The gases used for etching were O_2 and C_3F_8 having flow rates of 50 sccm and 25 sccm.

The wafer was designed with different NWFETs: all use a global back-gate. The back-gated NWFETs have 2, 4, and 16 parallel nanowires of 2, 10, and 20 µm channel length, respectively. It was also designed such that each chip had alongside biosensor devices with 100 nanowires. The NWFETs were fabricated using a three mask process: mask NW is used to create trenches that define where the nanowires will be located on the SiO_2, mask DP was used to define the ZnO pads that make up the source and drain and mask MT defines the aluminium electrodes.

Fig. 3 shows a finished device fabricated using the three mask process (mask NW, mask DP and mask MT). The device has two nanowires in parallel. The image was derived using an optical microscope. It shows that the photolithography produced well aligned devices. Fig. 4 shows an optical micrograph of two completed wafers. A *'6'* inch wafer contains 66 identical chips, so that it can be measured at different devices across the wafer
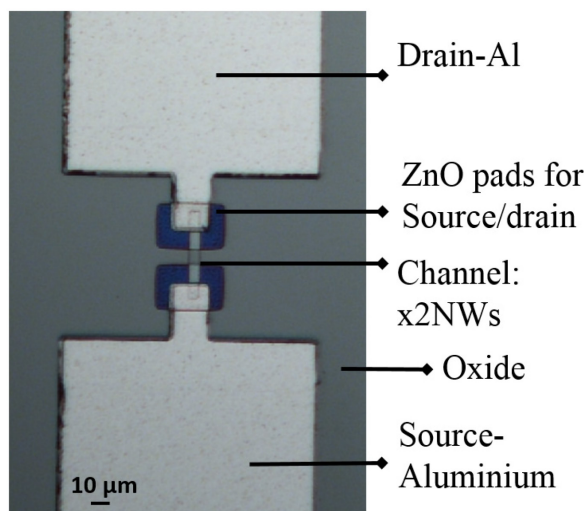

Fig. 3: Optical microscope image of a completed device fabricated using a three mask process (mask NW, mask DP and mask MT). The device has two nanowires in parallel
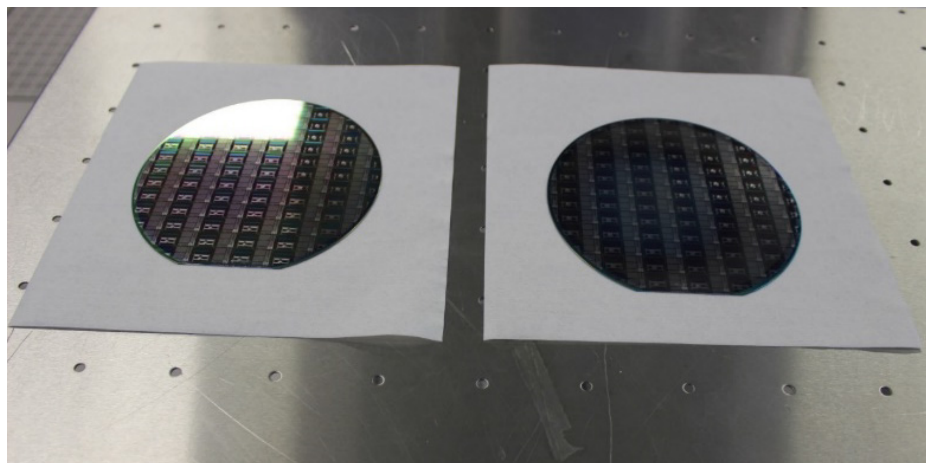

Fig. 4: Optical micrograph showing two completed wafers of the nanowire devices. Each wafer contains 66 identical chips.

The electrical I-V characterization of the ZnO NWFETs was performed using an Agilent Technologies B1500A semiconductor parametric analyser. Hall measurements were made on the ZnO layer and the results were compared with results reported by other researchers [4, 6–14].

Process Optimisation

This work aims to improve an existing process developed by S. M. Sultan et al., [6] on the remote plasma atomic layer deposition (RPALD) process. All other steps were kept relatively the same. RPALD is capable of producing highly conformal and quality films [8]. The process is cyclic and is based on the number of reactants. For ZnO films, the cycle depends on two reactants: metallisation and oxidation. Metallisation uses diethyl zinc (DEZ) as the zinc (Zn) metal precursor. Purge and pump steps are used to separate the execution of the reactants and to remove any by-products. Before deposition: the wafer (substrate) is pre-heated to a temperature used for deposition (190 °C) and it is also cleaned with an O_2 plasma to remove any polymer layer. During the metallisation step, the DEZ (Zn $(C_2H_5)_2$) is absorbed onto the surface of the wafer, then on another step, O_2 is delivered to react with the absorbed DEZ [2–10].

The existing process [6] is as follows: 333 cycles of an initial 4.0 s Ar purge, a 4.0 s oxygen plasma, a 1.0 s dose exposure to diethyl zinc (DEZ) and a final 2.0 s Ar purge. This was carried out at a temperature of 190 °C with RF power of 100 W and pressure of 15 mtorr. The ZnO layer achieved was 36 nm. The ZnO layer produced had a sheet resistance of 19.9 x 10^6 Ω/sq and a donor concentration of 2.0 x 10^{16} cm^{-3}. To improve the ZnO film properties, changes were made to the number of cycles, the order of the reactants, the oxygen plasma dose time and the DEZ dose time. These changes affected the doping, contact resistance and interface state charge, as will be discussed in the next section.

Contact Resistance Reduction

From the device fabricated by S. M. Sultan et al., [6] the Al/ZnO contact resistance, R_{con} measured was 1.8 x 10^8 Ω, and a sheet resistance of 2.09 x 10^7 Ω/sq was obtained. Consequently, the contacts between Aluminium and ZnO exhibited Schottky behaviour [6]. In order to reduce the contact resistance, most researchers [5–15] use annealing to improve the film quality and the contacts, with temperatures > 500 °C. The problem with aluminium is that it has a low melting temperature of 660 °C and is also a p-type dopant that compensates the natural n-type doping of the ZnO layer. The highest temperature that can be used for annealing Aluminium is around 400 °C. Therefore, researchers [4, 6–14] anneal Al contacts at temperatures between 300 °C and 400 °C [6]. However, the contact resistance did not improve significantly hence there is a need for an alternative technique to be used which is to use higher doping on the ZnO layer.

Higher doping was used to reduce contact resistance and sheet resistance. This was achieved by developing a new recipe for the RPALD. Three main parameters were altered: film thickness, DEZ dose time and O_2 dose time. DEZ dose time was reduced from a value of 1.0 s to a value of 50 ms, while O_2 dose time was reduced from 4.0 s to 2.65 s. Researchers [1–20] have shown that doping concentration in ZnO depends on oxygen defects (oxygen interstitials (O_i), oxygen antisite defects (O_{Zn}), and oxygen vacancies (V_o)). By reducing the DEZ dose time from 1.0 s to 50 ms, it caused the O content to be much higher than the Zn content which increased the doping concentration. This means oxygen interstitials O_i and oxygen antisite defects O_{Zn} have more effect on the doping concentration than oxygen vacancies V_o.

Interface States Charge

From the simulation study, it was found the device fabricated by S. M. Sultan et al., [6] had high interface state charge density that needed to be reduced [6]. Normally interface state charge is reduced by annealing and wet cleaning [5–16] process. A high temperature annealing cannot be

used to improve the film properties as aluminium compensates the natural n-type doping of the ZnO layer. In addition, this work follows the same cleaning procedure as outlined [6].

To reduce the interface state charge, the ZnO deposition recipe was modified. Instead of flowing O_2 first into the chamber, DEZ was flowed first. An O_2 plasma tends to damage the SiO_2 surface, thereby increasing the amount of interface state charge. The deposition of a zinc layer first provides some protection against surface damage from the O_2 plasma.

Passivation

An unpassivated device cannot be used as a biosensor because the ZnO NW channel can be etched by the bioanalytic solutions [18]. Therefore an insulating layer is needed on top of the ZnO layer. The device has a SiO_2 layer beneath the ZnO. However, for the upper surface passivation layer, Al_2O_3 is used as an alternative to SiO_2. This is because it can be deposited at a lower temperature [16, 17]. Also, its dielectric constant is between 9.0 and 10.1 which is higher compared to SiO_2 in which the dielectric constant is only 3.9. High dielectric constant is desired and forms good diffusion barriers between the channel and the bioanalytes which makes it more sensitive than SiO_2. This means that the physical thickness of the gate dielectric (Al_2O_3) can be reduced more than SiO_2 without losing sensitivity to charge and with no adverse leakage currents [9–20].

Results

The ZnO layer produced from the optimized technique was characterized in 4-point probe Hall measurement. The ZnO layers had a sheet resistance of 1.1×10^4 Ω/sq which is 2 order magnitude lower than reported [6]. The donor concentration was measured to be at 1.7×10^{18} cm^{-3}, which is higher by 2 order of magnitude than reported [6]. Fig. 5 shows the results of thickness and uniformity measurements for the thermally grown SiO_2 and the RPALD deposited ZnO. The SiO_2 has an average thickness of 292 nm and uniformity of 1.21 %. The ZnO has an average thickness of 76 nm and a uniformity of 2.85 %.
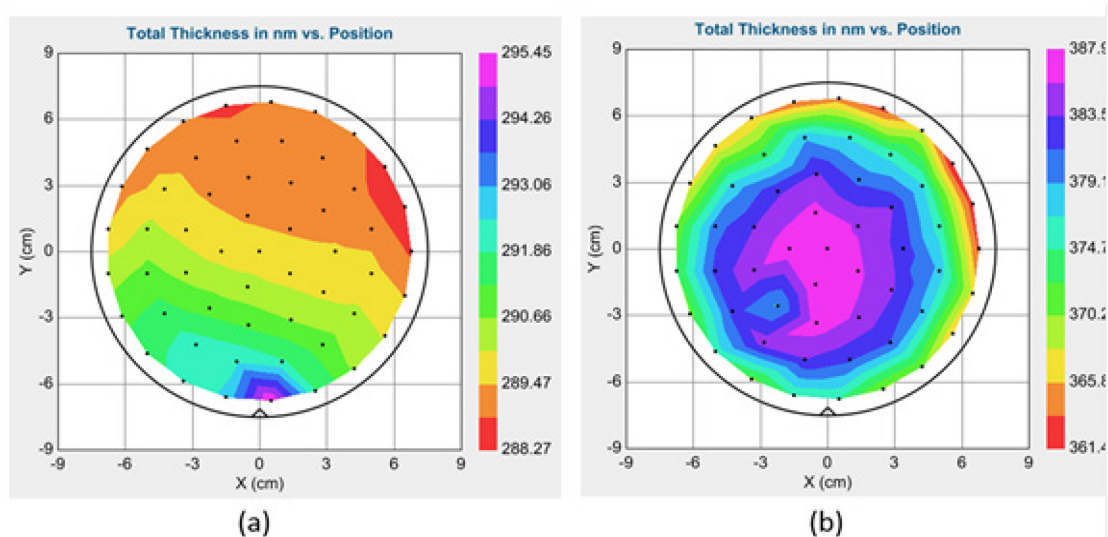

Fig. 5: Ellipsometry measurements showing the thickness uniformity of the thermal SiO2 and the RPALD-ZnO layers (a) SiO2 uniformity (b) ZnO film uniformity.

To give an indication of device uniformity, Fig. 6 shows $I_{DS}V_{DS}$ characteristics for the same type of NWFET device measured on five different chips. The chips were derived from a single wafer and only devices with a 100 nanowires in parallel were measured. Well behaved output characteristics are obtained with transistor operation up to 40 V and above. The uniformity of the transistor characteristics was assessed by measuring the drain current at a drain voltage of 40 V with a standard percentage deviation of < 23 %. All devices across the wafer gave well behaved transistor characteristics.
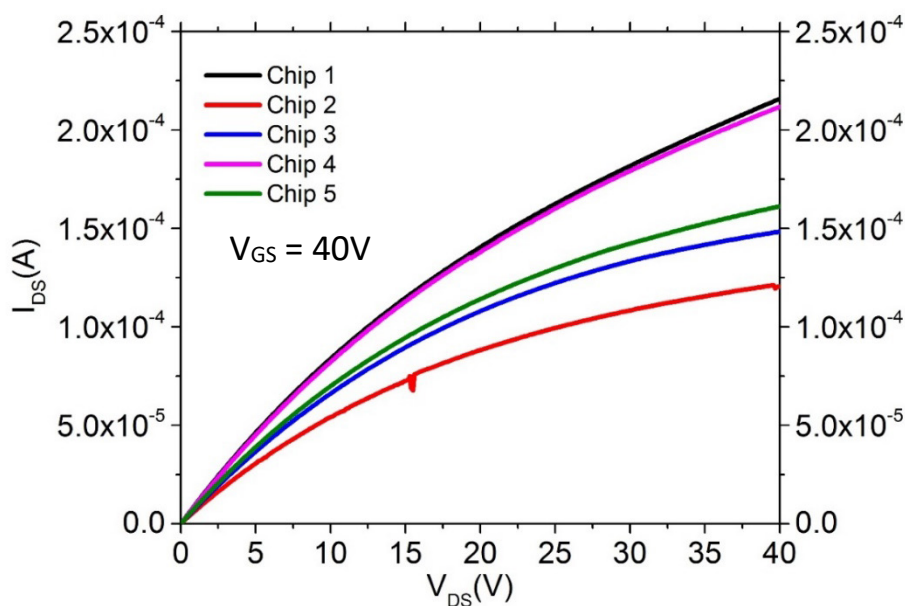
Fig. 6: $I_{DS}V_{DS}$ characteristics for the same type of ZnO NWFET device measured on different chips at V_{GS} at 40 V. The NWFET has 100 parallel nanowires and a channel length of L = 20 µm.

Un-Passivated NWFET Device

Fig. 7 shows typical un-passivated ZnO NWFET characteristics for devices measured in air and in dark. The device has two nanowires in parallel and a channel length of 8.6 µm. The NWFET is n-type with a donor concentration of 1.7 x 10^{18} cm^{-3} and operates in enhancement mode with a positive threshold voltage of 6.5 V. The device was expected to be depletion mode operation because it is intrinsically n-type with high doping concentration. However, the I-V characteristics show enhancement mode behaviour. This can be due to surface charges accumulated on the surface of the ZnO nanowires.

The output characteristic in Fig. 7 (a) shows a well-defined linear region at low bias, clear pinch-off and excellent saturation at high bias. The sub-threshold characteristic in Fig. 7 (b) shows an excellent sub-threshold slope of 125 mV/decade and a threshold voltage of 6.5 V. These characteristics are close to ideal especially the subthreshold slope which is close to the ideal value of 60 mV/decade. A threshold voltage of 6.5 V was obtained by extrapolating the linear I_{DS}/V_{GS} characteristic in Fig. 7 (b). The theoretical threshold voltage for the device was also calculated and found to be 9.8 V. The equation assumed that surface potential $\emptyset_{SBB} = \emptyset_B/2$ and that interface state charge (Q_{IT}) had more effect than the fixed charge (Q_f). Q_{IT} is derived from the subthreshold slope equation. Surface potential ($\emptyset_{SBB}$) is also known as surface barrier height whereas $\emptyset_B$ stands for surface band bending.
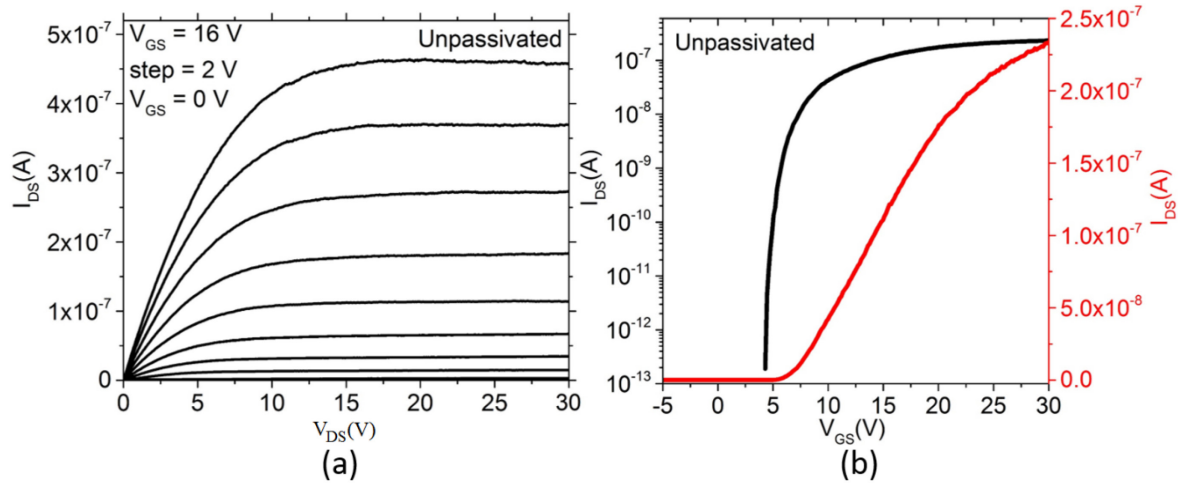
Fig. 7: Electrical characteristics of an unpassivated ZnO NWFET (a) $I_{DS}V_{DS}$ characteristic with a V_{GS} drive from 0 V to 16 V (b) $I_{DS}V_{GS}$ characteristics with V_{DS} = 1.0 V. The NWFET has two parallel nanowires and a channel length of L = 8.6 µm.
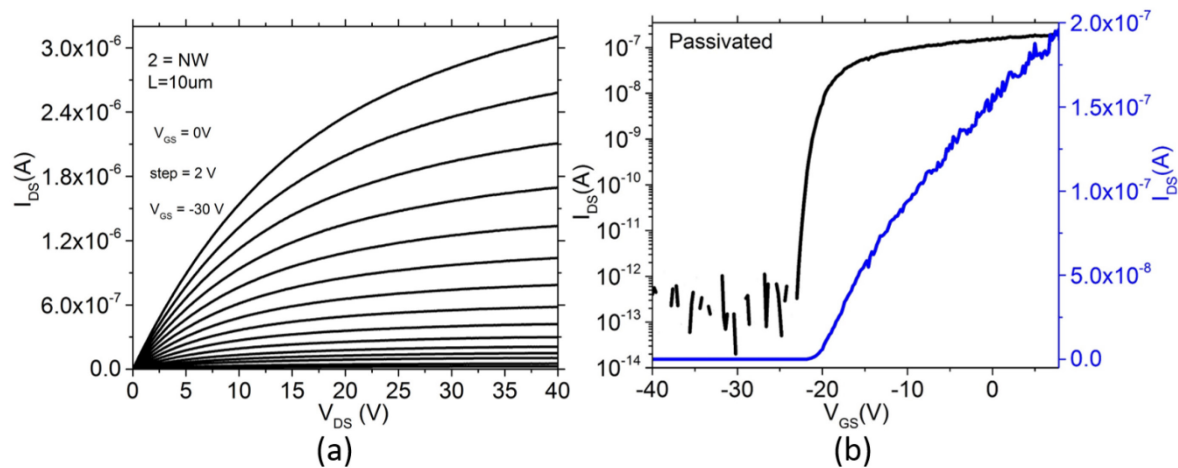

Fig. 8: Electrical characteristics of a passivated ZnO NWFET (a) $I_{DS}V_{DS}$ characteristic with a V_{GS} drive from -30 V to 0 V (b) $I_{DS}V_{GS}$ characteristic with V_{DS} = 1.0 V. The NWFET has two parallel nanowires and a channel length of L = 8.6 µm.

Passivated NWFET Device

Fig. 8 shows typical passivated ZnO NWFET electrical characteristics measured in air and darkness. Darkness is used because the device is sensitive to light. This is the same type of device as the un-passivated one, hence, it has two nanowires in parallel and a channel length of 8.6 µm. The NWFET is n-type with a donor concentration of 1.7 x 10^{18} cm^{-3} and has a negative threshold voltage of -20.1 V. The device therefore shows depletion mode operation. The output characteristic in Fig. 8 (a) shows a well-defined linear region at low bias, but pinch-off and saturation regions are not as well-defined at high currents as for the un-passivated device. Fig. 8 (b) shows a sub-threshold slope of 225 mV/decade, an off current of around 1.0 x 10^{-13} A.

Fig. 9 compares the un-passivated and passivated devices. These results shows novelty by being the first to show how ZnO devices can be being converted from enhancement to depletion mode via passivation. The results show a threshold voltage shift of 26.6 V. All devices were measured in air and in darkn with V_{DS} = 1.0 V. The passivated and un-passivated devices have comparable currents of 0.29 x 10^{-6} A and 0.28 x 10^{-6} A, respectively at V_{GS} = 40 V. These results suggest that contact resistance is lower in the passivated and un-passivated devices compared to results reported [6]. This is due to the higher doping concentration in the ZnO layer obtained in the current work. The subthreshold slope is changed from 125 mV/decade for the un-passivated device to 225 mV/decade for the passivated device, which are both better than the value of 1500 mV/decade reported [6]. The

passivated device has a maximum peak transconductance, g_m of 5.2 x 10^{-9} S compared with 1.5 x 10^{-8} S for the un-passivated device. However, device [6] obtained from the previous process has a maximum g_m of 1.0 x 10^{-8} S [6]. Values of field effect mobility were calculated from g_m and found to be 10.9 cm^2/Vs, 31.4 cm^2/Vs and 10.0 cm^2/Vs obtained for passivated, un-passivated and device from literature [6], respectively.
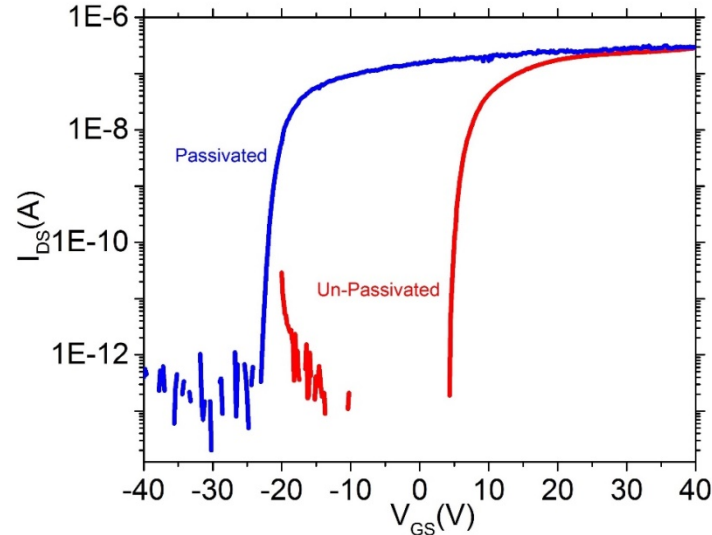

Fig. 9: Comparison of passivated and un-passivated ZnO NWFETs. These are $I_{DS}V_{GS}$ characteristics with $V_{DS} = 1.0$ V.

Discussion

Contact resistance reduction

The Transmission line method (TLM) was used to extract values of contact resistance and sheet resistance. The passivated device has a contact resistance R_{con} of 2.5 x 10^4 Ω, and a sheet resistance of 1.1 x 10^4 Ω/sq. Meanwhile, the un-passivated device has a contact resistance R_{con} of 3.0 x 10^5 Ω, and a sheet resistance of 2.8 x 10^5 Ω/sq. The two results are significantly better than those reported in literature [4, 6–14].

The above results have shown that the new RPALD process has led to lower values of contact resistance in both unpassivated and passivated devices. This has been achieved by increasing the doping concentration in the deposited ZnO layer from 2.0 x 10^{16} cm^{-3} in the previous process [6] to 1.7 x 10^{18} cm^{-3} in an unpassivated ZnO layer. The literature device [6] exhibited Schottky-diode contacts as can be seen in Fig.10 from the slow turn-on of the transistor at low drain bias. In contrast the results in Fig 7 (a) and Fig. 8 (a) show perfectly linear characteristics at low drain bias, indicating that the contacts are ohmic. These lower values of contact resistance have led to increased values of drain current, as can be seen in Fig.9.
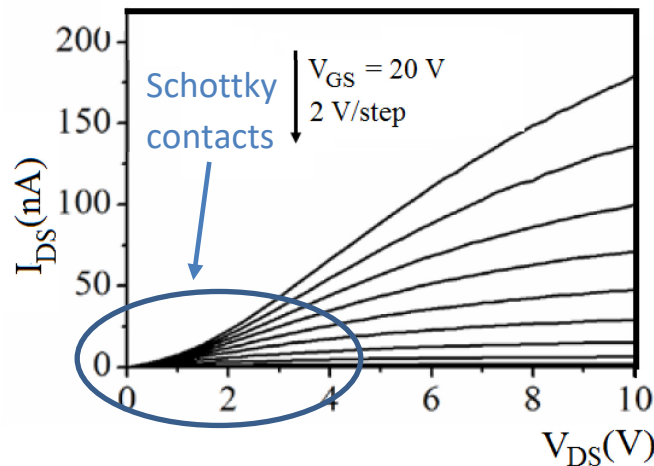
Fig. 10: Schottky-diode contacts characteristics of literature device [6].

Interface states charge

The new RPALD process has also led to lower values of interface state density, as can be seen from the improved values of sub-threshold slope. This was achieved by starting the ZnO deposition process with a zinc dose step instead of the oxygen dose step reported [6]. Values of interface state density will be estimated from device simulations later in this paper.

A passivation process has been successfully developed using atomic layer deposited aluminium oxide. The passivated devices show well behaved transistor characteristics. However, the threshold voltage is much lower (-20.1 V) compared with unpassivated device (6.5 V). Thus at zero bias, the unpassivated transistor is off (enhancement mode), while the passivated transistor is on (depletion mode). This suggests that the unpassivated device has much more negative fixed charge on the ZnO surface that the passivated device has on the Al_2O_3 surface. Alternatively, the Al_2O_3 layer may contain significant positive charge that compensates the negative surface charge. Furthermore, the passivated devices exhibit a higher subthreshold slope than the unpassivated devices (225 mV/decade compared with 125 mV/decade). This suggests that there are a significant number of interface states at the ZnO/Al_2O_3 interface, which might be due to the use of an acetone/IPA clean prior to Al_2O_3 deposition.

Comparing the results obtained with various ZnO NWFETs

Fig. 11 compares fourteen (14) different ZnO NWFETs fabricated by different authors using a variety of methods [6, 21–33]. The graph is plotted with field effect mobility against the subthreshold slope which are two important device parameters that determine ZnO NWFET performance. The nanowires were fabricated using top-down and bottom-up (self-assembled) processes. Self-assembled processes tend to display very high field effect mobility which is normally above 200 cm^2/Vs; whereas the top-down have lower mobility values. Most of the top-down fabricated devices have mobility < 1.0 cm^2/Vs with around three papers giving a mobility > 10.0 cm^2/Vs. As stated before, values of field effect mobility obtained are 31.4 cm^2/Vs and 10.0 cm^2/Vs for passivated, un-passivated and device, respectively. The figure below shows were such mobility lays. The difference in the mobility may be due to the fact that self-assembled nanowires are single-crystal, whereas top-down nanowires are polycrystalline. Nonetheless, top-down techniques are desirable as they currently pave way for mass production and will be pursued in this research investigation.
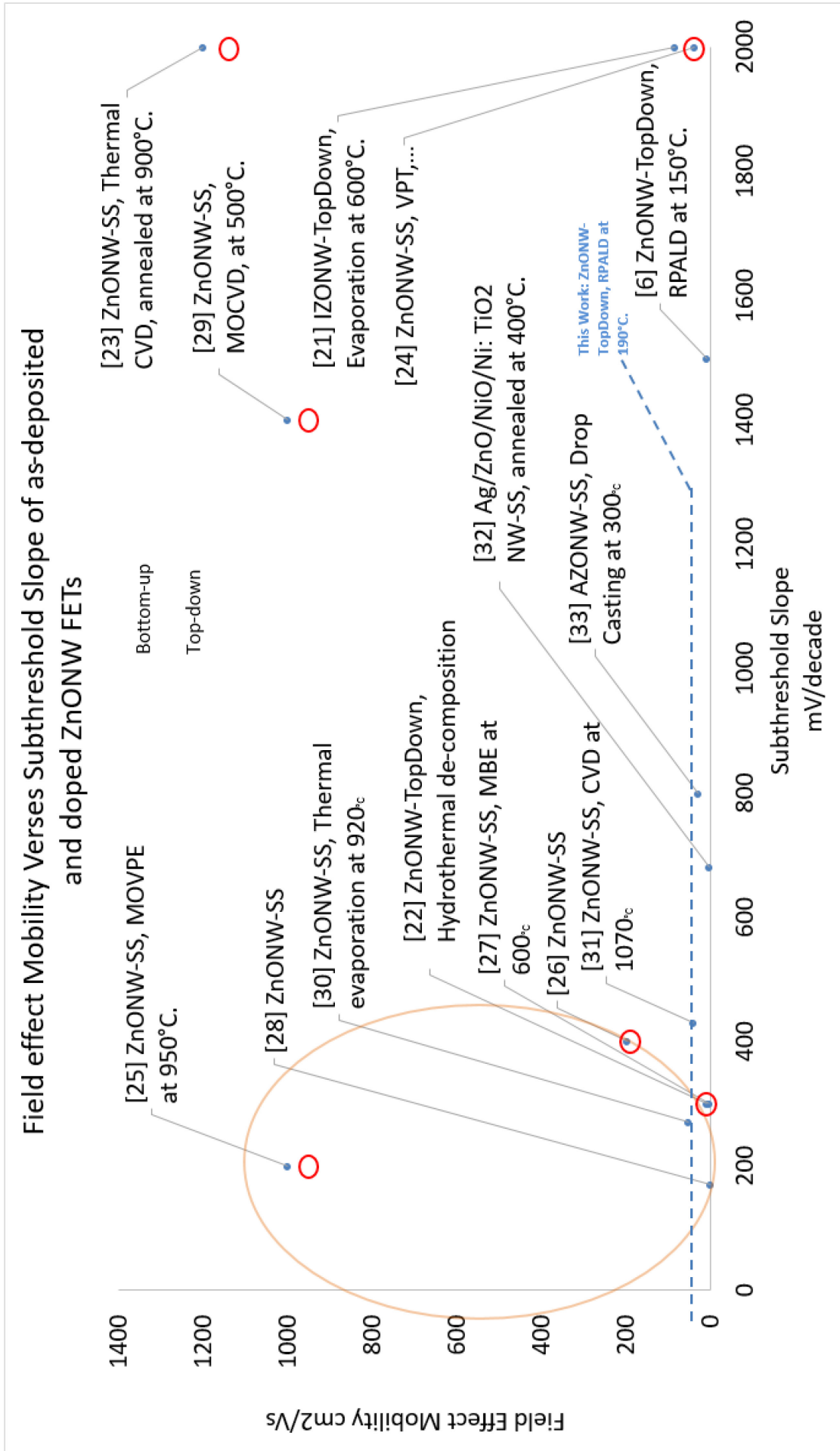
Fig. 11: Comparing the results obtained with various ZnO NWFETs looking at field effect mobility verses subthreshold slope of as-deposited and doped ZnO films.

3D TCAD Simulation: comparing experiment with 3D simulation

The electrical results obtained for the two devices (passivated and unpassivated) were then interpreted using 3D simulations. Two Silvaco products were used: Devedit and Atlas. The 3D device structures were developed using Devedit, whereas electrical characteristics and bias conditions were simulated through Atlas. The research investigation uses Devedit over Athena software because Devedit has a more advanced mesh definition which allows for greater accurate and precise output results. Devedit also allows for direct 3D interfacing with Atlas whereas it is impossible with the Athena software. There are several Atlas numerical methods that can be used for calculating device output results and these include: gummel, newton, direct and block. Block cannot be used in 3D simulation and gummel is very slow to utilize. Therefore, the numerical methods used throughout the simulation are newton and direct. The aim of the 3D simulation is to show that the devices have been optimised, therefore have less interface state charge, fixed charge and contact resistance than other devices reported [4, 6–14]. Fitting of the experimental results using simulations always starts with default parameters as given in Table 1.

Table 1: Parameters and their values for passivated and unpassivated devices for TCAD simulation.

3D Simulation			
Parameter	**Default Simulation values**	**Passivated Device**	**Unpassivated Device**
N_{TA}	4.0×10^{17} cm^{-3}	1.55×10^{18} cm^{-3}	9.1×10^{17} cm^{-3}
N_{GA}	3.0×10^{16} cm^{-3}	5.79×10^{16} cm^{-3}	3.79×10^{16} cm^{-3}
E_{GA}	1.7 eV	1.7 eV	1.7 eV
W_{GA}	0.21 eV	0.21 eV	0.21 eV
W_{TA}	0.14 eV	0.14 eV	0.14 eV
E_C	3.4 eV	3.4 eV	3.4 eV
Q_f	3.0×10^{10} cm^{-2}	7.31×10^{12} cm^{-2}	-3.0×10^{11} cm^{-2}
R_{con}	10 Ω	3.0×10^{6} Ω	3.0×10^{5} Ω

Fig.12 shows the default 3D simulation of a ZnO NWFET in comparison with the measured characteristics for passivated and unpassivated devices. Default 3D simulations were executed using the default parameter values from Table 1. The default simulation gives a higher current at high gate bias and a steeper sub-threshold slope. The simulated value of sub-threshold slope is 100 mV/decade, compared with the measured value of 225 mV/decade for the passivated device and 125 mV/decade for the unpassivated device. The similar value of sub-threshold slope for the simulated and measured unpassivated device is encouraging because it means that the unpassivated device has a small interface state charge which is a huge improvement over the devices [4, 6–14].
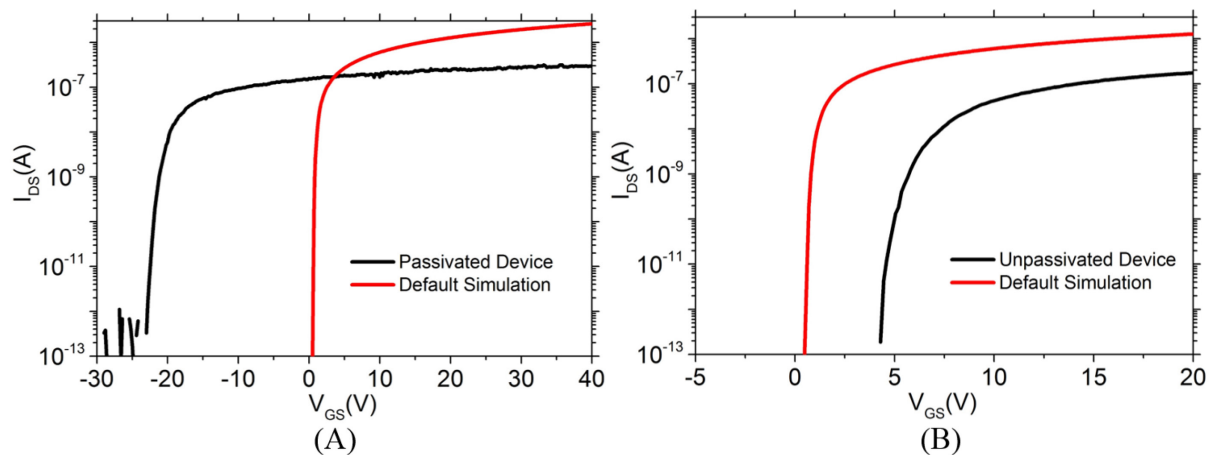

Fig.12: Default 3D simulation of ZnO NWFET compared with (a) passivated and (b) unpassivated devices. V_{DS} is fixed at 1.0 V.

Next, the fixed charge parameter (Q_f) in the simulation was altered to fit the simulation results with experiment. As shown in Fig.13, a positive fixed charge number of $+7.31 \times 10^{12}$ cm^{-2} is needed to fit the characteristic of the passivated device and a negative fixed charge number of -3.0×10^{11} cm^{-2} to fit the characteristic of the unpassivated device.

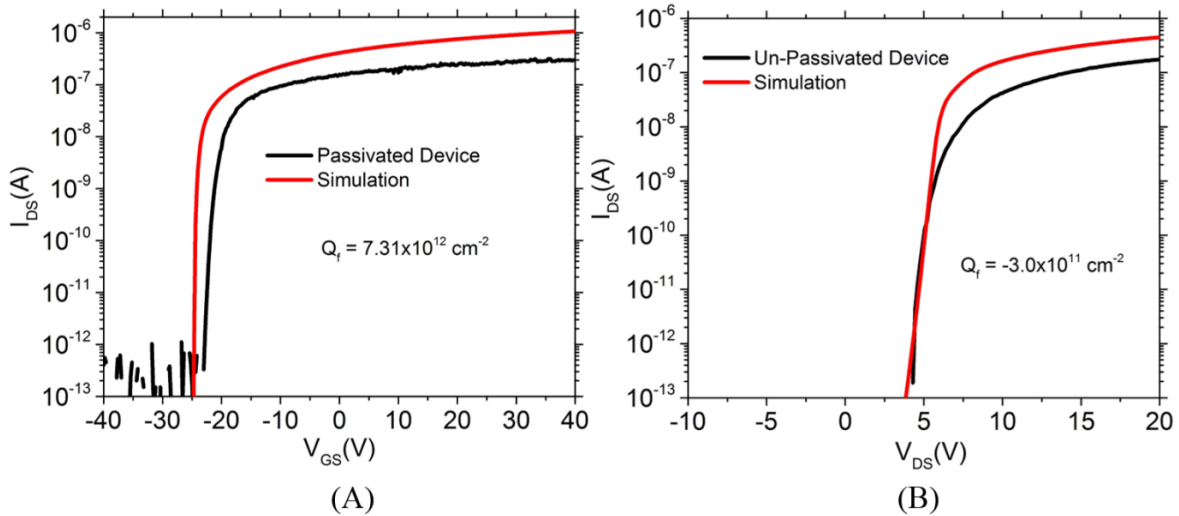(A)   (B)

Fig. 13: 3D Simulation of the ZnO NWFET compared with (a) passivated and (b) unpassivated devices after increasing or decreasing the fixed charge (Q_f). V_{DS} is fixed at 1.0 V.

The subthreshold slope of the unpassivated device fits well with simulation. However, the subthreshold slope of the passivated device does not agree well hence interface state charge was introduced in the simulation so as to better fit the measured characteristic of the passivated device. In Fig.14 the interface state charge parameter (N_{GA}) was the only parameter modified in the simulation of the passivated device to fit the subthreshold slope. It can be seen that the measured characteristic can be well fitted at currents below 1 nA. N_{GA} can be converted into an interface state density using the parameters in Table. *'E'* is assumed to equal the band-gap of ZnO, which is a value that gives the highest value of interface state density. This gives an interface state density of 9.1×10^{17} cm^{-3} for the unpassivated device and 1.5×10^{18} cm^{-3} for the passivated device. These values are higher than that typically obtained for the Si/SiO$_2$ interface, but are reasonable for a ZnO/SiO$_2$ interface that was fabricated using low temperature processing.
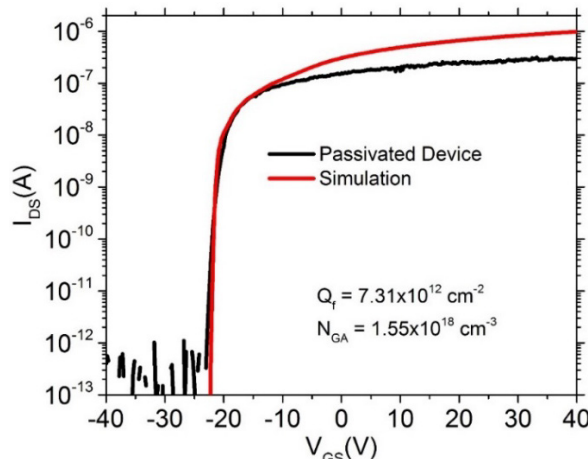

Fig.14: 3D Simulation of the passivated ZnO NWFET after increasing the density of states (DoS) parameter N_{GA}. V_{DS} is fixed at 1.0 V.

Fig.15 shows 3D simulations of the passivated and unpassivated ZnO NWFETs after introducing contact resistance. To fit the experimental curves, values of 3.0×10^5 Ω and 3.0×10^6 Ω were needed for the unpassivated and passivated devices respectively. The simulated value for the unpassivated device is in good agreement with the measured value ($R_{con} = 3.0 \times 10^5$ Ω). However, the simulated

value for the passivated device has higher contact resistance than experiment (R_{con} = 2.5 x 10^4 Ω). The passivated device had a less steep slope than the un-passivated device which means that it suffered from higher interface state trapped charge. This must have caused the inaccuracy of the simulated contact resistance.
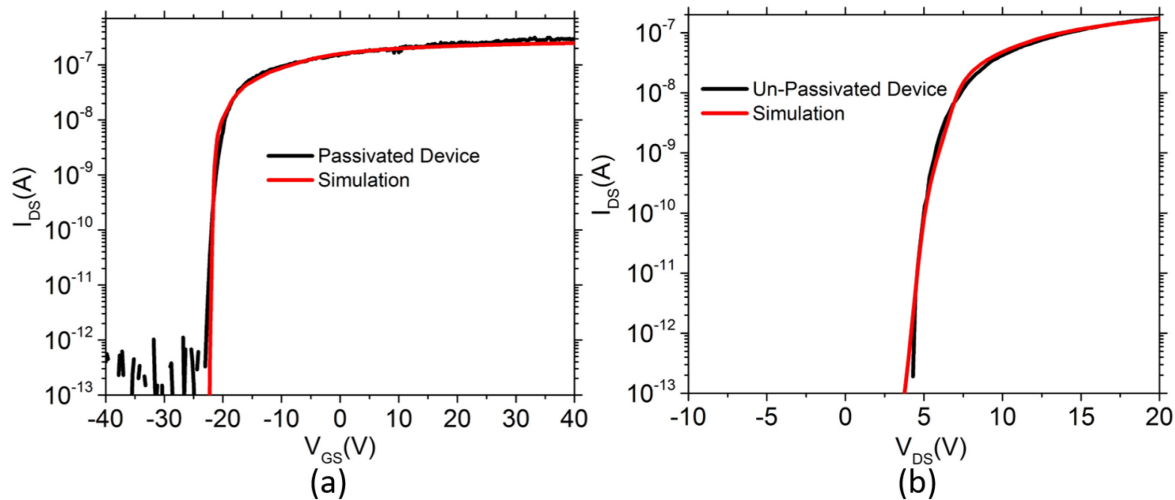

Fig.15: 3D Simulation of the ZnO NWFET after including contact resistance. (a) passivated ZnO NWFET device (b) unpassivated ZnO NWFET device. V_{DS} is fixed at 1.0 V.

Conclusion

Top-down ZnO NWFETs were successfully fabricated with and without Al_2O_3 passivation. This was done by developing a new recipe for depositing a thin film of ZnO. By using a high donor concentration of 1.7 x 10^{18} cm^{-3} for the thin film, contact resistance values were lowered (passivated has R_{con} = 2.5 x 10^4 Ω; unpassivated has R_{con} = 3.0 x 10^5 Ω). By depositing Zn first instead of O_2, steep subthreshold slopes were obtained. The passivated device has a subthreshold slope of 225 mV/decade and the unpassivated device a slope of 125 mV/decade. Well-behaved electrical characteristics have been obtained and the passivated device shows a field effect mobility of 10.9 cm^2/Vs and the un-passivated device a value of 31.4 cm^2/Vs. Simulations have shown that these values of sub-threshold slope translate into interface state densities of 9.1 x 10^{17} cm^{-3} for the unpassivated device and 1.5 x 10^{18} cm^{-3} for the passivated device. The passivated device is suitable for biosensing applications.

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