ADAPTIVE PROPORTIONAL-INTEGRAL-DERIVATIVE CONTROLLER ON FIELD PROGRAMMABLE GATE ARRAY

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Dedicated, in thankful appreciation for support and encouragement to my lovely wife Chantheve Syita, both of my sons Krydtanand Srisuwan and Krydchakphorn Srisuwan, my parents, families and friends.

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ABSTRACT

Proportional-Integral-Derivative (PID) controllers tuned with heuristic tuning methods such as Ziegler-Nichols method are not completely capable to perform high precision control, typically due to large overshoots and poor load regulation. Any changes to the tunable PID parameters we done accordingly offline. Current Field Programmable Gate Array (FPGA) based platform can be used as a high-precision controller implementation. Using FPGA for high precision control offer good resource utilization, power consumption, programmability, cost, and more importantly, it can support parallel controllers. With the improvement of FPGA devices that sometime mirror the performance of the general purpose processor, more complex PID design such as adaptive PID can be implemented. Adaptive PID controller can adjust its own parameters and is able to simultaneously support multiple applications at once. The objective of this project is to design adaptive PID controller on FPGA and analyze the performance of it adaptive or self-tuning capabilities when reference and error signal vary. Another objective is to minimize the instability and reducing the overshoot, undershoot, settling time and ringing. The Altera Quartus and Altera ModelSim environments are used to model the adaptive PID using Verilog Hardware Description Language through Register Transfer Level modeling methodology. These tools are also used for simulating the controller and evaluating non-functional performance characterization.The overall adaptive PID result outperforms the conventional PID and offer slight improvement on noise injection test case.

ABSTRAK

Pengawal berkadar terus-berkamiran-pembeza (PID) dilaraskan mengunakan kaedah heuristik seperti kaedah Ziegler-Nichols kebiasaanya tidak memuaskan dalam kawalan yang mementingkan ketepatan. Setiap perubahan parameter PID perlu dilakukan sesuai secara luar talian. Platform berasaskan penggabungan sistem seni bina (FPGA) boleh digunakan untuk melaksanakan pengawal yang mempunyai ketepatan yang tinggi. Menggunakan FPGA untuk kawalan ketepatan yang tinggi menawarkan penggunaan sumber yang optimum, mengurangkan penggunaan kuasa, memudahkan penyusunan program, mengurangkan kos dan yang lebih penting ialah kebolehan menyokong pengawal selari. Dengan peningkatan prestasi peranti FPGA ia seakan mencerminkan prestasi mikro pemproses, ia sesuai untuk reka bentuk PID yang lebik kompleks. Pengawal PID adaptasi yang boleh melaraskan parameter sendiri secara dalam talian. Objektif projek ini adalah untuk mereka bentuk pengawal PID adaptive di platform FPGA dan menganalisis prestasi dan keupayaan sistem mudah suai ketika berlaku kesilapan atau isyart yang berbeza. Satu lagi objektif adalah untuk meminimumkan ketidakstabilan dan mengurangkan isyarat lampau, masa pengenapan dan ketidaksabilan. Altera Quartus II dan Altera ModelSim digunakan untuk mereka bentuk PID dengan menggunakan verilog. Perisian yang sama juga digunakan untuk simulasi pengawal PID dan menganalisis prestasinya.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

APID	-	Adaptive Proportional-Integral-Derivative
ASIC	-	Application Specific Integrated Circuit
DC	-	Direct Current
DSP	-	Digital Signal Processor
DFG	-	Design Flow Graph
DU	-	Datapath Unit
FPGA	-	Field-Programmable Gate Array
IC	-	Intergrated Circuit
P	-	Proportional
PI	-	Proportional-Integral
PID	-	Proportional-Integral-Derivative
ZN	-	Ziegler-Nichols

CHAPTER 1

INTRODUCTION

Around 60 years in the industry, PID (Proportional-Integral-Derivative) controller was the only one design method in the control system. The most common controllers are PID controller and the variant.PID controller is simple to design and offers robust performance.Besides that, the PID controller also knows as a good noise tolerance and cheaper solution. Operation of digital PID controller has gone over several stages of evolution. It is from the early mechanical and pneumatic designs to the microprocessor based systems. On the other hand, these systems have the disadvantages of demanding control requirements of modern power conditioning systems will excess most of the microprocessors and the computing speed limits the use of microprocessor in complex algorithms. However, microprocessors, microcontrollers and digital signal processors (DSPs) can no longer keep pace with the new generation of applications. This is because it requires more flexible and higher performance without increasing any resources and cost. Additionally the tasks are executed consecutively which takes longer processing time to achieve the same task in microcontrollers and DSPs.

Lately, Field Programmable Gate Arrays (FPGA) has becoming another option for digital control systems realization. There are few benefits provided in FPGA based controllers. For examples faster computation time, complex functionality, real-time processing abilities and the power consumption is low[3]. Through this project, the design consideration is digital PID controller with adaptive module implemented in FPGA platform. The controller functionality is defined in Verilog following the standard digital design practices.The project is therefore targeted toward the FPGA board by using the synthesis tool. The FPGA stands a greater substitute to cover programmed ASICs. Moreover, FPGAs is cheaper platform, reduce the development time and the inflexibility of ASICs. Furthermore, the programmability of FPGA is allowed the design changes or upgrades in the field without any replacement of hardware that not possible with ASICs.

1.1 Problem Statement

Proportional-Integral-Derivative (PID) controllers tuned with heuristic tuning methods such as Ziegler-Nichols method are not completely capable to perform high precision control, typically due to large overshoots and poor load regulation. Any changes to the tunable PID parameters is done accordingly offline.

Current FPGA based platform can be used as a high-precision controller implementation. Using FPGA for high precision control offer good resource utilization, power consumption, programmability, cost, and more importantly, it can support parallel controllers. Current PID controller realization on FPGA only adopt this type of method. With the improvement of FPGA devices that sometime mirror the performance of the general purpose processor, more complex PID design such as adaptive PID can be implemented. Adaptive PID that can adjust its own parameters on the fly and is able to simultaneously support multiple applications at once.

1.2 Objective

The general goal for this project is to design and simulate the adaptive PID controller in Verilog. The project objective can be described as:

- To design the conventional PID as a benchmark for adaptive PID controller.
- The adaptive PID controller is design based on conventional with adaptive block or updating factor $\beta(k)$.
- To compare the performance between conventional PID versus adaptive PID controller.
- To analyze the performance of it adaptive or self-tuning capabilities when reference and error signals vary.
- To minimize the instability and reducing the overshoot, undershoot, settling time and ringing.

1.3 Scope

The project scope is another important criteria that lead the project according to the objective. This is important key that to ensure the project is done correctly and meet the goal. The scope of work are:

- Analyse discrete PID controller algorithm
- RTL design and testbench written in Verilog programming using Altera Quartus II and ModelSim-Altera.
- A testbench is used to validate the PID
- Compare the expected result versus simulated result.

1.4 Organization

There are five chapters in this project report.

Chapter 2 consist of the literature review and discussion about the research of the PID controller design.

Chapter 3 consist of the system overview, methodology and implementation of the project. This will mention about the algorithm of the PID and also the adaptive module algorithm. Lastly, the architecture development and hardware design step.

Chapter 4 will explains the testing and result of the design. This including the discussion and the performance comparison analysis.

Chapter 5 conclude about the project result and the recommendation to enhance the design in the future.

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