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Modeling of Nanoscale MOSFET Performance in the Velocity Saturation Region

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Abstract: Velocity saturation as a function of temperature and drain voltage for n-channel MOSFET is investigated. The combination of an existing current-voltage (I-V) model, drain source resistance model and a more precise mobility derivation gives an accurate representation of velocity saturation as a function of the above parameters. A simplified threshold voltage formulation is developed to provide similar accuracy when compared to actual devices. The models show good agreement with the experimental data over a wide range of gate and drain bias for 90nm process technology.

Keywords: Current-voltage, Drain source resistance, MOSFET, Threshold voltage, Velocity saturation.

1. INTRODUCTION

Velocity saturation in Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a phenomenon which occurs in high electric field where the mobility degradation causes drift velocity to reach a maximum value typically at $\upsilon_{sat} \approx 10^7$ cm/s. The electric field at which saturation occurs differs with different semiconductors. At high fields up to 10^6 V/cm [1] in nanoelectronic devices, scattering rate of highly energetic electrons increases with the average carrier energy. Eventually, the carrier loses their energy by optical-phonon emission nearly as fast as they gain from the field. This ultimately increases the transit time of carriers through the channel. In the quest to obtain higher speed, performance and chip density, the channel length (L) and channel width (W) are being scaled down [2]. The basic structure of a n-channel MOSFET (NMOS) is shown in Figure 1.

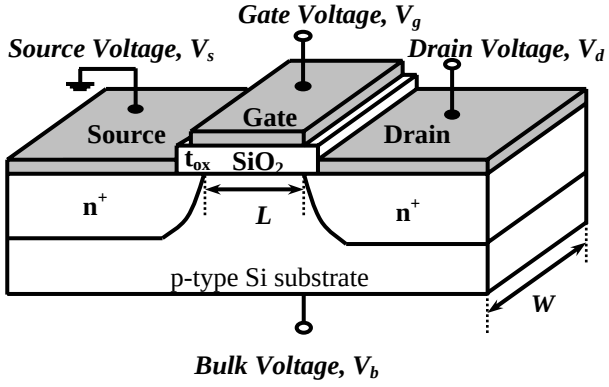

Figure 1. Basic structure of a NMOS

As devices are getting smaller and smaller, undesirable effects are encountered. In the current 65nm and 90nm process technology designs, second order effects such as velocity saturation, short channel effect (SCE), channel length modulation (CLM) and narrow width effect (NWE) are encountered during the design phases [3]. Velocity saturation particularly affects the drive strength in the saturation velocity region. SCE could be ignored in previous long channel CMOS generation as the effects is not that significant [4].

The development of short channel semi empirical model for nanoscale MOSFET [5-7] has enable an in depth investigation on the saturation velocity impact in a wider scope. The nanoscale MOSFET has features size beyond 50nm and below 100nm for 90nm process technology. In this paper, the occurrence of velocity saturation, υ_{sat} and its impact on electric field, external environment and I-V characteristic at different process parameters are analyzed and presented. The paper is organized as follows. Section 1 gives a deeper insight onto velocity saturation and its limitation that was highlighted by several researchers [8-10] as well as the key contribution. A detailed description on the models used is presented in Section 2. Results are presented and discussed in Section 3. Section 4 concludes the study.

2. MODEL AND METHODS

Threshold voltage, effective mobility, doping concentration, diffused junction depth, gate oxide thickness, gate oxide capacitance and others related physical parameter are extracted from the experimental data generated from the Intel Proprietary Schematic Editor and Intel Proprietary Circuit Simulator. Subsequently, curves based on the newly developed threshold voltage model, effective mobility model and I-V model are plotted using Microsoft Excel. The velocity longitudinal field equation is then incorporated to model the velocity saturation region (VSR). Finally, based on the graphs depicted, the velocity saturation relationship between the models is analyzed.

2.1 The Threshold Voltage Model

A new effective threshold voltage model is derived in this section based on the long channel device. Several modifications are employed to consider the effects of

short and narrow channel effects. There are varieties of definition models [11]–[14] which are used to measure and predict the threshold voltage model each with its unique features and limitations. In this work, the threshold voltage equation for n-channel MOSFET with n+ polysilicon gate and p-type silicon substrate is defined as

$$V_T = 2\phi_f + V_{FB} + \frac{\sqrt{2\varepsilon_{Si} q N_A \left(2\phi_f\right)}}{C_{ox}} \tag{1}$$

where ϕ_f is the Fermi potential given as

$$\phi_f = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) \tag{2}$$

N_A is the substrate doping concentration, k is the Boltzmann's constant, ε_{Si} is the dielectric permittivity of the silicon and C_{ox} is the gate oxide capacitance. The flat band voltage, V_{FB} is given as

$$V_{FB} = \left(\phi_{ms} - \frac{Q_{ss}}{C_{ox}}\right) \tag{3}$$

where ϕ_{ms} is the metal-semiconductor work function difference and Q_{ss} is the fixed oxide charge. As the device is scaled down in size, additional effects on V_T occur. The short channel threshold voltage shift reducew V_T predicted by the long channel. The threshold voltage shift due to short channel effects can be expressed as

$$\Delta V_{T\ for\ short\ channel} = -\frac{qNx_{dT}}{C_{ox}}\left[\frac{r_j}{L}\sqrt{1+\frac{2x_{dT}}{r_j}} - 1\right] \tag{4}$$

where x_{dT} is the lateral space charge width and r_j is the diffused junction as shown in Figure 2 below.

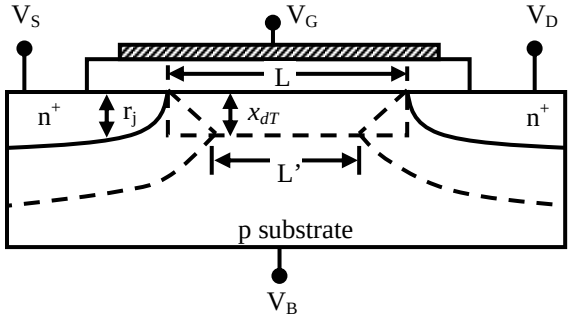

Figure 2. Charge sharing in the short channel threshold voltage model

On the other hand, as the channel width is reduced, the threshold voltage is reduced. This is know as the narrow-width effect and can be approximated as

$$\Delta V_{T\ for\ narrow\ width} = \frac{qNx_{dT}}{C_{ox}}\left[\frac{\xi x_{dT}}{W}\right] \tag{5}$$

where ξ is the empirical parameter that account for the shape of the fringe depletion region and q is the electronic charge. The resultant threshold voltage expression that take into account the short channel and narrow width effect can be expressed as

$$V_T = 2\phi_{fp} + V_{FB} \pm \frac{\sqrt{2\varepsilon q N\left(2\phi_f\right)}}{C_{ox}} - \frac{qNx_{dT}}{C_{ox}}\left[\left(\frac{r_j}{L}\sqrt{1+\frac{2x_{dT}}{r_j}} - 1\right) - \left(\frac{\xi x_{dT}}{W}\right)\right] \tag{6}$$

The Mobility Model

The effective mobility of inversion layer carriers is a significant factor in the performance of a MOSFET. A physically based semi-empirical equation is employed to model the surface roughness, phonon and coulomb scattering. This model is an extension of the work done by Schwarz and Russek [15]. The scattering mechanism now includes surface roughness and coulombic scattering to account for high transverse electric field and high doping concentration operation level. Each scattering contribution to the effective mobility is calculated according to Matthiessen's rule as depicted below [16].

$$\mu_{\perp eff} = \left[\frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_c}\right]^{-1} \tag{7}$$

where μ_c is Coulombic scattering due to doping concentration, μ_{ph} is phonon scattering and μ_{sr} is surface roughness scattering. The model for effective mobility of electron in MOS with (100) plane structure is given as [17]

$$E_{\perp eff} = \frac{1}{\varepsilon_{si}}\left(\frac{1}{2}Q_{inv} + Q_B\right) = \frac{1}{6t_{ox}}\left(V_{gs} + V_t\right) \tag{8}$$

$$\mu_{ph} = \left[\left(\frac{K_B}{T_n^{-2.5}}\right)^{-1} + \left(\frac{z}{3.2\text{x}10^{-9}\, pT_n^{1/2}}\right)^{-1}\right]^{-1} \tag{9}$$

$$\mu_{sr} = K_{sr} E_{\perp eff}^{-2} \tag{10}$$

$$\mu_c = \frac{1.1\text{x}10^{-21} T_n^{1.5}}{\ln\left(1+\gamma_{BH}^2\right) - \frac{\gamma_{BH}^2}{\gamma_{BH}^2+1}}\frac{1}{N_A} \tag{11}$$

$$p = 0.09T_n^{1.75} + 4.53\text{x}10^{-8}\left(\frac{N_I}{z}\right)^{-0.25}\left(\frac{N_f}{T_n}\right) \tag{12}$$

$$z = z_{QM} + z_d = \frac{0.388T_n}{E_{\perp eff}} + \frac{1.73\text{x}10^{-5}}{E_{\perp eff}^{1/3}} \qquad (13)$$

where p is the Fuchs factoring scattering which describe the probability of diffuse scattering, z is the averaged inversion layer width, N_f is the interface charge density, z_{cl} is the classical channel width, z_{QM} is the quantum mechanically broadened width due to the two dimensional quantization of the energy levels in the inversion layer, γ^2_{BH} is the Brooks Herring constant while K_B, K_{QM}, K_{sr}, K_c and K_γ are numerical coefficients that provide best agreements with the experimental data. The normalized temperature, T_n is given by

$$T_n = \frac{T}{300} \qquad (14)$$

2.2 The I-V Model

There are parasitic resistances associated with the source and drain. These source drain resistance has to be taken into account as it causes a substantial drain current degradation as well as an RC delay. A physically-based source/drain (S/D) series resistance R_{ds} model comprising intrinsic and extrinsic component is included. The model is based on the concept introduced by Zhou and Lim [18] and is given by

$$R_{s/d} = R_{ext} + R_{int} = \frac{2\rho S}{x_j W} + \frac{\upsilon}{V_{GS} - V_T} \qquad (15)$$

where R_{ext} is the extrinsic resistance, R_{int} is intrinsic resistance, x_j is the junction depth, S is the spacer thickness and ρ is taken as effective resistivity of the S/D regions (including contacts). The I-V model is based on the compact model derivation by Xing Zhou *et al.* [19].

The model has similar characteristic as BSIM3v3 model and comparable to HSPICE level 49. It is selected to be the core model formulation since it well considered being the standard model from deep submicron into nanoscale CMOS circuit design. The step by step derivation of I_{ds} model including the effect of CLM and R_{sd} is given below. The initial drain current, I_{ds} when source drain resistance is ignored is expressed as

$$I_{ds0} = \frac{\mu_{eff} C_{ox} W}{(2L)\left[1 + \left(V_{deff}/EL\right)\right]}\left(V_{GT}V_{deff} - \frac{1}{2}mV_{deff}^{\ 2}\right) \qquad (16)$$

V_{deff} is the smoothing function to replace V_{ds} for a smooth transition from linear to saturation region to form a single compact model and is given as

$$\begin{aligned} V_{deff} &= V_{dsat} - \frac{1}{2}\left[V_{dsat} - V_{ds} - \delta_s\right] \\ &\quad - \frac{1}{2}\left[\sqrt{\left(V_{dsat} - V_{ds} - \delta_s\right)^2 + 4\delta_s V_{dsat}}\right] \end{aligned} \qquad (17)$$

When CLM effect is taken into consideration, Equation (16) can be rewritten as

$$I_{deff} = \left(1 + \frac{V_{ds} - V_{deff}}{V_{Aeff}}\right) I_{ds0} \qquad (18)$$

where I_{deff} is the smoothing function for I_{ds0} with effective early voltage, V_{Aeff}. With the inclusion of Equation (17) and Equation (18), the drain current is given by

$$I_{ds} = \frac{I_{deff}}{1 + \left(R_{s/d} I_{deff}\right)/V_{deff}} \qquad (19)$$

2.4 The Velocity-Field Model

In order to describe the electric field dependence, the velocity model for electron [20-21] is given as

$$v_d = \frac{\mu_{eff} E}{\left[1 + \left(E_y/E_c\right)^2\right]^{1/2}} \qquad (20)$$

where E_c is the critical electric field for velocity saturation defined by

$$E_c = \frac{v_{sat}}{\mu_{eff}} \qquad (21)$$

The longitudinal electric field across the channel, E_c can be expressed as

$$E_y = \frac{V_d - IR_{sd}}{L} \qquad (22)$$

3. RESULTS AND DISCUSSION

The simulations cover a wide range of temperatures, effective field and parasitic resistance to establish reliable models operating at different environment. The short channel NMOS channel length is 80 nm with the widths of 1.3 micron. Figure 3 gives the variation of the electron mobility as a function of effective longitudinal field along the channel.

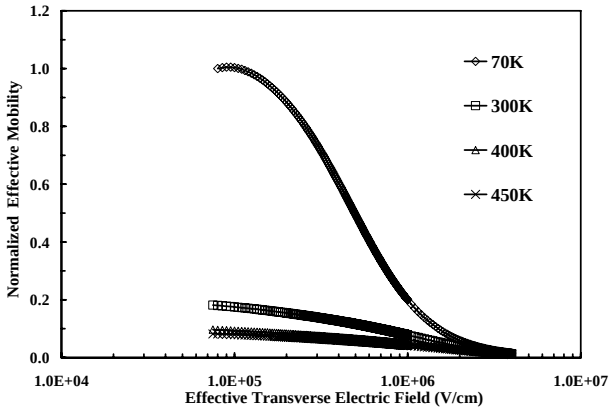

Figure 3. Normalized effective mobility versus transverse electric field at different temperature

It is shown that for an electric field of $1.0\text{x}10^5$ V/cm, devices at 77K have a higher effective mobility and this

in turn gives a higher drift velocity. As the temperature is increase to 300 K and above, the mobility decreases substantially as scattering is far more frequent. Devices at low temperature will first gain velocity saturation. The drift velocity of electrons at different temperature becomes saturates beyond the critical field region at $1.0x10^6$ V/cm.

In order to get an overall best fit graph, the velocity saturation value has to be in the range of the process model parameter. The velocity saturation is extracted from the experimental data by using the I-V models. By incorporating the parameter into the velocity model, the simulation results illustrate a satisfactory agreement with the I-V experimental data across a wide range of gate voltage as shown in Figure 4.

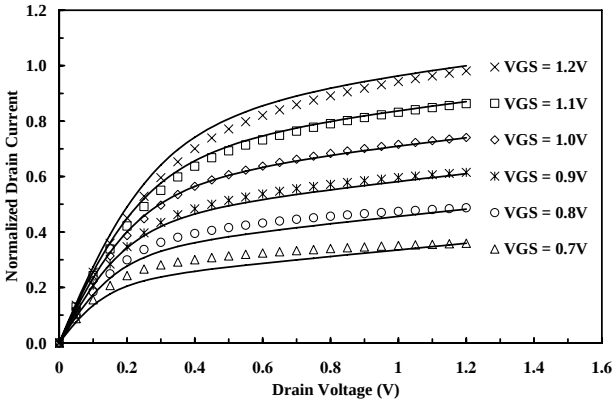

Figure 4. Comparison of calculated versus measured I-V characteristics for a wide range of gate voltage at resistivity 3.5e-5 Ω/cm

The results of experimental data investigation with simulation model are presented. This includes observation in the constant velocity saturation region with respect to gate voltage at low and high effective parasitic resistance. Parasitic resistances, ρ of 3.5e-5 Ω/m and 5.5e-5 Ω/m are used. Low parasitic resistance has a reduced source drain series resistance, R_{sd} and this gives a higher drain current as shown in Figure 5.

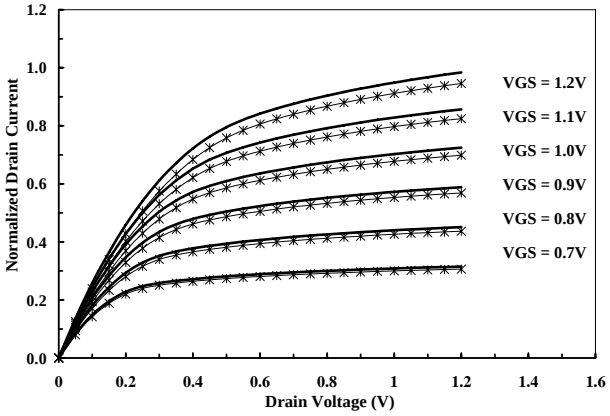

Figure 5. Comparison of calculated I-V characteristics for a wide range of gate voltage at resistivity 3.5e-5 Ω/cm (bold solid line) and 4.5e-5 Ω/cm (in asterix)

In addition, saturation voltage is reduced. The reason for this is that drain current is inversely proportional to the drain series resistance. When R_{sd} is taken into consideration, a larger drain and source voltage need to be applied to achieve velocity saturation in order to make up for the drain and source voltage drop. It is found that the drift velocity is affected by the longitudinal electric field drop when R_{sd} is increased.

Channel length modulation (CLM) is a non ideal characteristic that is present in short channel MOSFET. The channel length is modulated by the drain current when it is saturated. The current deviate from its ideal I-V curve as the average electric field increase with the shortening of effective channel length. Figure 6 show the comparison of the calculated I-V characteristics for a wide range of gate voltage at resistivities of 3.5e-5 Ω/cm with and without channel length modulation.

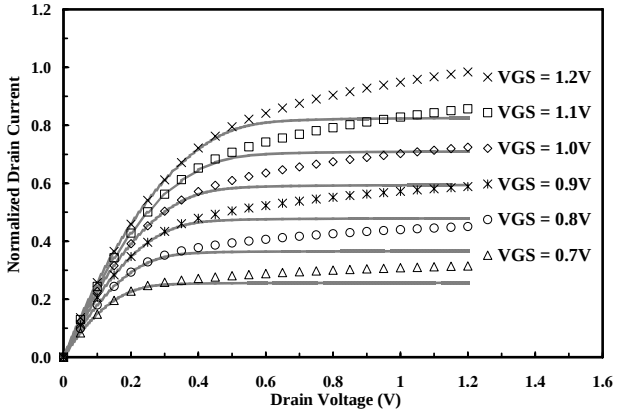

Figure 6. Comparison of calculated I-V characteristics for a wide range of gate voltage at resistivity 3.5e-5 Ω/cm with CLM (pattern) and without CLM (shaded line)

Notable differences can be found where the saturation drain current is predicted higher in the saturation region compared to the shaded lines (without CLM) as shown in Figure 6.

4. CONCLUSION

The analytical and semi empirical models are used to investigate the electrical behavior of nanoscale NMOS. We have demonstrated that simulation from the I-V model is in good agreement with the experimental data. The semi empirical formula presented here has allowed us to see the impact of velocity saturation. Saturation current in the short channel devices no longer has an ideal square law dependence predicted for long channel. The saturation current is now increasing linearly with gate voltage as shown in Figure 7.

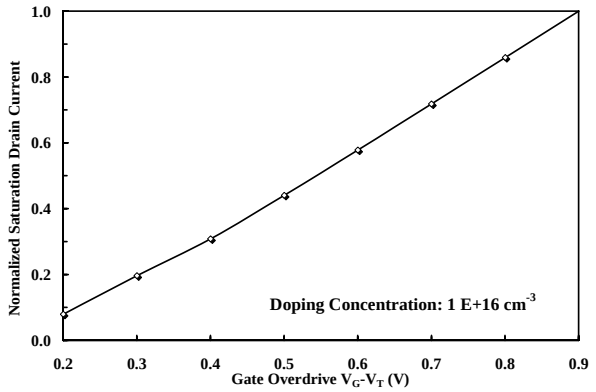

Figure 7. Normalized saturation drain current versus gate overdrive

On the other hand, the drain current for short channel device under the influence of velocity saturation is lower causing a longer switching transition time due to a low gate overdrive. The introduction of strained silicon can be used to enhance transistor current flow or drive current which allow electrons and holes to move smoother at higher mobility.

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