Characterization of 50 nm MOSFET with dielectric pocket

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Characterization of a metal-oxide-semiconductor field effect transistor incorporating dielectric pocket (DP) for suppression of short-channel effect (SCE) is demonstrated by using 2D numerical simulation. An analysis of 120 nm and 50 nm channel length (L_g) with DP incorporated between the channel and source/drain has been done successfully. The DP has suppressed short channel effect (SCE) without the needs of increasing the channel doping profile. With uniform doping of 10^{17} cm^{-3} and 10^{20} cm^{-3} for channel and source/drain region respectively, a reduction of 2.5 decades of leakage current (I_{OFF}) was obtained in MOSFET with DP without altering the drive current (I_{ON}) for 120 nm channel length. A very low leakage current of 0.002 pA/µm is obtained for DP device with drain voltage (V_{DS}) of 0.1 V and increase to 18 pA/µm with V_{DS} = 1.0V for 120 nm Lg. This obtained with drive current of 0.5 mA and 5 mA respectively. Meanwhile, with L_g = 50 nm, 700 nA/µm leakage current and 1 mA/µm drive current was observed. With the same doping profiles, a reduction of 1.4 decades of I_{OFF} was shown by the incorporation of DP for L_g = 50 nm. Thus, the incorporation of DP will enhance the electrical performance and give a very good control of the SCE for scaling the MOSFET in nanometer regime for future development of nanoelectronics product.

I. INTRODUCTION

MOSFETs device have been scaled down aggressively over the past few decades in order to achieve increased circuit density (more circuit functions in a given silicon area) and higher performance (higher switching speed, lower power dissipation, etc). However, continued scaling faces challenges such as lithography, doping fluctuations and short channel effects (SCE) [1]. Recently, in deep submicron CMOS technology, pocket implementation [2-9] appears to be a commonly used strategy for suppressing SCE. However, many problems such as increased of the body factor and junction capacitance as well as junction leakage current [10]. In addition, high channel doping increases the avalanche breakdown at the drain/substrate junction. The incorporation of an oxide layer (called dielectric pocket) between source/drain and body suppressed SCE and allows the threshold voltage and the performance of the device to be optimized [11]. Unfortunately, the study on incorporation of DP was only made with the gate length down to 120 nm.

In this paper, characterization of a metal-oxide-semiconductor field effect transistor incorporating dielectric pocket (DP) for suppression of short-channel effect (SCE) is demonstrated by using 2D numerical simulation. An analysis of 120 nm and 50 nm channel length (L_g) with DP incorporated between the channel and source/drain has been done successfully. The DP has suppressed short channel effect (SCE) without the needs of increasing the channel doping profile. With uniform doping of 10^{17} cm^{-3} and 10^{20} cm^{-3} for channel and source/drain region respectively, a reduction of 2.5 decades of leakage current (I_{OFF}) was obtained in MOSFET with DP without altering the drive current (I_{ON}) for 120 nm channel length. A very low leakage current of 0.002 pA/µm is obtained for DP device with drain voltage (V_{DS}) of 0.1 V and increase to 18 pA/µm with V_{DS} = 1.0 V for 120 nm Lg. This obtained with drive current of 0.5 mA and 5 mA respectively. Meanwhile, with L_g = 50 nm, 700 nA/µm leakage current and 1 mA/µm drive current was observed. With the same doping profiles, a reduction of 1.4 decades of I_{OFF} was shown by the incorporation of DP for L_g = 50 nm. Thus, the incorporation of DP will enhance the electrical performance and give a very good control of the SCE for scaling the MOSFET in nanometer regime for future development of nanoelectronics product.

II. DEVICE STRUCTURE AND MODELING

The device structure is design and simulated using SILVACO (ATLAS) software package. Fig. 1 shows the simulated device structure with all the dimension of respective region is explicitly shown. The device consists of a silicon semiconductor substrate with uniform boron doping of 10^{17} cm^{-3} on which a thin layer of insulting oxide (SiO_2) of thickness t_{ox} = 2 nm is grown. A conducting layer called the polysilicon gate electrode is deposited on top of the oxide. The gate is heavily doped with phosphorus of 10^{20} cm^{-3}. Two heavily phosphorus doped of 10^{20} cm^{-3} regions with depth X_j = 100 nm, called the source and the drain are formed in the substrate on either side of the gate. The

source and the drain regions overlap slightly with the gate. The channel length region of 50 nm and 120 nm are designed for an analysis of their characteristics. The height and width of the dielectric pockets are 70 nm and 20 nm, respectively. A heavily dense mesh is needed in critical regions such as channel, DP area and gate oxide for accurate characterization of the device.

The inversion layer mobility model from Lombardi [12] was employed for its dependency on the transverse field (i.e. field in the direction perpendicular $E_\perp$ to the Si/SiO_2 interface of the MOSFET) and through velocity saturation at high longitudinal field (i.e. field in the direction from source-to drain parallel E to the Si/SiO_2 interface) combined with SRH (Shockley-Read-Hall Recombination) with fixed carrier lifetimes models [12]. This recombination model was selected since its take into account the phonon transitions effect due to the presence of a trap (or defect) within the forbidden gap of the semiconductor. An interface fixed oxide charge of 3×10^{10} Coulomb is assumed with the used of n-type Polysilicon gate contact for the device. The Drift-Diffusion transport [12] model with simplified Boltzmann carrier statistics [12] is employed for numerical computation of the design device.

II. ELECTRICAL CHARACTERIZATION

The combination of Gummel and Newton numerical methods [12] was employed for a better initial guess in solving quantities for obtaining a convergence of the device structure. Figs. 2 and 3 show the current-voltage ($I_D - V_{GS}$) characteristics and subthreshold curves for NMOS device of channel length L_g = 50 nm with the comparison between with and without DP. In Fig. 2, the V_T is increased in magnitude with an incorporation of DP. As summarized in Table I, with L_g = 50 nm and V_{DS} = 0.1 V, V_T is increase to −0.17 V while V_T increase to −0.63 V when V_{DS} = 1.0 V. The lower value of V_T was obtained due to the lower body or channel doping of 10^{17} cm^{-3} and high S/D doping of 10^{20} cm^{-3}. Thus, the channel was created with the small value of V_{GS}. With the DP existed between S/D regions, the SCE is controllable and the device was behaving more to NMOS rather than PMOS for channel length of 50 nm.

In the off-state operation mode the transistor show a drain leakage current I_{OFF} which is independent of the gate voltage, but increases with increasing drain voltage as depicted in Fig. 3. With DP incorporation, a very low off-state leakage current I_{OFF} = 6.74×10^{-7} A/μm and good drive current I_{ON} of 9.82×10^{-4} A/μm taken at V_{DS} = 0.1 V was explicitly shown. Its increase to 9.98×10^{-5} A/μm in I_{OFF} and 4.8×10^{-3} in I_{ON} when taken at V_{DS} = 1.0 V. Thanks to dielectric pockets, the off-state current can be significantly reduced by 0.5 decades for V_{DS} = 1.0 V and increases to 1.4 decades for V_{DS} = 0.1 V. The reduction in the SCEs in the devices with dielectric pockets explains the difference in the threshold voltages of measured short-channel devices.

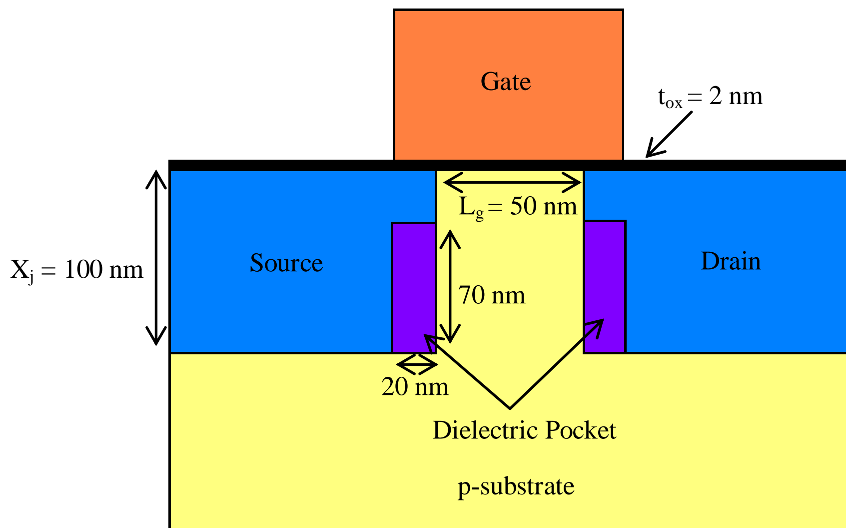

FIG. 1. Schematic structure of NMOS device with dielectric pocket.

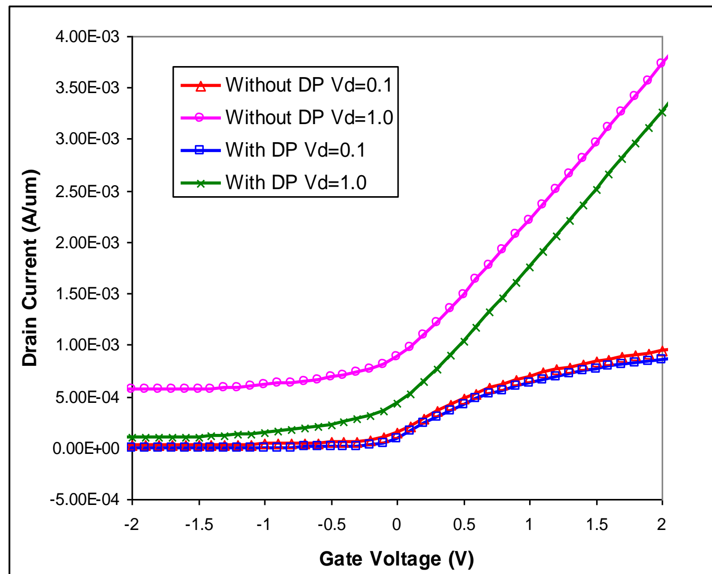

FIG. 2. Current-voltage (I_D vs V_{GS}) characteristic of NMOS incorporating DP with L_g = 50 nm.

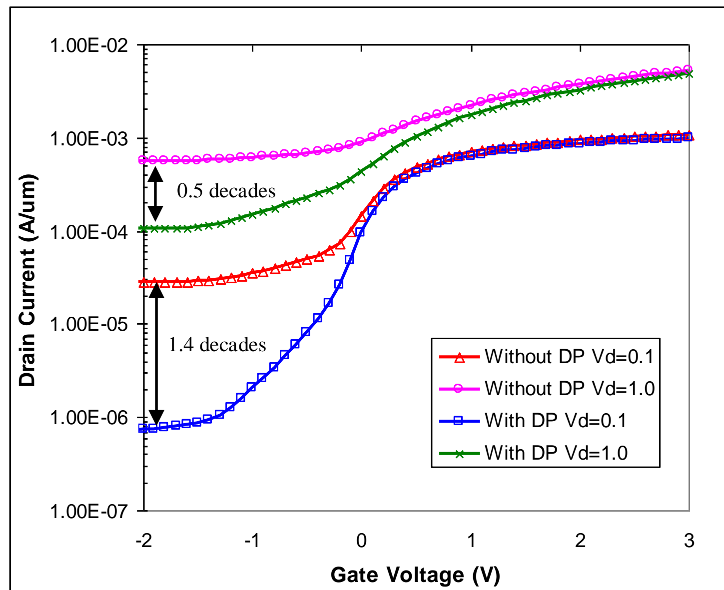

FIG. 3. Subthreshold curves of NMOS incorporating DP with L_g = 50 nm.

TABLE I. Characterization of NMOS incorporating DP with L_g = 50 nm.

NMOS	L_g	V_{DS}	V_T	I_{OFF}	I_{ON}
Without DP	50 nm	0.1	-0.24	2.72e-5	1.08e-3
With DP	50 nm	0.1	-0.17	6.74e-7	9.82e-4
Without DP	50 nm	1.0	-0.92	5.59e-4	5.25e-3
With DP	50 nm	1.0	-0.63	9.98e-5	4.8e-3

III. DEVICE ANALYSIS

Further analysis on the NMOS incorporating DP was done by comparing between channel length, L_g = 50 nm and L_g = 120 nm taken at V_{DS} = 0.1 V. By applying the same mobility and recombination model with different channel length, the resulted of current-voltage characteristic (Fig. 4) and subthreshold characteristics (Fig. 5) of NMOS incorporating DP is summarized in Table II. With V_{DS} = 0.1 V, V_T is increase to −0.17 V when L_g = 50 nm while V_T increase to −0.06 V when L_g = 120 nm. The incorporation of DP is observed more critically needed for 50 nm compared to 120 nm MOSFETs. In other words, for scaling the channel length beyond the nanometer regime, the DP is essential for controlling the aggravated of SCE and setting properly the V_T with lower channel doping [13].

Fig. 5 shows a subthreshold characteristics of NMOS incorporating DP with L_g = 50 nm and 120 nm taken at V_{DS} = 0.1 V. A low off-state leakage current was observed for both cases with the incorporation of DP. However, a reduction of 1.4 decades was observed for 50 nm device and increased to 2.5 decades for 120 nm as compared to non DP device. Even though the reduction is more severe for 120 nm device, the reduction of 1.4 decades in 50 nm device is consider high enough since as the gate length reduce the SCE is aggravated and the reversed biased drain-substrate diode current is increased (the origin of leakage current I_{OFF}). Consequently, with the lower doping levels, the mobility of electrons and holes is also increased and finally the leakage currents increase sharply. This phenomenon is observed critically for deep submicron device. Therefore, with the incorporation of DP between source and drain regions, the carriers mobility can be decreased so as the decreased of leakage currents.

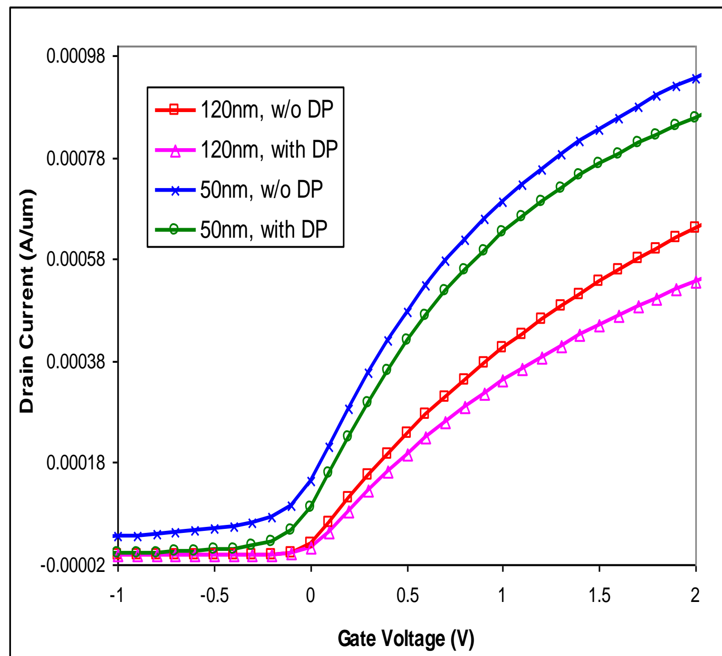

FIG. 4. Current-voltage (I_D vs V_{GS}) characteristic of NMOS incorporating DP with L_g = 50 nm and 120 nm taken at V_{DS} 0.1 V.

TABLE II. Characterization of NMOS incorporating DP with L_g 50 nm and 120 nm taken at V_{DS} = 0.1 V.

NMOS	L_g	V_{DS}	V_T	I_{OFF}	I_{ON}
Without DP	50 nm	0.1	-0.24	2.72e-5	1.08e-3
With DP	50 nm	0.1	-0.17	6.74e-7	9.82e-4
Without DP	120 nm	0.1	-0.08	7.71e-13	8.03e-4
With DP	120 nm	0.1	-0.06	1.76e-15	6.67e-4

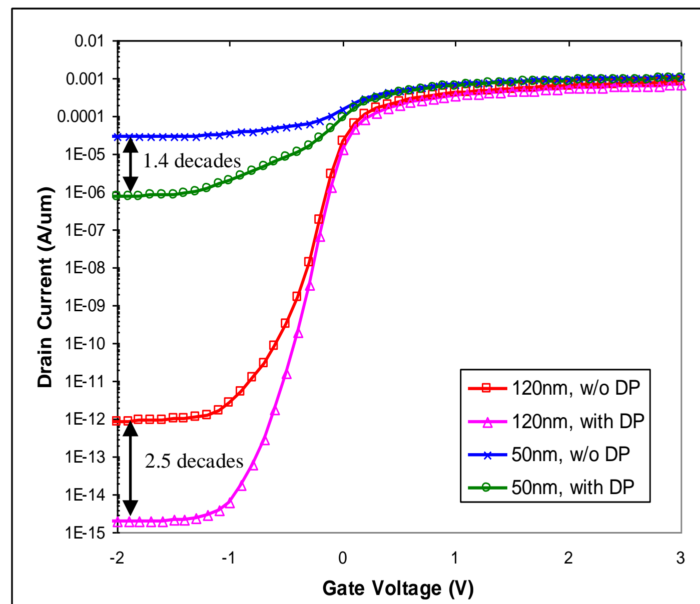

FIG. 5. Subthreshold curves of NMOS incorporating DP with L_g = 50 nm and 120 nm taken at V_{DS} 0.1 V.

IV. CONCLUSIONS

For the first time the analysis of a 50 nm MOSFET with DP incorporated between source and drain regions has been successfully done using commercial ATLAS TCAD tools. By employing the inversion layer mobility model from Lombardi combined with SRH (Shockley-Read-Hall Recombination) with fixed carrier lifetimes models; a detailed investigation on the MOSFET with DP performance was successfully done. The DP has suppressed short channel effect (SCE) without the needs of increasing the channel doping profile. With the gate length of 50 nm, oxide thickness, t_{ox} = 2 nm and uniform doping of 10^{17} cm^{-3} and 10^{20} cm^{-3} for channel and source/drain region respectively, a reduction of leakage current I_{OFF} from 2.72×10^{-5} to 6.74×10^{-7} A/µm was obtained in MOSFET with DP with a small changes of the drive current compared with non-DP devices. Thus, the off-state current can be significantly reduced by 0.5 decades for V_{DS} = 1.0 V and increases to 1.4 decades for V_{DS} = 0.1 V. However, a reduction of 1.4 decades was observed for 50 nm device and increased to 2.5 decades for 120 nm as compared to non DP device due to aggravated of SCE is and an increased of the reversed biased drain-substrate diode current.

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