

Analysis, Design and Simulation of RC Passive Damping Network in a Simple Distributed DC Power System using PSpice

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Abstract: The sub-system interaction and instability phenomena are a common problem in the Distributed Power System (DPS). In order to regulate the output voltage or the speed, the internal control function of a converter known as constant power load (CPL) results in the converter tends to draw a constant power. This phenomenon cause the input impedance of CPL has negative incremental input impedance, which tends to create instability as it is connected to a system. This paper concerns about the compensation method used to improve the stability of two or more connected subsystems, consisting of an L-C filter and a CPL. A compensation method known as passive damping network containing only RC components is examined purposely to eliminate and reduce the instability of the subsystem. The passive damping network was designed and simulated using PSpice. The results show that the designed passive damping network is suitable for small-scale power distribution system that contains constant power load with power level of 1 kW.

Keywords: Constant power load, DC-DC converter, Passive damping circuit.

1. INTRODUCTION

In a distributed power system (DPS), the instability phenomenon is a common problem. DPS is a system, where the power processing functions are distributed among many power processing units or DC/DC converters at the point of need. It is being used in applications such as aircraft, spacecraft, hybrid-electric and electric vehicles, ships, defense electronic power systems, communication and computer systems. The beneficial in terms of weight, size, isolation, voltage regulation, flexibility, capability to integrate a large variety of loads and also enables one to control more easily the quality of power reaching each separate board [1-2] are the reason of using it.

However DPS has some drawbacks such as interaction between the converters and bus instability, as well as imbalance in power distribution among parallel converters, which leads to an unequal distribution of output current hence may create excessive stress on some of the modules and increase their rate of failure. The interaction arises because each individual converter has internal control functions, such as the regulation of the converter output voltage or motor speed [3-6]. As a result, the converter tends to draw a constant power and therefore has a negative incremental input resistance within the bandwidth of the converter control loop. The negative incremental input impedance characteristic is a main characteristic of the constant power load (CPL). When the source voltage falls, then the operation of the internal controller results in the converter drawing more

current. This in turn could cause the source voltage to fall even further.

The negative incremental impedance of a CPL means that it has a hyperbolic characteristic of the voltage against current. CPL can be modeled as a dependent current source, that is $i = v/P$, where v in the input voltage and P is the output power. A CPL can be constructed using Analogue Behavior Model (ABM) using block GVALUE in Orcard PSpice simulator. In order to ensure constant power, GVALUE is used as a voltage control current source (VCCS), in such away that it tries to maintain constant current by controlling the voltage of the DC bus voltage. A simple CPL model with bus voltage V and power level P is shown in Figure 1. It shows that constant current is obtained by power (P) divided by voltage (v). Figure 2 shows the CPL characteristic as the input voltage varies with P is set to 1 kW. It clearly shows that as the input voltage increases, the current decreases as expected, the symbol of the impedance can be expressed as $-R_L$.

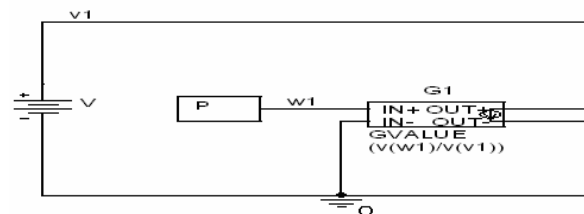


Figure 1. CPL block diagram

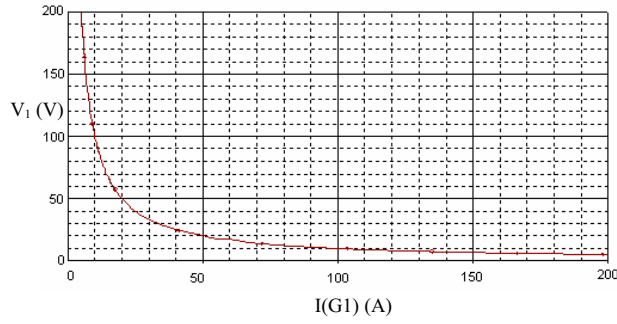


Figure 2. The CPL characteristics

The instability phenomenon causes by the interaction of LC filter and CPL can be shown in a simple circuit, Figure 3. The L-C filter and a CPL are connected to supply voltage of 270 Vdc. The values is chosen based on typical practical values. The input voltage disturbance V_3 with magnitude of 50 V is injected. The simulation result is shown in Figure 4. The plot shows that prior to the disturbance, the bus voltage V_2 is stable at 270 V. As the disturbance voltage is imposed at simulation time of 4 ms, the bus voltage experiences oscillation and ringing which indicates instability in the system due to the interaction of the negative incremental input impedance of the CPL with the input filter.

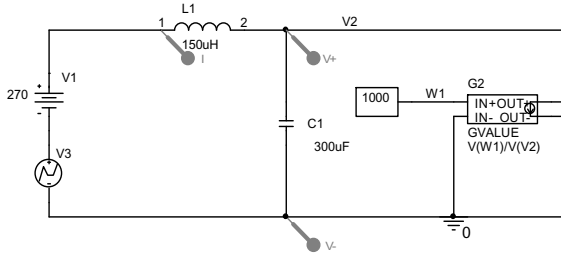


Figure 3. LC Filter with CPL

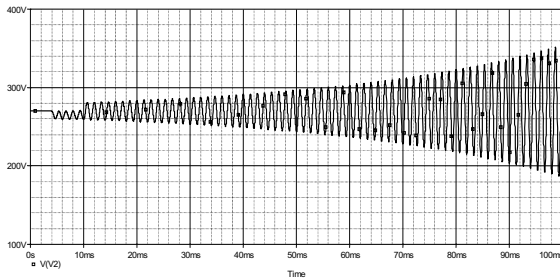


Figure 4. Bus voltage as 50 V input voltage imposed.

2. ANALYSIS

Although there is always some natural damping in the L-C filter due to the parasitic components such as equivalent series resistor in the inductor, normally it is not enough to damp instability. The schematic diagram with the insertion of RC passive damping network is shown in Figure 5. The series damping capacitor used to block DC thus prevent DC current from entering the

damping resistor. On the other hand, the damping resistor performs the damping function at filter resonant frequency. Figure 5 shows a constant power load ($-R_L$) connected to the L- C_1 filter with a RC $_2$ passive damping network. The total effective resistance of this circuit is

R_{eff} , where R_{eff} can be written as $R_{\text{eff}} = \frac{-RR_L}{R - R_L}$. Based

on stability criteria set by Middlebrook's[7], that is $R < R_L$ for a system to be stable, the passive damping resistor R has to be smaller than R_L so that the total effective resistance will be positive. The output to the input voltage transfer function of Figure 5 is given in Equation (1).

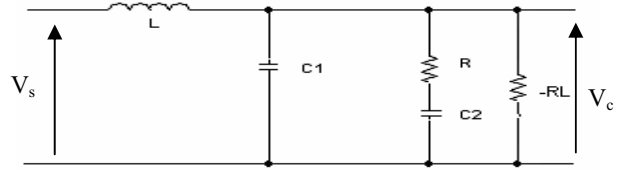


Figure 5: LC Filter with CPL and passive damping network

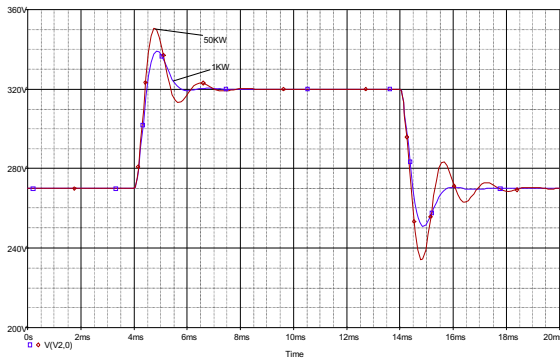
$$\frac{V_C}{V_s} = \frac{(1 + sC_2R)}{LC_1C_2R} \cdot \frac{1}{s^3 + s^2 \left(\frac{C_1R_L + C_2R_L - C_2R}{C_1C_2RR_L} \right) + s \left(\frac{C_2RR_L - L}{LC_1C_2R_LR} \right) + \frac{1}{LC_1C_2R}} \quad (1)$$

By equating the denominator part of Equation (1) to zero, and rearranging this characteristic yields Equation (2).

$$-R = -\frac{1}{K} = \frac{s^2(LC_1R_L + LC_2R_L) - sL + R_L}{s^3LC_1C_2R_L - s^2LC_2 + sR_LC_2} \quad (2)$$

Equation (2) actually is a root locus plot where a parameter (R) can be adjusted so that the system poles can be located as a specific place in s -plane for stability purposes. The plot of pole movements as the damping resistor R varies is given in Figure 6. Parameters used are: $L = 150\mu\text{H}$, $C_1 = 300\mu\text{F}$, $C_2 = 1.2\text{mF}$ and 5 different values of CPL resistance (R_L) are 0.3 Ω , 0.6 Ω , 1 Ω , 5 Ω and 30 Ω . These values are equivalent to the CPL power level of 243 kW, 122 kW, 73 kW, 14.6 kW and 2.4 kW, i.e $\left(R_L = \frac{V^2}{P} \right)$. The DC voltage source applied is 270 V.

Figure 6 indicates that the poles are in the right half plane for a damping resistor of zero and infinity. As the damping resistance varies between zero and infinity the poles move to the left, and may cross into the left-half plane, as in the case for $R_L = 0.6 \Omega$ and above. With $R_L = 0.3 \Omega$ the system remains unstable for all values of damping resistance, showing the limitation of the approximate stability condition derived earlier, namely $R < |R_L|$.

Figure 8. Simulated bus voltage V_2

The effectiveness of the passive damper can be proven further. In this case, the CPL is connected to DC bus bar through a long cabling system. Typical components values for the cabling can be represented by the series R-L element [8]. This can be shown in Figure 9 where R_3 - L_3 is the cable parameter. C_5 is a decoupling capacitor normally connected across CPL. The simulation results of the bus voltage without passive damping is shown in Figure 10, with CPL power level of 5 kW connected through. The plot shows that at simulation time of 200 ms, a +10V voltage transient was imposed for a 40 ms period of simulation. There is severe oscillatory response in the bus voltage. Likewise the same phenomena can be observed as the voltage step down -10V at 260 ms simulation time.

However with the insertion of the passive damping network, the problem of bus interaction and instability phenomena were eliminated. This is shown in the plot of Figure 11. The plot shows that at simulation time 200 ms, +10V voltage transient is imposed for a period of 40 ms, and at simulation time of 260 ms, a -10 V voltage transient is again imposed for the period of time of 50 ms. The plot shows that the system is well damped where the bus voltage experiences a single overshoot and then quickly settle to the steady-state value, illustrating the effectiveness of the damping network.

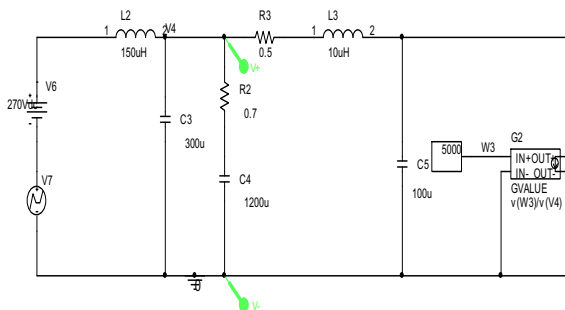
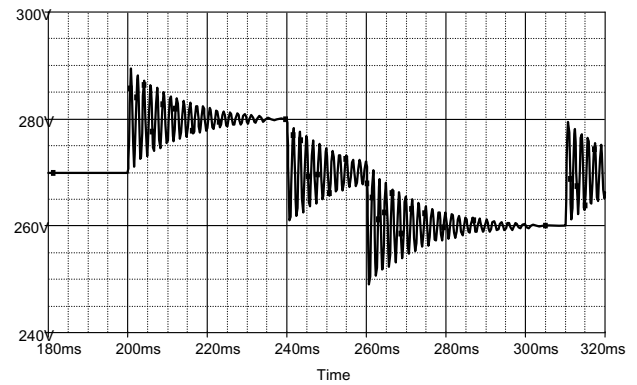
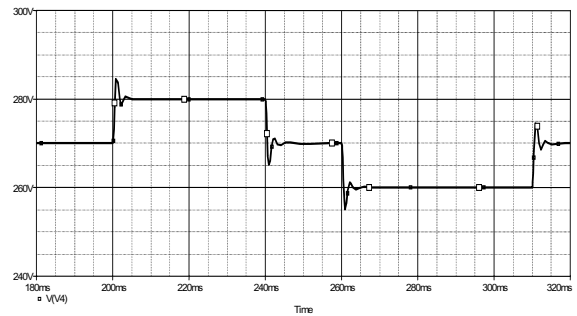


Figure 9. Schematic diagram with R-L cabling connected

Figure 10. Simulated bus voltage V_2 without passive dampingFigure 11. Simulated bus voltage V_2 with passive damping

5. CONCLUSION

The analysis, theoretical design and simulation of the RC damping network were examined extensively in a simple system consisting of LC filter and constant power load. Detail analysis and design of obtaining the damper components for CPL of 1 kW were given. The PSpice simulation results show the effectiveness of the designed passive damping network that satisfactorily maintained the DC bus bar from any oscillation due to the interaction of negative incremental impedance and LC filter. The simulation result also proved that the designed RC damping network could be further implemented for higher CPL power level of 5 kW.

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